W25Q33PW

# 1.8V 32M-BIT
# SERIAL NOR FLASH MEMORY WITH
# DUAL/QUAD SPI

*Publication Release Date: January 8, 2025*
*-Revision C*

## Table of Contents

# 1. GENERAL DESCRIPTIONS

The W25Q33PW (32M-BIT) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 1.65V to 1.95V power supply with current consumption as low as 0.1µA for power-down. All devices are offered in space-saving packages.

The W25Q33PW array is organized into 8,192 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q33PW has 512 erasable sectors and 32 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See figure 2.)

The W25Q33PW array is organized into 16,384 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q33PW has 1,024 erasable sectors and 64 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See Figure 2.)

Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP Register, a 64-bit Unique Serial Number and three 256-bytes Security Registers.

# 2. FEATURES

- **New Family of SpiFlash Memories**
  – W25Q33PW: 32M-BIT / 1M-byte
  – Standard SPI: CLK, /CS, DI, DO, /WP
  – Dual SPI: CLK, /CS, $IO_0$, $IO_1$, /WP
  – Quad SPI: CLK, /CS, $IO_0$, $IO_1$, $IO_2$, $IO_3$
  – Software Reset
  – JEDEC Reset Signaling Protocol
  – Page Buffer
- **Highest Performance Serial Flash**
  – 133MHz Single, Dual/Quad SPI clocks
  – 266/512MHz equivalent Dual/Quad SPI
  – 62MB/S continuous data transfer rate
  – Min. 100K Program-Erase cycles
  – More than 20-year data retention
- **Efficient "Continuous Read"**
  – Continuous Read with 8/16/32/64-Byte Wrap
  – Allows true XIP (execute in place) operation
  – Outperforms X16 Parallel Flash

– Allows true XIP (execute in place) operation
– Outperforms X16 Parallel Flash

- **Flexible Architecture with 4KB sectors**
  – Uniform Sector/Block Erase (4K/32K/64K-Byte)
  – Program 1 to 256 byte per programmable page
  – Erase/Program Suspend & Resume
- **Advanced Security Features**
  – Software and Hardware Write-Protect
  – Power Supply Lock-Down and OTP protection
  – Top/Bottom, Complement array protection
  – 64-Bit Unique ID for each device
  – Discoverable Parameters (SFDP) Register
  – 3X256-Bytes Security Registers with OTP locks
  – Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging**
  – 8-pin SOIC 150/208-mil
  – 8-pad XSON 2x3x0.4-mm
  – 8-pad USON 4X3-mm
  – Contact Winbond for KGD and other options

# 3. PACKAGE TYPES AND PIN CONFIGURATIONS

## 3.1 Pin Configuration SOIC 150-mil/208-mil

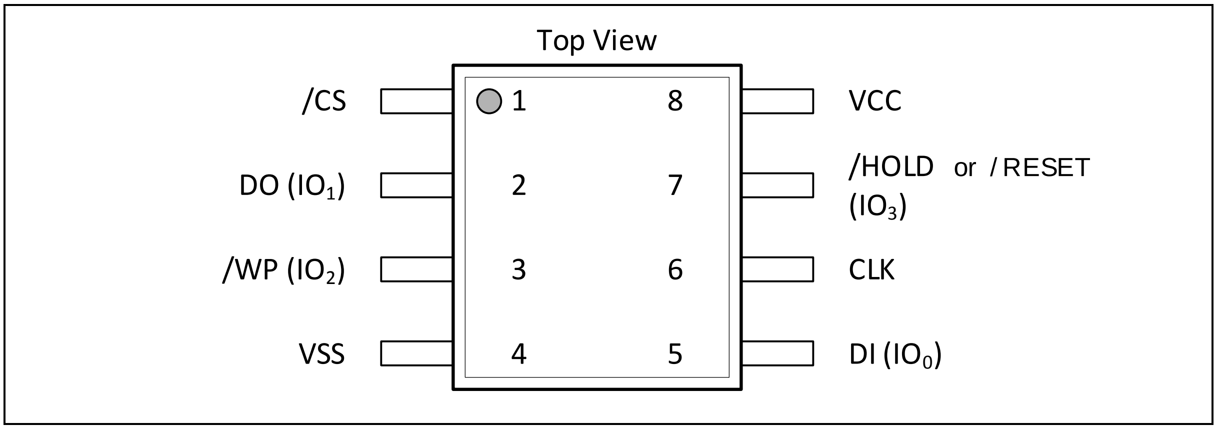



Figure 1a. W25Q33PW Pin Assignments, 8-pin SOIC (Package Code SN/SS)

## 3.2 Pad Configuration XSON 2x3-mm & USON 4X3

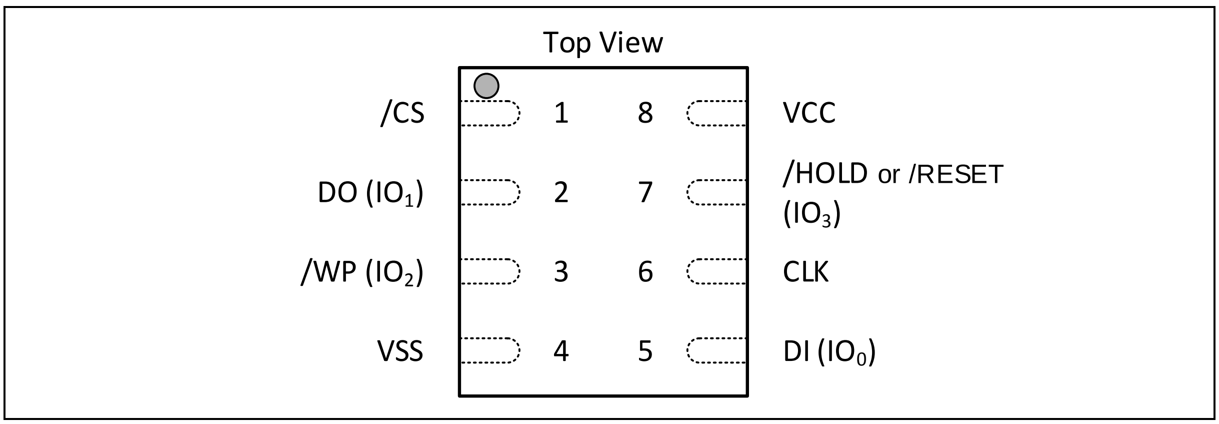



Figure 1b. W25Q33PW Pad Assignments, 8-pad WSON 6x5-mm (Package Code XH/UU)

## 3.3 Pin Description SOIC 150/ 208-mil, XSON 2x3-mm,USON 4X3-mm

| PIN NO. | PIN NAME | I/O | FUNCTION |
|---|---|---|---|
| 1 | /CS | I | Chip Select Input |
| 2 | DO (IO1) | I/O | Data Output (Data Input Output 1)(1) |
| 3 | /WP (IO2) | I/O | Write Protect Input ( Data Input Output 2)(2) |
| 4 | VSS | | Ground |
| 5 | DI (IO0) | I/O | Data Input (Data Input Output 0)(1) |
| 6 | CLK | I | Serial Clock Input |
| 7 | /HOLD or /RESET (IO3) | I/O | Hold or Reset Input (Data Input Output 3)(2) |
| 8 | VCC | | Power Supply |

**Notes:**

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /HOLD (or /RESET) functions are only available for Standard/Dual SPI.

# 4. PIN DESCRIPTIONS

## 4.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 58). If needed a pull-up resister on the /CS pin can be used to accomplish this.

## 4.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25Q33PW supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

## 4.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /WP pin function is not available since this pin is used for IO2. See Figure 1a-c for the pin configuration of Quad I/O operation.

## 4.4 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See Figure 1a-c for the pin configuration of Quad I/O operation.

## 4.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

## 5. BLOCK DIAGRAM

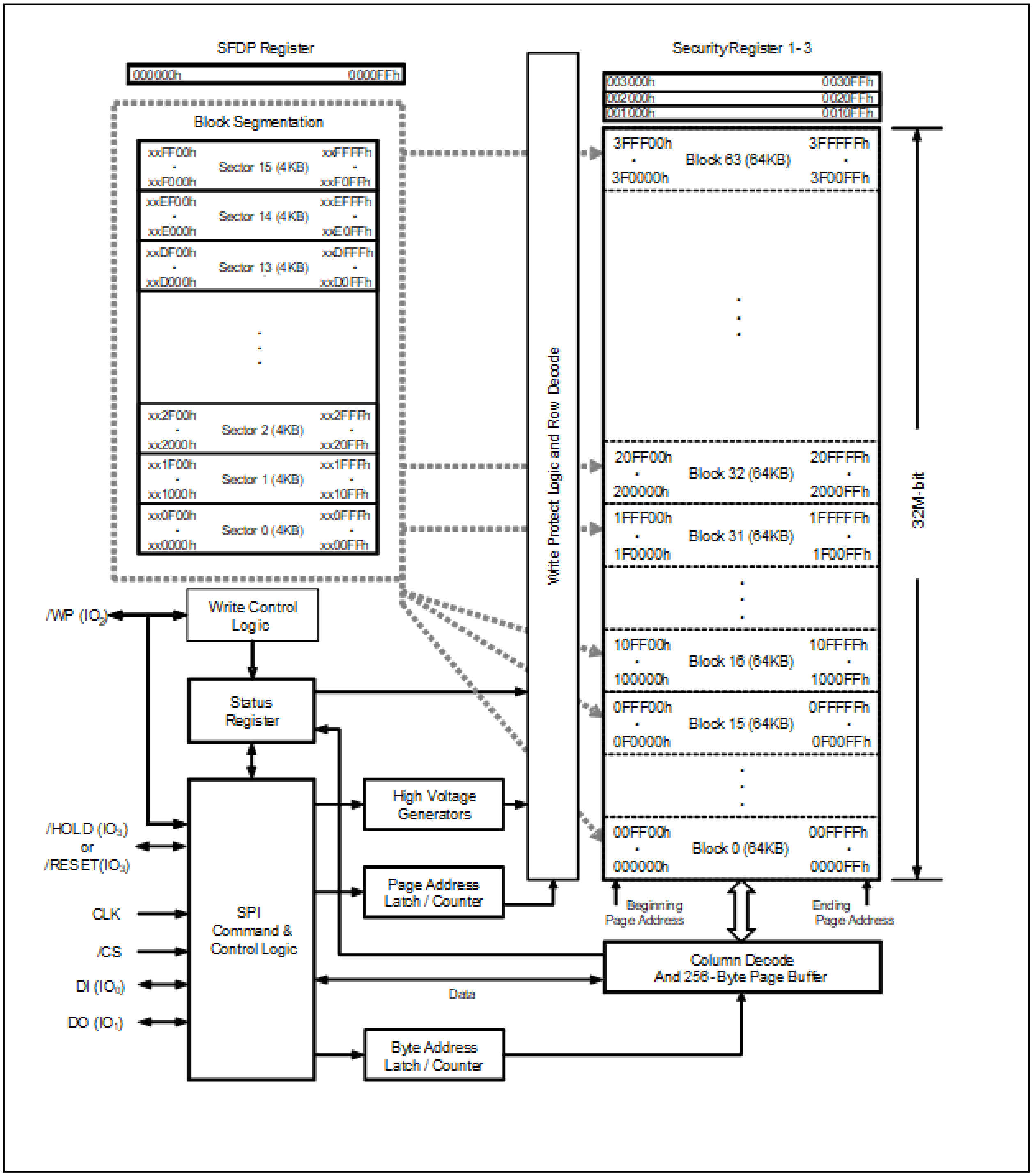



Figure 2. W25Q33PW Serial Flash Memory Block Diagram

# 6. FUNCTIONAL DESCRIPTIONS

## 6.1 SPI Operations

### 6.1.1 Standard SPI Instructions

The W25Q33PW is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

### 6.1.2 Dual SPI Instructions

The W25Q33PW supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

### 6.1.3 Quad SPI Instructions

The W25Q33PW supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, and “Fast Read Quad I/O (EBh). These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

### 6.1.4 Software Reset

The W25Q33PW can be reset to the initial power-on state by a software Reset sequence. This sequence must include two consecutive instructions: Enable Reset (66h) & Reset (99h). If the instruction sequence is successfully accepted, the device will take approximately 30uS ($t_{RST}$) to reset. No instruction will be accepted during the reset period.

If QE bit is set to 1, the /HOLD or /RESET function will be disabled, the pin will become one of the four data I/O pins.

### 6.1.5 JEDEC Reset Signaling Protocol

Winbond's new product supports the JEDEC Hardware Reset Protocol, as defined by the JESD 252 standard, titled "Serial Flash Reset Signaling Protocol." This standard defines a signaling protocol that allows a host to reset a Serial Flash device without needing a dedicated hardware reset pin or a software Reset instruction. This functionality requires the correct sequencing of /CS, CLK, and DI signals, and the internal Flash needs approximately $t_{RST2}$ = 100ms to execute the protocol reset.

## 6.2 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25Q33PW provides several means to protect the data from inadvertent writes.

### 6.2.1 Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Status Registers
- Write Protection using Power-down instruction
- Lock Down write protection for Status Register until the next power-up
- One Time Program (OTP) write protection for array and Security Registers using Status Register*

  * Note: This feature is available upon special flow. Please contact Winbond for details.

Upon power-up or at power-down, the W25Q33PW will maintain a reset condition while VCC is below the threshold value of $V_{WI}$, (See Power-up Timing and Voltage Levels and Figure 43). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds $V_{WI}$, all program and erase related instructions are further disabled for a time delay of $t_{PUW}$. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and $t_{VSL}$ time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse instruction sequence. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP, SRL) and Block Protect (CMP, SEC, TB, BP[2:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

## 6.3 Page Buffer

In Standard SPI mode, one of the new powerful features of the W25Q33PW is the integrated Serial SRAM buffer and its associated Program Buffer. Together, the 256-byte Serial SRAM provides usable SRAM storage. The SRAM can be used in conjunction with the Flash memory or independently. The main purpose of the Serial SRAM is to serve as the primary buffer for data to be written into the Serial Flash memory array. In case of need, it can help to transform random Byte Write to page Program Buffer.

Using the Write Buffer instruction, data is first shifted into the SRAM from the SPI bus. When the instruction sequence has been completed, the entire 256-bytes is transferred to the Program Buffer. The Program Buffer supports the array during the Erase/Write cycle (tWP), freeing the SRAM to accept new data. This double-buffering scheme increases erase/write transfer rates and can eliminate the need for external RAM buffers (Figure 3). The SRAM is fully byte-addressable. Thus, the entire 256-bytes, a single byte, or a sequence of bytes can be read from or written to the SRAM. This allows the SRAM to be used as a temporary work area for read-modify-write operations prior to a sector write.

The Transfer Sector to SRAM instruction allows the con- tents of a specified sector of Flash memory to be moved to the SRAM. This can be useful when only a portion of a sector needs to be altered. In this case the sector is first transferred to the SRAM, where modifications are made using the Write to SRAM instruction. Once complete, a Transfer SRAM to Sector instruction is used to update the sector.

Page Buffer control instruction as below:

- Clear Buffer(81h): Reset all the bit in the Page Buffer becomes ‘1’.
- Write Buffer(82h): Write the data into the Page Buffer, from the 1st byte to the 256th byte.
- Read Buffer(83h): Read out the data from Page Buffer.
- Program Buffer(8Ah): Write the Page Buffer data into the specified Flash Physical memory page.
- Load Buffer(8Bh): Read the data from the specified Flash Physical memory page into the Page Buffer.

Upon power off or the execution of a reset, all bits in the Page Buffer become ‘1’, effectively clearing the buffer. After Release Power-down(ABh), a clear buffer command must be issued.”

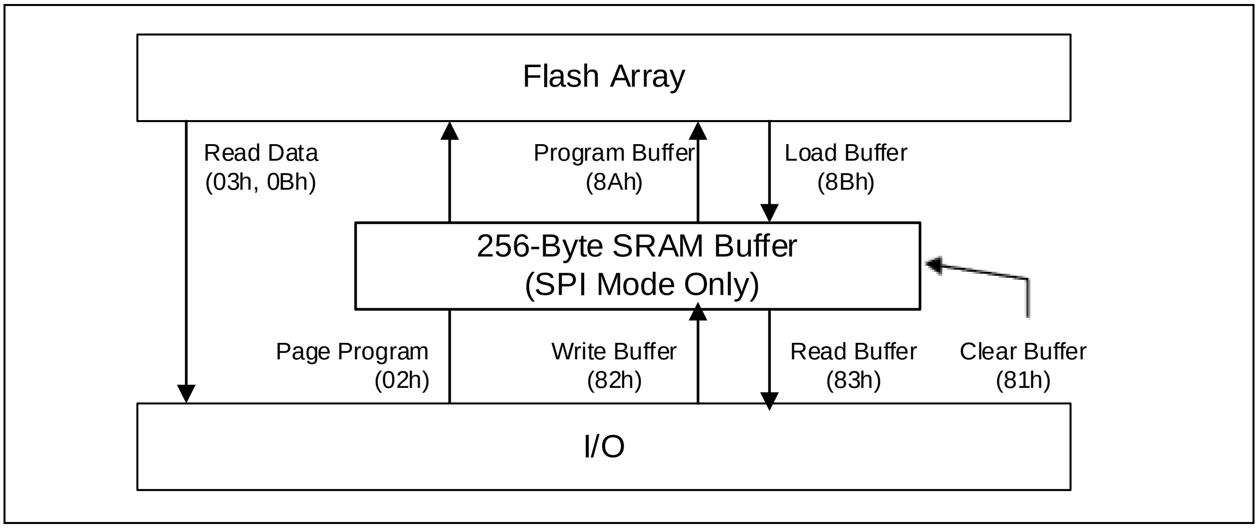



Figure 3. Serial Flash Buffer Mode

“For details, please refer to the application note on ‘Winbond SPI NOR Flash Page Buffer Operation.’

## 7. STATUS AND CONFIGURATION REGISTERS

Three Status and Configuration Registers are provided for W25Q33PW. The Read Status Register-1/2/3 instructions can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status, and output driver strength. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, Hold/Reset functions and output driver strength. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP, SRL), the Write Enable instruction, and during Standard/Dual SPI operations, the /WP pin.

### 7.1 Status Registers

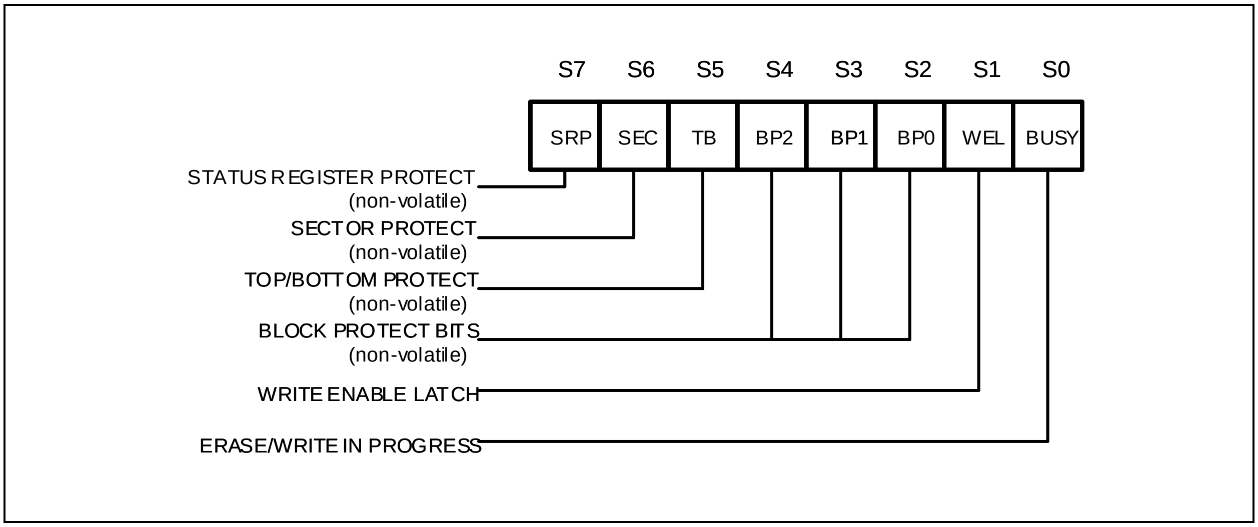



Figure 4a. Status Register-1

#### 7.1.1 Erase/Write In Progress (BUSY) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

#### 7.1.2 Write Enable Latch (WEL) – *Status Only*

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

#### 7.1.3 Block Protect Bits (BP2, BP1, BP0) – *Volatile/Non-Volatile Writable*

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

### 7.1.4 Top/Bottom Block Protect (TB) – *Volatile/Non-Volatile Writable*

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP, SRL and WEL bits.

### 7.1.5 Sector/Block Protect Bit (SEC) – *Volatile/Non-Volatile Writable*

The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The default setting is SEC=0.

### 7.1.6 Complement Protect (CMP) – *Volatile/Non-Volatile Writable*

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 64KB block can be protected while the rest of the array is not; when CMP=1, the top 64KB block will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

### 7.1.7 Status Register Protect (SRP, SRL)

The Status Register Protect bits (SRP) are non-volatile read/write bits in the status register (S7). The SRP bit controls the method of write protection: software protection or hardware protection. The Status Register Lock bits (SRL) are non-volatile/volatile read/write bits in the status register (S8). The SRL bit controls the method of write protection: temporary lock-down or permanently one time program.

<table>
<tr><th>SRP</th><th>/WP</th><th>Status Protection</th><th>Description</th></tr>
<tr><td>0</td><td>X</td><td>Software Protection</td><td>/WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default]</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>Hardware Protected</td><td>When /WP pin is low the Status Register can't be written to.</td></tr>
<tr><td>1</td><td>Hardware Unprotected</td><td>When /WP pin is high the Status register can be written to after a Write Enable instruction, WEL=1.</td></tr>
<tr><th>SRL</th><th colspan="2">Status Register Lock</th><th>Description</th></tr>
<tr><td>0</td><td colspan="2">Non-Lock</td><td>Status Register is unlocked</td></tr>
<tr><td rowspan="2">1</td><td colspan="2">Lock-Down (1)<br>(temporary/Volatile)</td><td>Status Register is locked by standard status register write instruction and can't be written to again until the next power-down, power-up cycle.</td></tr>
<tr><td colspan="2">One Time Program(2)<br>(Permanently/Non-Volatile)</td><td>Status Register is permanently locked by special instruction flow* and can't be written to</td></tr>
</table>

1. When SRL =1, a power-down, power-up cycle will change SRL =0 state.
2. Special One Time Protection feature is available upon special order; please contact Winbond for details

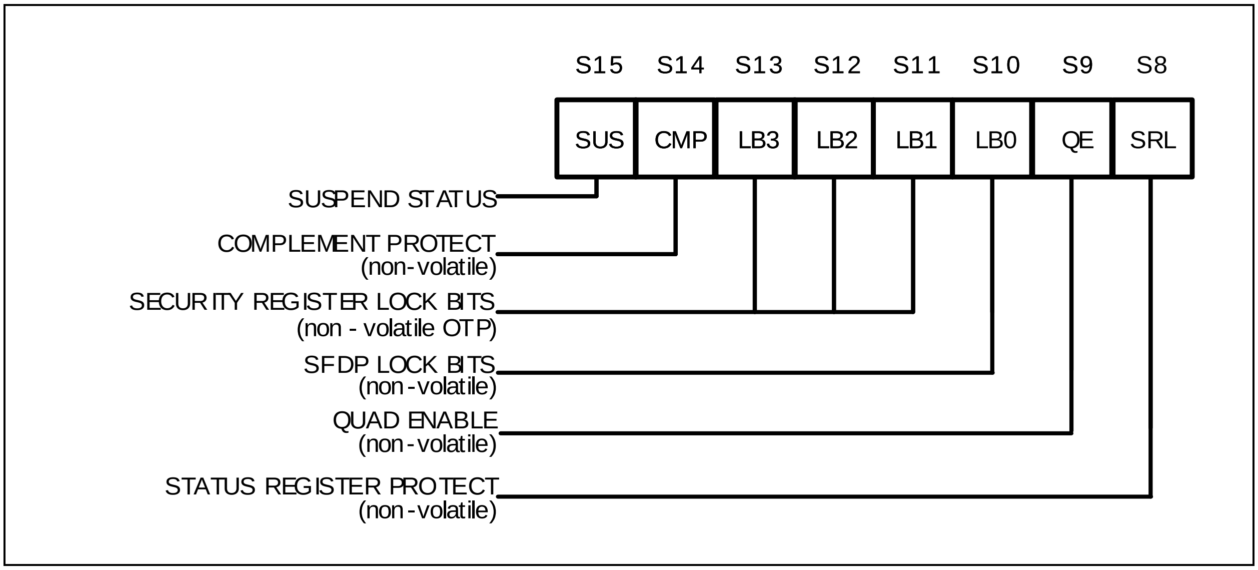



Figure 4b. Status Register-2

### 7.1.8 Erase/Program Suspend Status (SUS) – *Status Only*

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

### 7.1.9 Security Register Lock Bits (LB3, LB2, LB1,LB0) –*Volatile/Non-Volatile OTP Writable*

The Security Register Lock Bits (LB3, LB2, LB1,LB0) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11,S10) that provide the write protect control and status to the Security Registers. The default state of LB3-1 is 0, Security Registers are unlocked. LB3-1 can be set to 1 individually using the Write Status Register instruction. LB3-0 are One Time Programmable (OTP), once it’s set to 1, the corresponding 256-Byte Security Register will become read-only permanently.

The default state of LB0 is 1, SFDP Register is locked.

### 7.1.10 Quad Enable (QE) – *Volatile/Non-Volatile Writable*

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI and QPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options “IM”), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1(factory default for Quad Enabled part numbers with ordering option “IQ”), the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled.

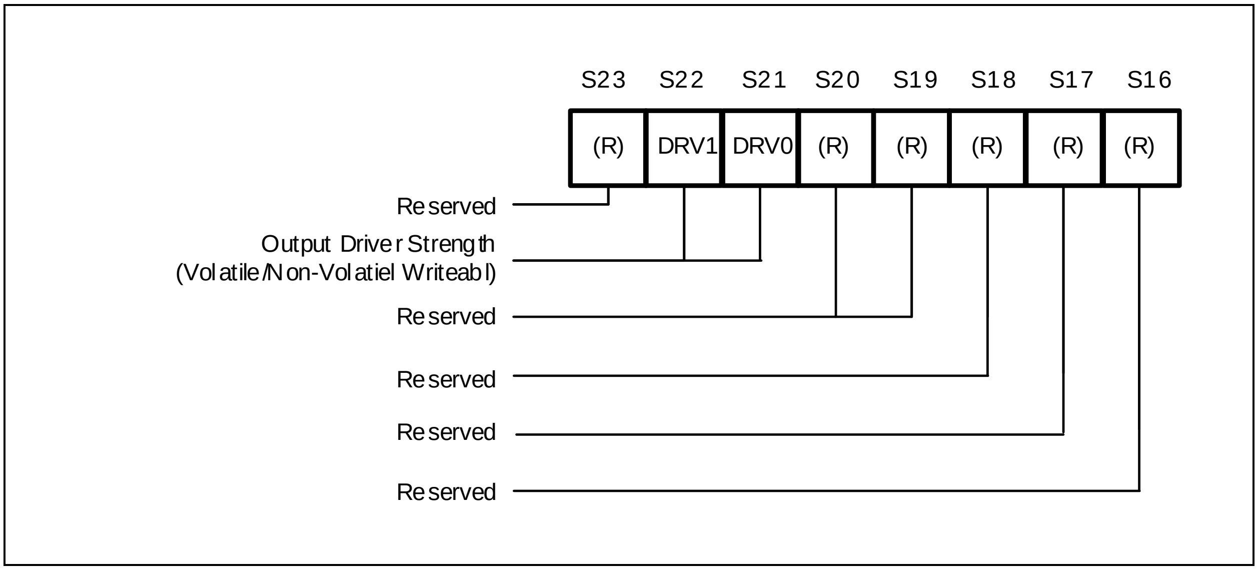



Figure 4c. Status Register-3

### 7.1.11 **Output Driver Strength (DRV1, DRV0) – *Volatile/Non-Volatile Writable***

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

| DRV1, DRV0 | Resistor |
|---|---|
| 0, 0 | 25-ohm |
| 0, 1 | 33-ohm |
| 1, 0 | 50-ohm(default) |
| 1, 1 | 100-ohm |

### 7.1.12 **Reserved Bits – *Non Functional***

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects.

### 7.1.13 Status Register Memory Protection (CMP = 0)

| STATUS REGISTER[1] | | | | | W25Q33PW (32M-BIT) MEMORY PROTECTION[3] | | | |
|---|---|---|---|---|---|---|---|---|
| SEC | TB | BP2 | BP1 | BP0 | PROTECTED BLOCK(S) | PROTECTED ADDRESSES | PROTECTED DENSITY | PROTECTED PORTION[2] |
| X | X | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | 63 | 3F0000h – 3FFFFFh | 64KB | Upper 1/64 |
| 0 | 0 | 0 | 1 | 0 | 62 and 63 | 3E0000h – 3FFFFFh | 128KB | Upper 1/32 |
| 0 | 0 | 0 | 1 | 1 | 60 thru 63 | 3C0000h – 3FFFFFh | 256KB | Upper 1/16 |
| 0 | 0 | 1 | 0 | 0 | 56 thru 63 | 380000h – 3FFFFFh | 512KB | Upper 1/8 |
| 0 | 0 | 1 | 0 | 1 | 48 thru 63 | 300000h – 3FFFFFh | 1MB | Upper 1/4 |
| 0 | 0 | 1 | 1 | 0 | 32 thru 63 | 200000h – 3FFFFFh | 2MB | Upper 1/2 |
| 0 | 1 | 0 | 0 | 1 | 0 | 000000h – 00FFFFh | 64KB | Lower 1/64 |
| 0 | 1 | 0 | 1 | 0 | 0 and 1 | 000000h – 01FFFFh | 128KB | Lower 1/32 |
| 0 | 1 | 0 | 1 | 1 | 0 thru 3 | 000000h – 03FFFFh | 256KB | Lower 1/16 |
| 0 | 1 | 1 | 0 | 0 | 0 thru 7 | 000000h – 07FFFFh | 512KB | Lower 1/8 |
| 0 | 1 | 1 | 0 | 1 | 0 thru 15 | 000000h – 0FFFFFh | 1MB | Lower 1/4 |
| 0 | 1 | 1 | 1 | 0 | 0 thru 31 | 000000h – 1FFFFFh | 2MB | Lower 1/2 |
| X | X | 1 | 1 | 1 | 0 thru 63 | 000000h – 3FFFFFh | 4MB | ALL |
| 1 | 0 | 0 | 0 | 1 | 63 | 3FF000h – 3FFFFFh | 4KB | U - 1/1024 |
| 1 | 0 | 0 | 1 | 0 | 63 | 3FE000h – 3FFFFFh | 8KB | U - 1/512 |
| 1 | 0 | 0 | 1 | 1 | 63 | 3FC000h – 3FFFFFh | 16KB | U - 1/256 |
| 1 | 0 | 1 | 0 | X | 63 | 3F8000h – 3FFFFFh | 32KB | U - 1/128 |
| 1 | 1 | 0 | 0 | 1 | 0 | 000000h – 000FFFh | 4KB | L - 1/1024 |
| 1 | 1 | 0 | 1 | 0 | 0 | 000000h – 001FFFh | 8KB | L - 1/512 |
| 1 | 1 | 0 | 1 | 1 | 0 | 000000h – 003FFFh | 16KB | L - 1/256 |
| 1 | 1 | 1 | 0 | X | 0 | 000000h – 007FFFh | 32KB | L - 1/128 |

**Notes:**

1. X = don't care
2. If any Erase or Program instruction specifies a memory region that contains protected data portion, this instruction will be ignored.

### 7.1.14 W25Q33PW Status Register Memory Protection (CMP = 1)

| STATUS REGISTER[(1)] | | | | | W25Q33PW (32M-BIT) MEMORY PROTECTION[(3)] | | | |
|---|---|---|---|---|---|---|---|---|
| SEC | TB | BP2 | BP1 | BP0 | PROTECTED BLOCK(S) | PROTECTED ADDRESSES | PROTECTED DENSITY | PROTECTED PORTION[(2)] |
| X | X | 0 | 0 | 0 | 0 thru 63 | 000000h – 3FFFFFh | 4MB | ALL |
| 0 | 0 | 0 | 0 | 1 | 0 thru 62 | 000000h – 3EFFFFh | 4,032KB | Lower 63/64 |
| 0 | 0 | 0 | 1 | 0 | 0 and 61 | 000000h – 3DFFFFh | 3,968KB | Lower 31/32 |
| 0 | 0 | 0 | 1 | 1 | 0 thru 59 | 000000h – 3BFFFFh | 3,840KB | Lower 15/16 |
| 0 | 0 | 1 | 0 | 0 | 0 thru 55 | 000000h – 37FFFFh | 3,584KB | Lower 7/8 |
| 0 | 0 | 1 | 0 | 1 | 0 thru 47 | 000000h – 2FFFFFh | 3MB | Lower 3/4 |
| 0 | 0 | 1 | 1 | 0 | 0 thru 31 | 000000h – 1FFFFFh | 2MB | Lower 1/2 |
| 0 | 1 | 0 | 0 | 1 | 1 thru 63 | 010000h – 3FFFFFh | 4,032KB | Upper 63/64 |
| 0 | 1 | 0 | 1 | 0 | 2 and 63 | 020000h – 3FFFFFh | 3,968KB | Upper 31/32 |
| 0 | 1 | 0 | 1 | 1 | 4 thru 63 | 040000h – 3FFFFFh | 3,840KB | Upper 15/16 |
| 0 | 1 | 1 | 0 | 0 | 8 thru 63 | 080000h – 3FFFFFh | 3,584KB | Upper 7/8 |
| 0 | 1 | 1 | 0 | 1 | 16 thru 63 | 100000h – 3FFFFFh | 3MB | Upper 3/4 |
| 0 | 1 | 1 | 1 | 0 | 32 thru 63 | 200000h – 3FFFFFh | 2MB | Upper 1/2 |
| X | X | 1 | 1 | 1 | NONE | NONE | NONE | NONE |
| 1 | 0 | 0 | 0 | 1 | 0 thru 63 | 000000h – 3FEFFFh | 4,092KB | L - 1023/1024 |
| 1 | 0 | 0 | 1 | 0 | 0 thru 63 | 000000h – 3FDFFFh | 4,088KB | L - 511/512 |
| 1 | 0 | 0 | 1 | 1 | 0 thru 63 | 000000h – 3FBFFFh | 4,080KB | L - 255/256 |
| 1 | 0 | 1 | 0 | X | 0 thru 63 | 000000h – 3F7FFFh | 4,064KB | L - 127/128 |
| 1 | 1 | 0 | 0 | 1 | 0 thru 63 | 001000h – 3FFFFFh | 4,092KB | U - 1023/1024 |
| 1 | 1 | 0 | 1 | 0 | 0 thru 63 | 002000h – 3FFFFFh | 4,088KB | U - 511/512 |
| 1 | 1 | 0 | 1 | 1 | 0 thru 63 | 004000h – 3FFFFFh | 4,080KB | U - 255/256 |
| 1 | 1 | 1 | 0 | X | 0 thru 63 | 008000h – 3FFFFFh | 4,064KB | U - 127/128 |

**Notes:**

1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program instruction specifies a memory region that contains protected data portion, this instruction will be ignored.

# 8. INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set of the W25Q33PW consists of 46 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table 1-2). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in Figures 5 through 57. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

## 8.1 Device ID and Instruction Set Tables

### 8.1.1 Manufacturer and Device Identification

| **MANUFACTURER ID** | **(MF7 - MF0)** | |
|---|---|---|
| Winbond Serial Flash | EFh | |
| | | |
| **Device ID** | **(ID7 - ID0)** | **(ID15 - ID0)** |
| **Instruction** | **ABh, 90h, 92h, 94h** | **9Fh** |
| W25Q33PW-Q | 15h | 6016h |

### 8.1.2 Instruction Set Table 1 (Standard SPI Instructions) [1]

| Data Input Output | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 | Byte 7 |
|---|---|---|---|---|---|---|---|
| **Number of Clock(1-1-1)** | **8** | **8** | **8** | **8** | **8** | **8** | **8** |
| Write Enable | **06h** | | | | | | |
| Volatile SR Write Enable | **50h** | | | | | | |
| Write Disable | **04h** | | | | | | |
| Release Power-down | **ABh** | | | | | | |
| Read ID | **ABh** | Dummy | Dummy | Dummy | (ID7-ID0)[2] | | |
| Manufacturer/Device ID | **90h** | Dummy | Dummy | 00h | (MF7-MF0) | (ID7-ID0) | |
| JEDEC ID | **9Fh** | (MF7-MF0) | (ID15-ID8) | (ID7-ID0) | | | |
| Read Unique ID | **4Bh** | Dummy | Dummy | Dummy | Dummy | (UID63-0) | |
| Read Data | **03h** | A23-A16 | A15-A8 | A7-A0 | (D7-D0) | | |
| Fast Read | **0Bh** | A23-A16 | A15-A8 | A7-A0 | Dummy | (D7-D0) | |
| Page Program | **02h** | A23-A16 | A15-A8 | A7-A0 | D7-D0 | D7-D0[3] | |
| Sector Erase (4KB) | **20h** | A23-A16 | A15-A8 | A7-A0 | | | |
| Block Erase (32KB) | **52h** | A23-A16 | A15-A8 | A7-A0 | | | |
| Block Erase (64KB) | **D8h** | A23-A16 | A15-A8 | A7-A0 | | | |
| Chip Erase | **C7h/60h** | | | | | | |
| Read Status Register-1 | **05h** | (S7-S0)[2] | | | | | |
| Write Status Register-1 | **01h** | (S7-S0) | | | | | |
| Read Status Register-2 | **35h** | (S15-S8)[2] | | | | | |
| Write Status Register-2 | **31h** | (S15-S8) | | | | | |
| Read Status Register-3 | **15h** | (S23-S16)[2] | | | | | |
| Write Status Register-3 | **11h** | (S23-S16) | | | | | |
| Read ECC Status Register | **25h** | (ER7-ER0) [2] | | | | | |
| Read SFDP Register | **5Ah** | A23-A16 | A15-A8 | A7-A0 | Dummy | (D7-D0) | |
| Erase Security Register[4] | **44h** | A23-A16 | A15-A8 | A7-A0 | | | |
| Program Security Register[4] | **42h** | A23-A16 | A15-A8 | A7-A0 | D7-D0[3] | | |
| Read Security Register[4] | **48h** | A23-A16 | A15-A8 | A7-A0 | Dummy | (D7-D0) | |
| Erase / Program Suspend | **75h** | | | | | | |
| Erase / Program Resume | **7Ah** | | | | | | |
| Power-down | **B9h** | | | | | | |
| Set Read Parameters | **C0h** | P7-P0 | | | | | |
| Enable Reset | **66h** | | | | | | |
| Reset Device | **99h** | | | | | | |
| **Page Buffer** | **Byte 1** | **Byte 2** | **Byte 3** | **Byte 4** | **Byte 5** | **Byte 6** | **Byte 7** |
| **Number of Clock (1-1-1)** | **8** | **8** | **8** | **8** | **8** | **8** | **8** |
| Clear Buffer | **81h** | A23-A16 | A15-A8 | A7-A0 | | | |
| Write Buffer | **82h** | A23-A16 | A15-A8 | A7-A0 | D7-D0 | D7-D0[3] | |
| Read Buffer | **83h** | A23-A16 | A15-A8 | A7-A0 | Dummy | (D7-D0) | … |
| Program Buffer | **8Ah** | A23-A16 | A15-A8 | A7-A0 | | | |
| Load Buffer | **8Bh** | A23-A16 | A15-A8 | A7-A0 | | | |

### 8.1.3 Instruction Set Table 2 (Dual/Quad SPI Instructions)[1]

| Data Input Output | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 | Byte 7 | Byte 8 | Byte 9 |
|---|---|---|---|---|---|---|---|---|---|
| **Number of Clock(1-1-2)** | **8** | **8** | **8** | **8** | **4** | **4** | **4** | **4** | **4** |
| Fast Read Dual Output | **3Bh** | A23-A16 | A15-A8 | A7-A0 | Dummy | Dummy | (D7-D0)[7] | | |
| **Number of Clock(1-2-2)** | **8** | **4**[5] | **4**[5] | **4**[5] | **4**[5] | **4** | **4** | **4** | **4** |
| Fast Read Dual I/O | **BBh** | A23-A16 | A15-A8 | A7-A0 | M7-M0[12] | (D7-D0)[6] | | | |
| Mftr./Device ID Dual I/O | **92h** | A23-A16 | A15-A8 | 00 | Fx[14] | (MF7-MF0) | (ID7-ID0)[6] | | |
| **Number of Clock(1-1-4)** | **8** | **8** | **8** | **8** | **2** | **2** | **2** | **2** | **2** |
| Quad Input Page Program | **32h** | A23-A16 | A15-A8 | A7-A0 | D7-D0[8] | D7-D0[3] | … | | |
| Fast Read Quad Output | **6Bh** | A23-A16 | A15-A8 | A7-A0 | Dummy | Dummy | Dummy | Dummy | (D7-D0)[9] |
| **Number of Clock(1-4-4)** | **8** | **2**[7] | **2**[7] | **2**[7] | **2** | **2** | **2** | **2** | **2** |
| Mftr./Device ID Quad I/O | **94h** | A23-A16 | A15-A8 | 00 | Fx[12] | Dummy | Dummy | (MF7-MF0) | (ID7-ID0) |
| Fast Read Quad I/O | **EBh** | A23-A16 | A15-A8 | A7-A0 | M7-M0[12] | Dummy | Dummy[10,11] | (D7-D0) | |
| Set Burst with Wrap | **77h** | Dummy | Dummy | Dummy | W7-W0[11] | | | | |

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data output from the device on either 1, 2 or 4 IO pins.
2. The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. Security Register Address:
   Security Register 1: A23-16 = 00h; A15-8 = 10h; A7-0 = byte address
   Security Register 2: A23-16 = 00h; A15-8 = 20h; A7-0 = byte address
   Security Register 3: A23-16 = 00h; A15-8 = 30h; A7-0 = byte address
5. Dual SPI address input format:
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
6. Dual SPI data output format:
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
7. Quad SPI address input format:
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3

   Set Burst with Wrap input format:
   IO0 = x, x, x, x, x, x, W4, x
   IO1 = x, x, x, x, x, x, W5, x
   IO2 = x, x, x, x, x, x, W6, x
   IO3 = x, x, x, x, x, x, x, x
8. Quad SPI data input/output format:
   IO0 = (D4, D0, …..)
   IO1 = (D5, D1, …..)
   IO2 = (D6, D2, …..)
   IO3 = (D7, D3, …..)
9. Fast Read Quad I/O data output format:
   IO0 = (x, x, x, x, D4, D0, D4, D0)
   IO1 = (x, x, x, x, D5, D1, D5, D1)
   IO2 = (x, x, x, x, D6, D2, D6, D2)
   IO3 = (x, x, x, x, D7, D3, D7, D3)
10. The number of dummy clocks for SPI Fast Read Quad I/O Read with is controlled by read parameter P6 – P4. The number of dummy clocks for
11. “Set Burst Wrap (77h)” instruction controls enable/disable of wrap around and sets the wrap length.
12. The first dummy is the “Read Instruction Bypass Mode” bits M(7-0) should be set to Fxh

## 8.2 Instruction Descriptions

### 8.2.1 Write Enable (06h)

The Write Enable instruction (Figure 5) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

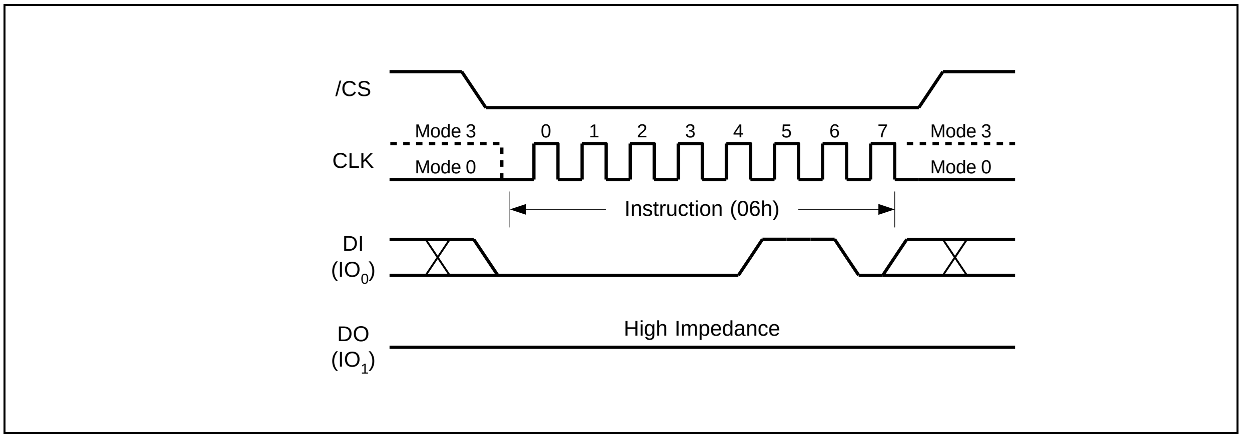



Figure 5. Write Enable Instruction for SPI Mode

### 8.2.2 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 7.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 6) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

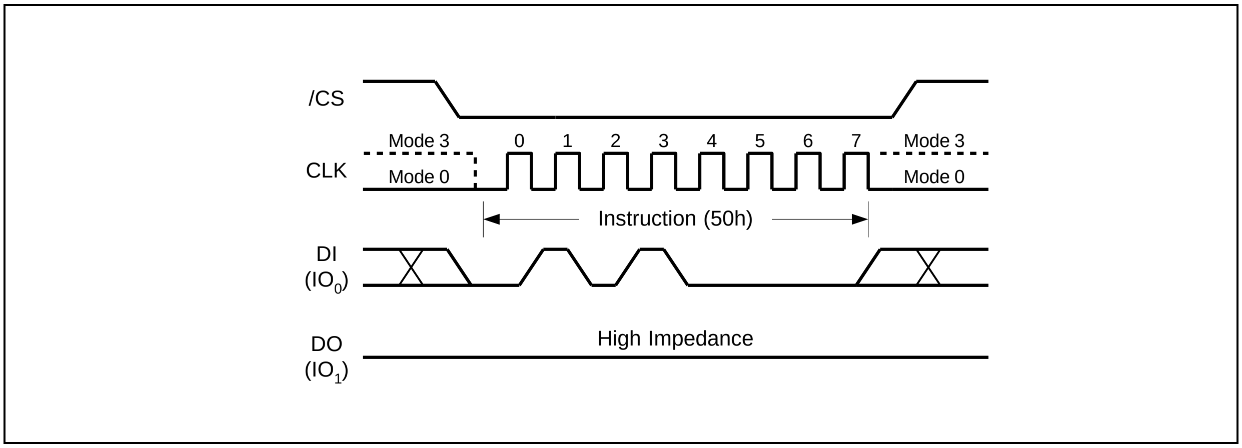



Figure 6. Write Enable for Volatile Status Register Instruction for SPI Mode

### 8.2.3 Write Disable (04h)

The Write Disable instruction (Figure 7) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code "04h" into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase and Reset instructions.

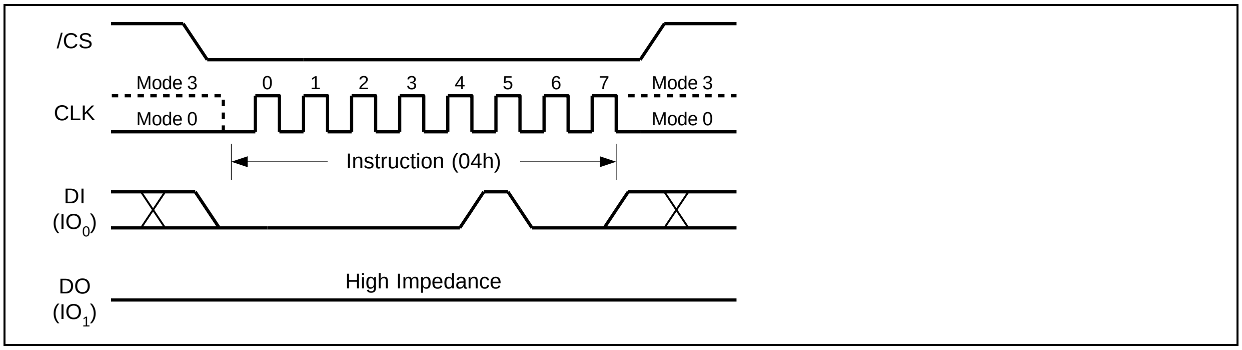



Figure 7. Write Disable Instruction for SPI Mode

### 8.2.4 Read Status Register-1 (05h), Status Register-2 (35h) & Status Register-3 (15h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code "05h" for Status Register-1, "35h" for Status Register-2 or "15h" for Status Register-3 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 8. Refer to section 7.1 for Status Register descriptions.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 8. The instruction is completed by driving /CS high.

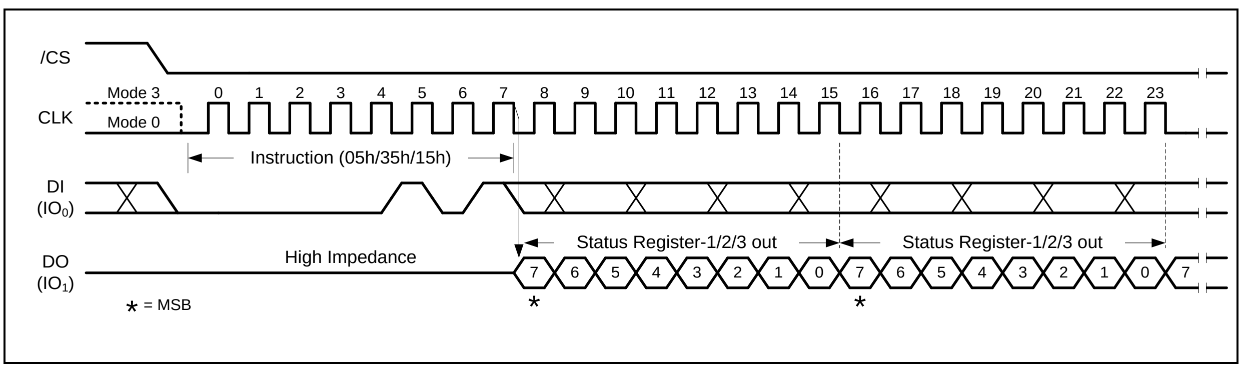



Figure 8a. Read Status Register Instruction

### 8.2.5 Write Status Register-1 (01h), Status Register-2 (31h) & Status Register-3 (11h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SRP, SEC, TB, BP[2:0] in Status Register-1; CMP, LB[3:1], QE, SRL in Status Register-2; DRV1, DRV0, in Status Register-3. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB[3:1] are non-volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code "01h/31h/11h", and then writing the status register data byte as illustrated in Figure 9a & 9b.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRL and LB[3:1] cannot be changed from "1" to "0" because of the OTP protection for these bits. Upon power off or the execution of a Software Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During non-volatile Status Register write operation (06h combined with 01h/31h/11h), after /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tw (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of $t_{SHSL2}$ (See AC Characteristics). BUSY bit will remain 0 during the Status Register bit refresh period.

Refer to section 7.1 for Status Register descriptions.

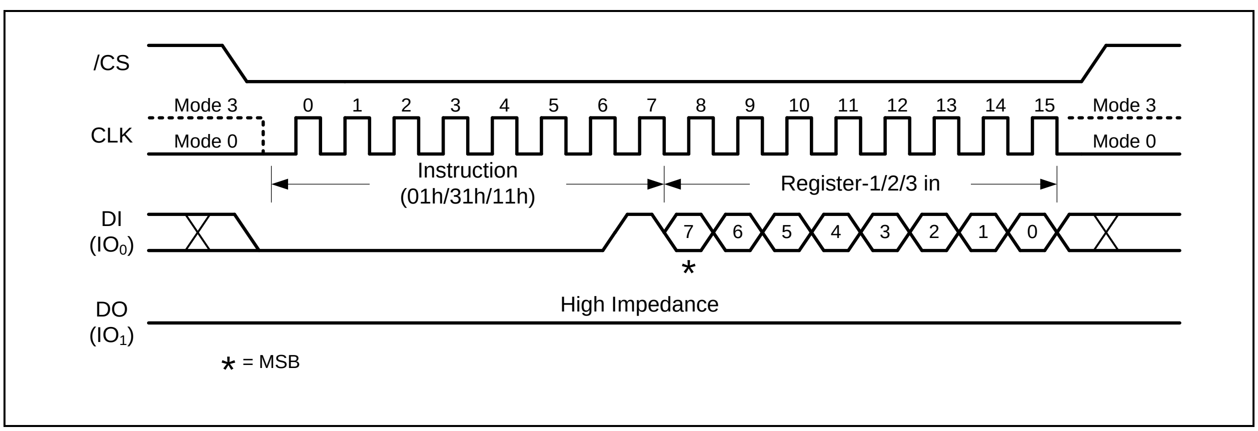



Figure 9a. Write Status Register-1/2/3 Instruction

### 8.2.6 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in Figure 14. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of $f_R$ (see AC Electrical Characteristics).

The Read Data (03h) instruction is only supported in Standard SPI mode.

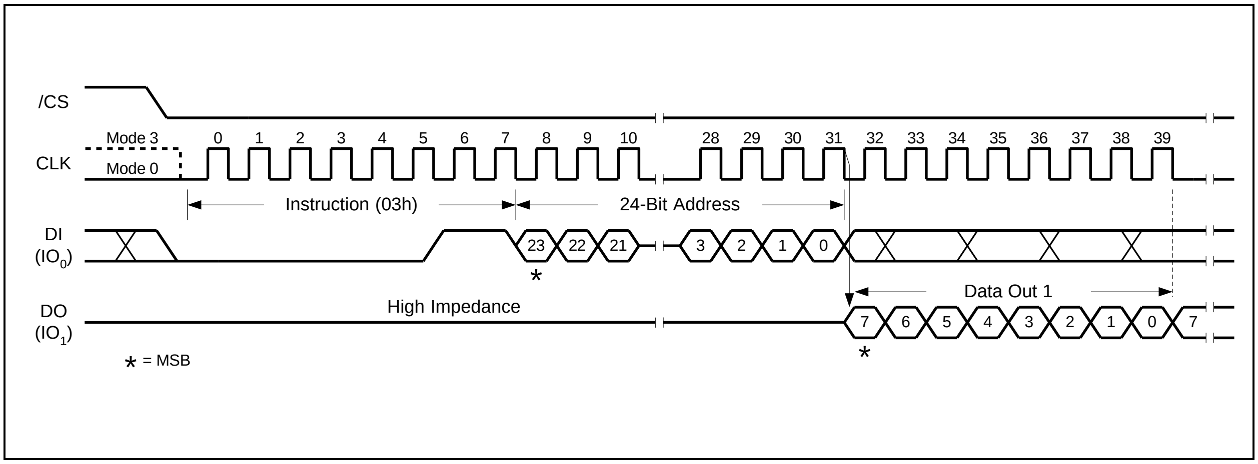



Figure 14. Read Data Instruction

### 8.2.7 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in Figure 16. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a "don't care".

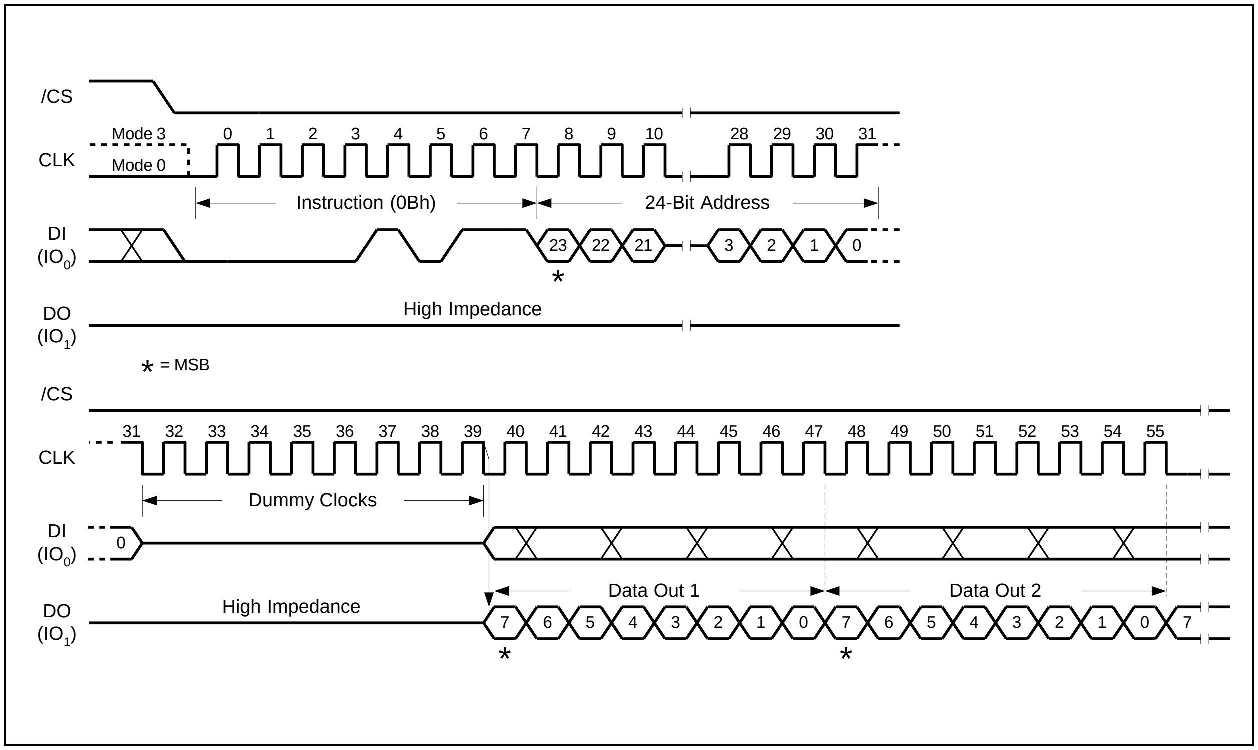



Figure 16a. Fast Read Instruction

### 8.2.8 ast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; $IO_0$ and $IO_1$. This allows data to be transferred at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in Figure 18. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the $IO_0$ pin should be high-impedance prior to the falling edge of the first data out clock.

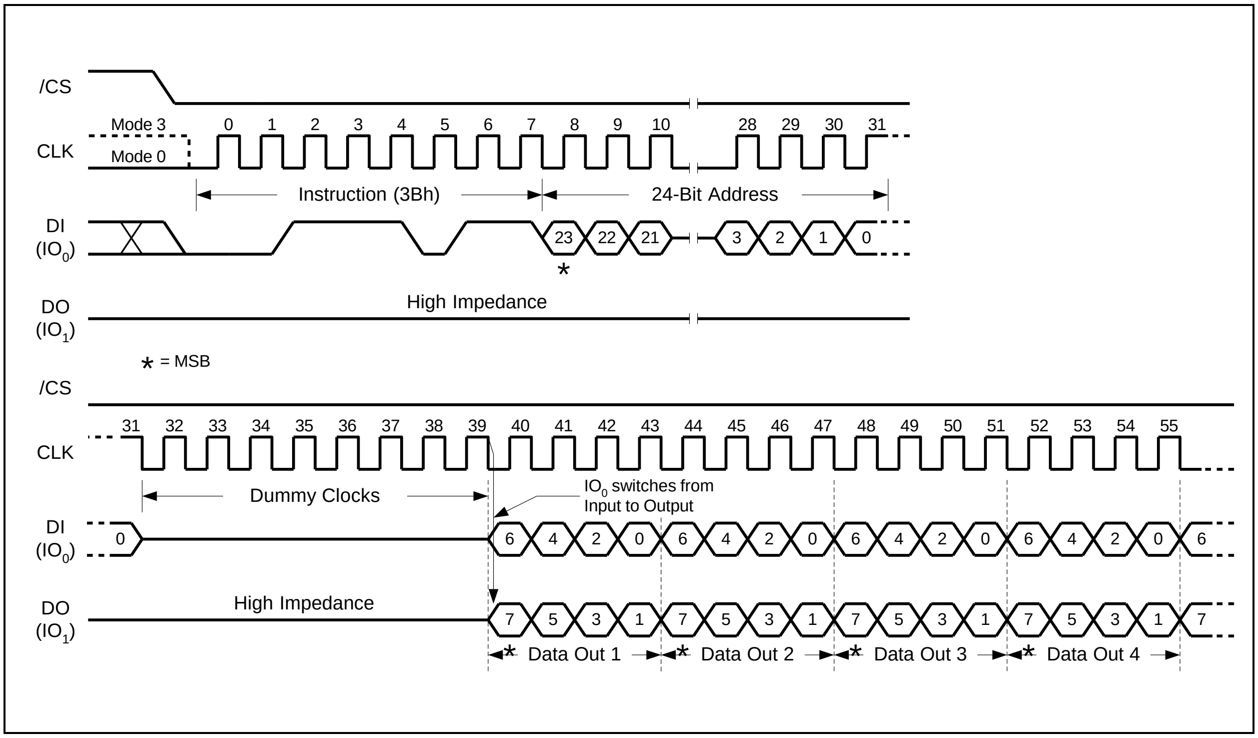



Figure 18. Fast Read Dual Output Instruction

### 8.2.9 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, $IO_0$, $IO_1$, $IO_2$, and $IO_3$. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the Fast Read Quad Output Instruction. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in Figure 20. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

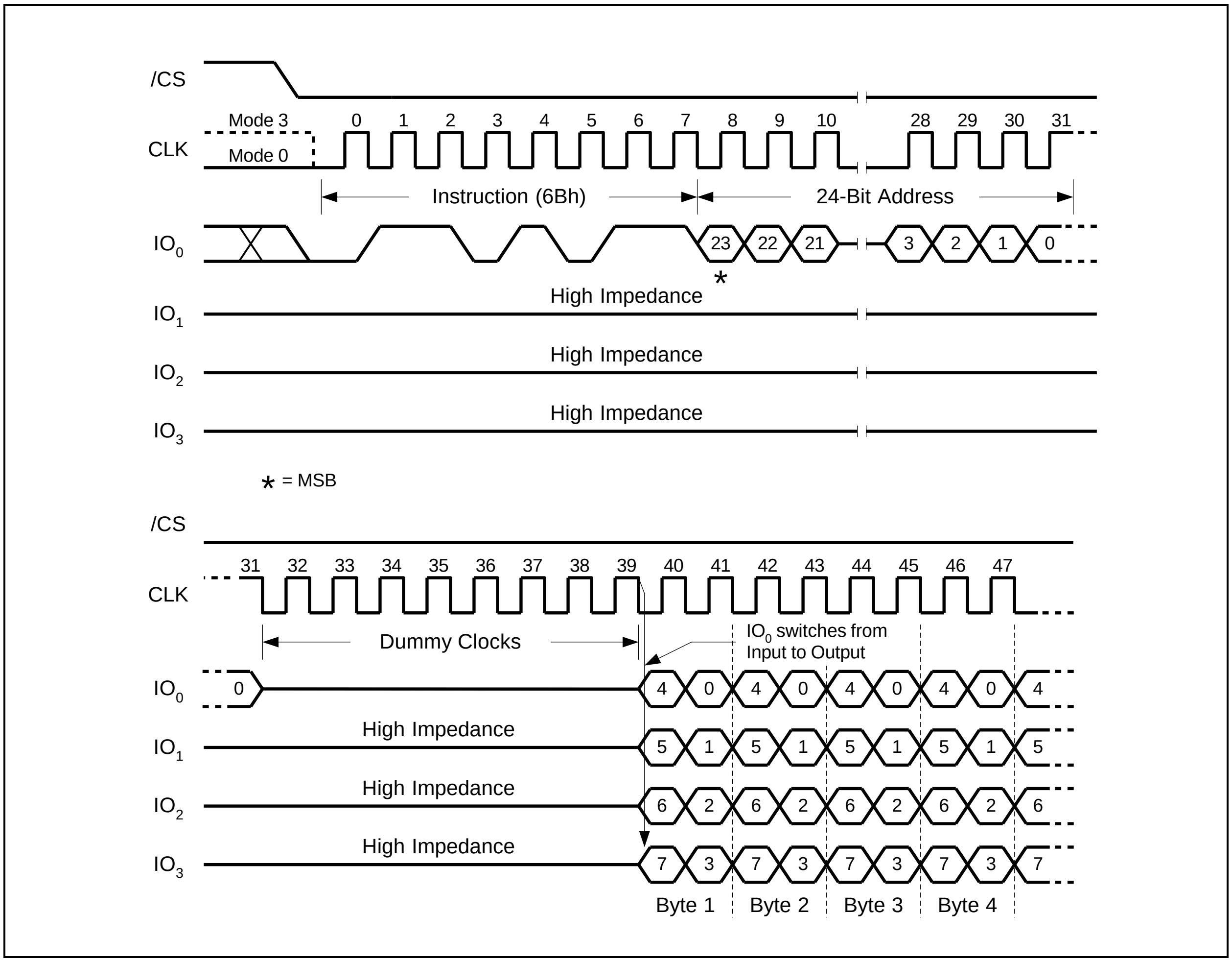



Figure 20. Fast Read Quad Output Instruction

### 8.2.10 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, $IO_0$ and $IO_1$. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

**Fast Read Dual I/O with "Read Instruction Bypass Mode"**

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Read Instruction Bypass Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 22a. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Read Instruction Bypass Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in Figure 22b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Read Instruction Bypass Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on IO0 for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.

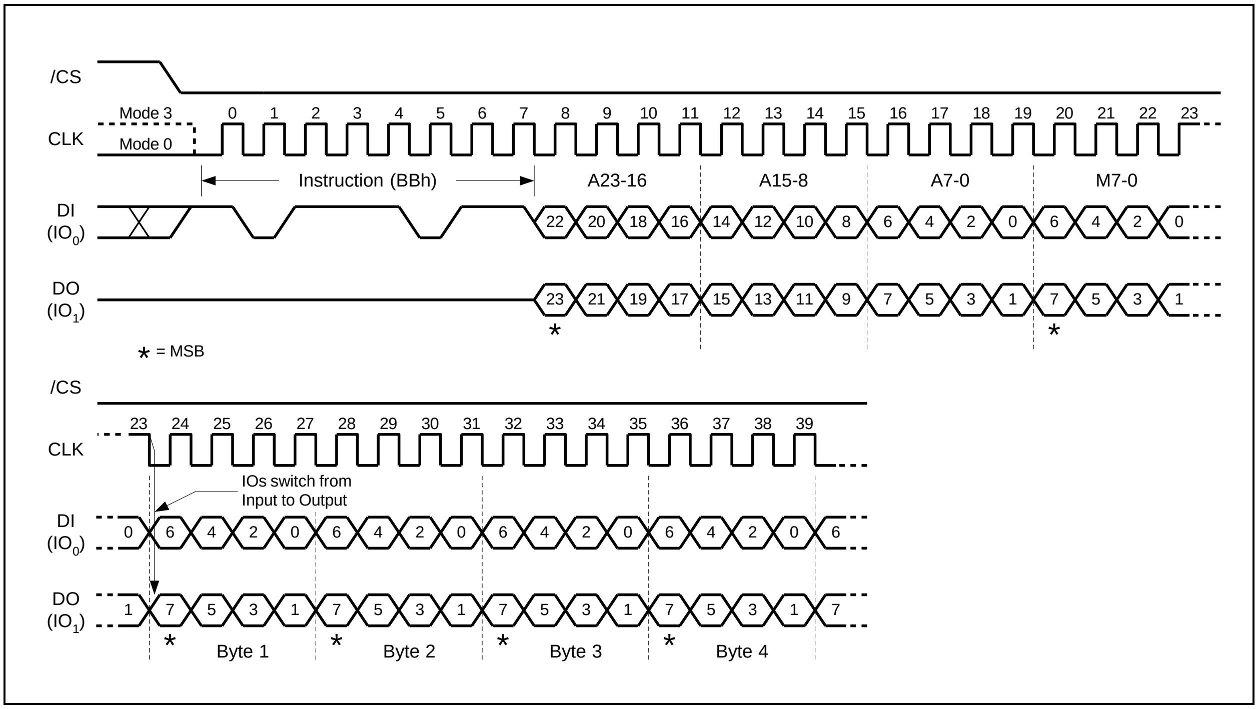



Figure 22a. Fast Read Dual I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

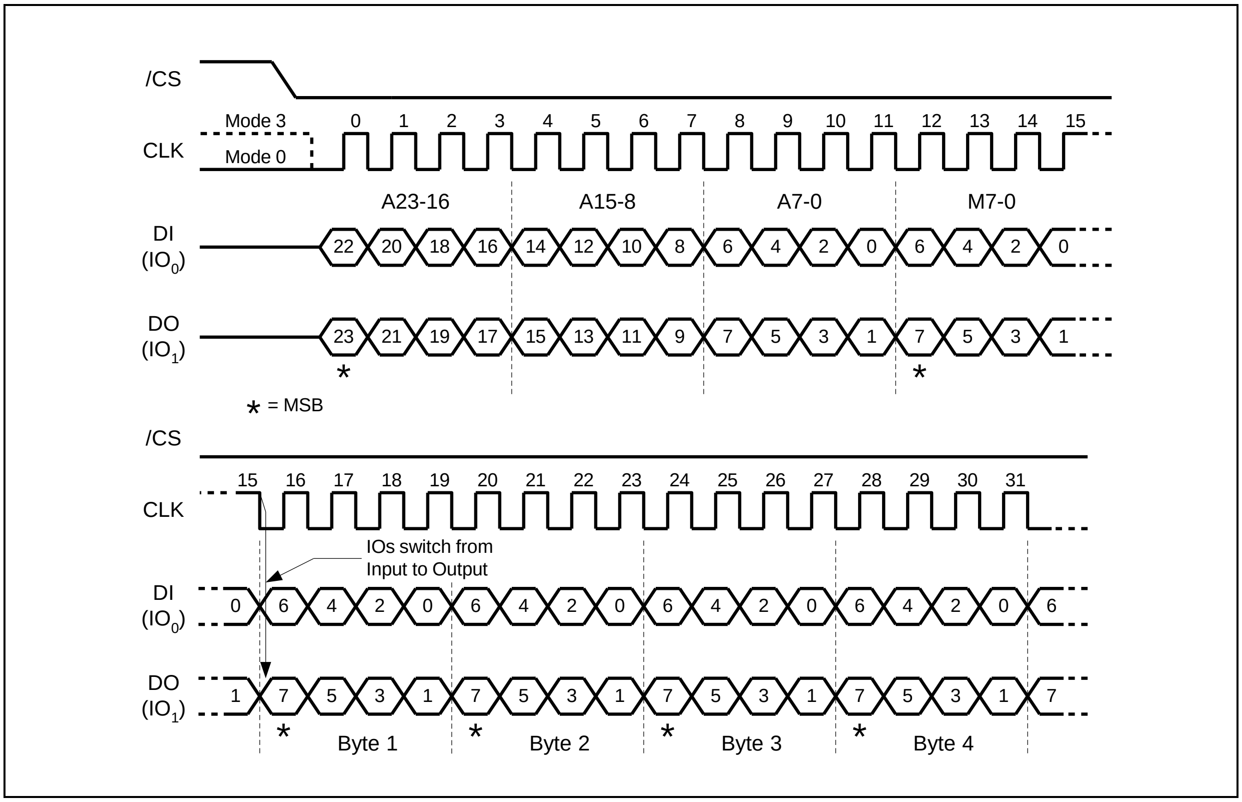



Figure 22b. Fast Read Dual I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)

### 8.2.12 **Fast Read Quad I/O (EBh)**

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins $IO_0$, $IO_1$, $IO_2$ and $IO_3$ and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

**Fast Read Quad I/O with "Read Instruction Bypass Mode"**

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Read Instruction Bypass Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 24a. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Read Instruction Bypass Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure 24b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Read Instruction Bypass Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

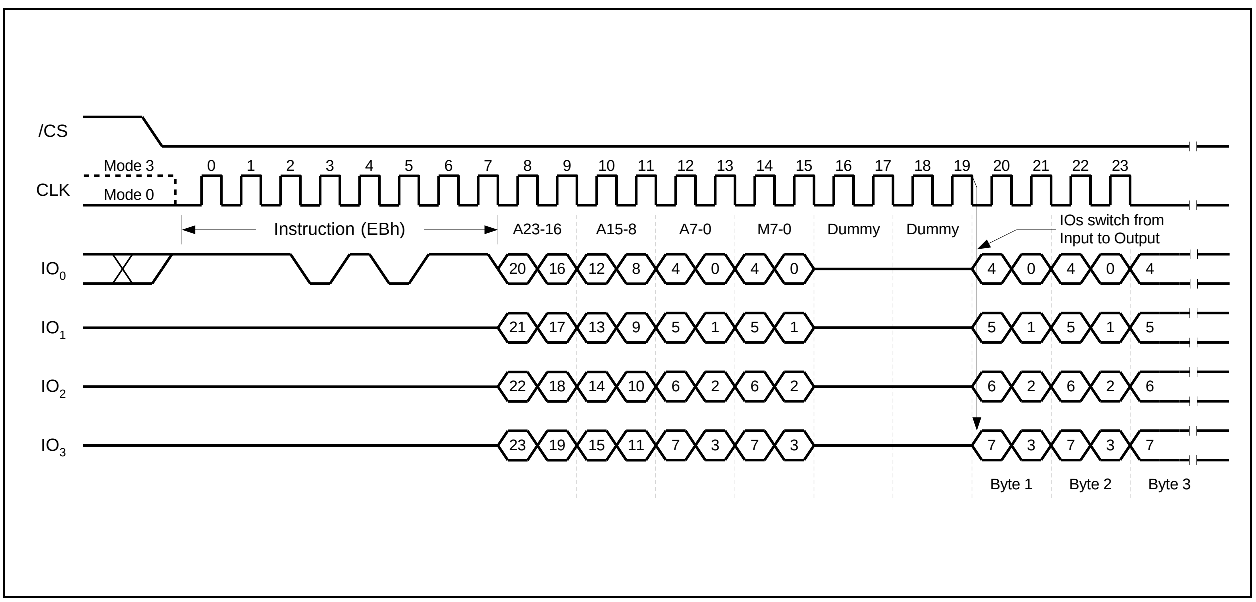



Figure 24a. Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, SPI Mode)

***** "Set Read Parameters" instruction (C0h) can set the number of dummy clocks.

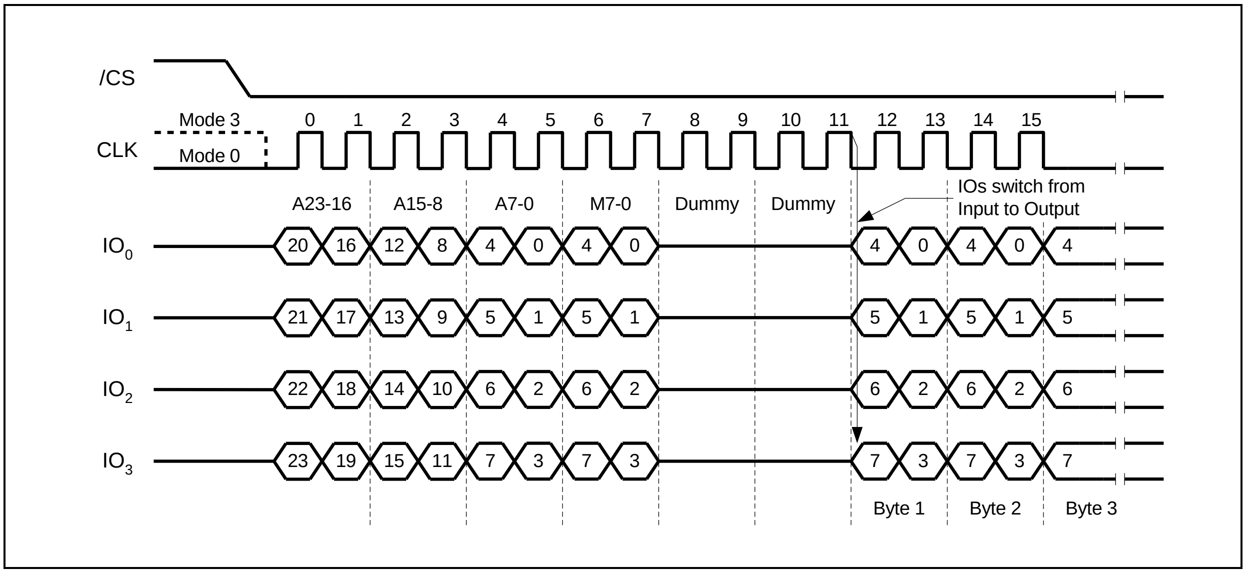



Figure 24b. Fast Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode)

**Fast Read Quad I/O with “8/16/32/64-Byte Wrap Around” in Standard SPI mode**

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a “Set Burst with Wrap” (77h) instruction prior to EBh. The “Set Burst with Wrap” (77h) instruction can either enable or disable the “Wrap Around” feature for the following EBh instructions. When “Wrap Around” is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The “Set Burst with Wrap” instruction allows three “Wrap Bits”, W6-4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to “Set Burst with Wrap (77h)” for detail descriptions.

#### 8.2.13 Set Burst with Wrap (77h)

In Standard SPI mode, the Set Burst with Wrap (77h) instruction is used in conjunction with “Fast Read Quad I/O” instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code “77h” followed by 24 dummy bits and 8 “Wrap Bits”, W7-0. The instruction sequence is shown in Figure 28. Wrap bit W7 and the lower nibble W3-0 are not used.

| W6, W5 | W4 = 0 | | W4 =1 (DEFAULT) | |
|---|---|---|---|---|
| | **Wrap Around** | **Wrap Length** | **Wrap Around** | **Wrap Length** |
| **0 0** | Yes | 8-byte | No | N/A |
| **0 1** | Yes | 16-byte | No | N/A |
| **1 0** | Yes | 32-byte | No | N/A |
| **1 1** | Yes | 64-byte | No | N/A |

Once W6-4 is set by a Set Burst with Wrap instruction, the following “Fast Read Quad I/O” instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on or after a software reset is 1.

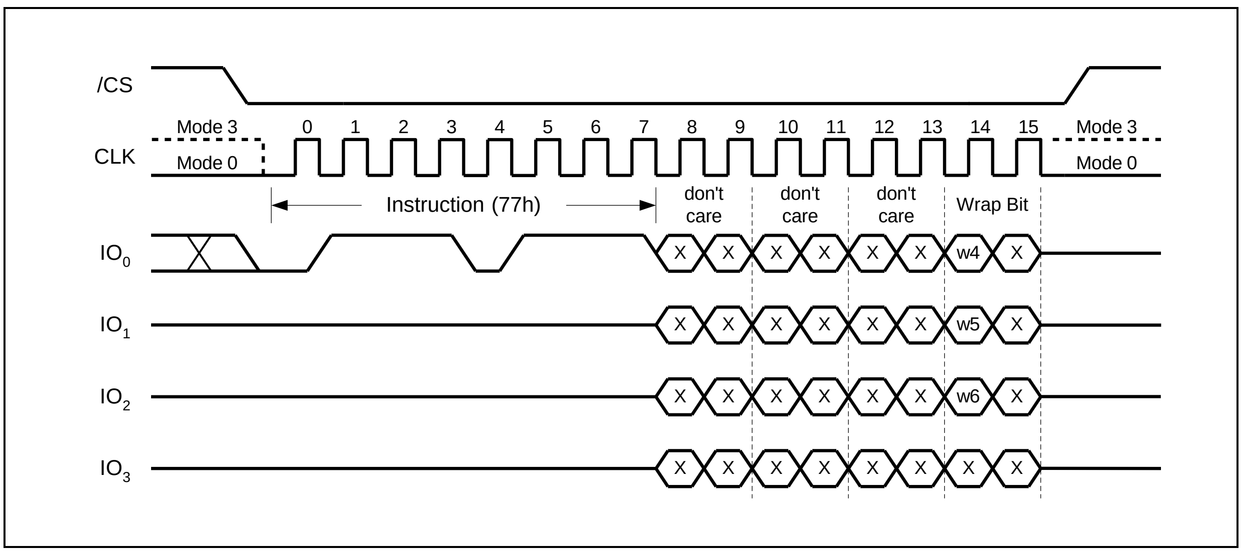



Figure 28. Set Burst with Wrap Instruction

#### 8.2.14 Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 29.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

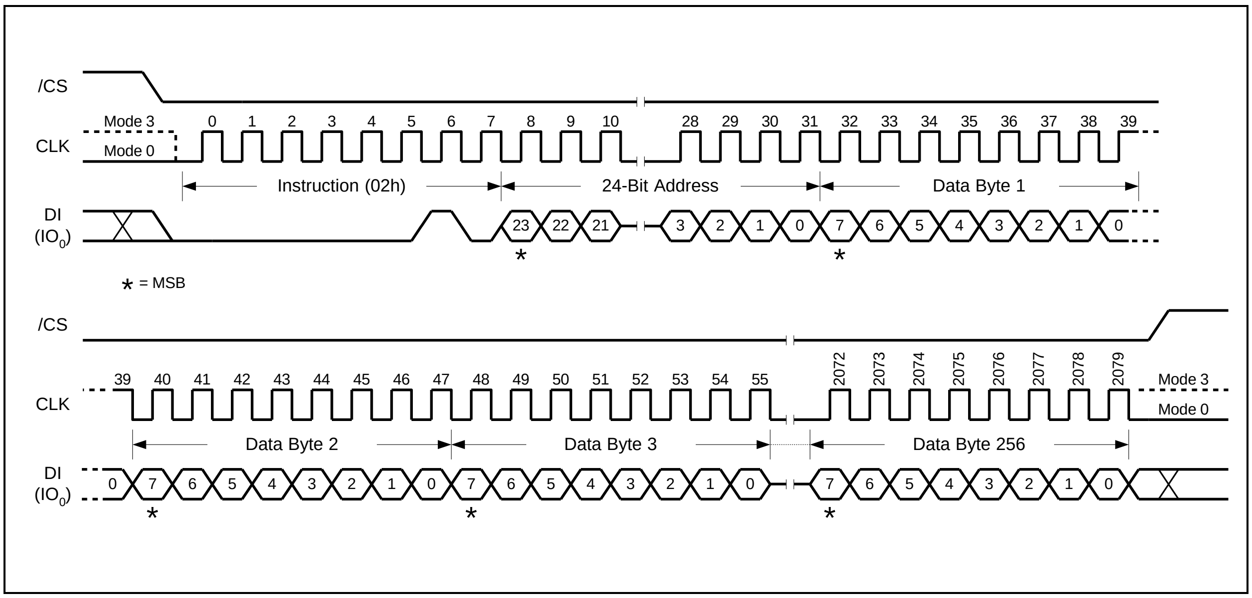



Figure 29a. Page Program Instruction

### 8.2.15 Quad Input Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: $IO_0$, $IO_1$, $IO_2$, and $IO_3$. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable (QE) bit in Status Register-2 must be set to 1. A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code "32h" followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in Figure 30.

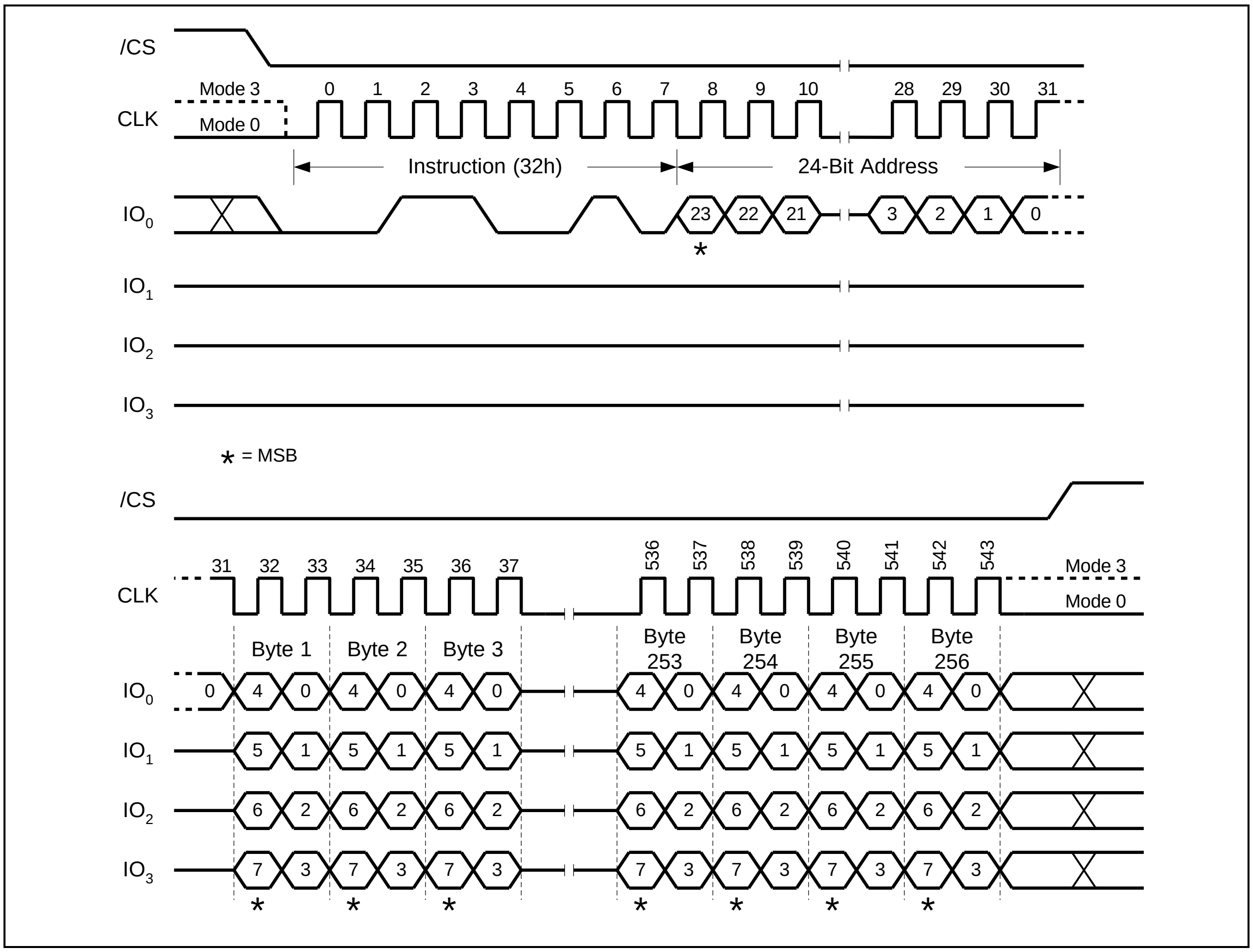



Figure 30. Quad Input Page Program Instruction

#### 8.2.16 Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0). The Sector Erase instruction sequence is shown in Figure 31a & 31b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of tSE (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

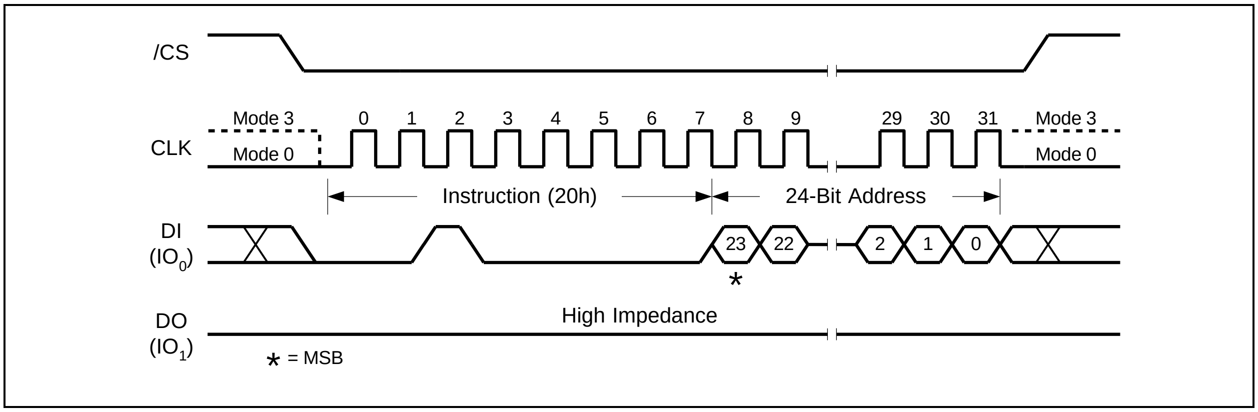



Figure 31a. Sector Erase Instruction

#### 8.2.17 32KB Block Erase (52h)

The Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "52h" followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 32a & 32b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of $t_{BE1}$ (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

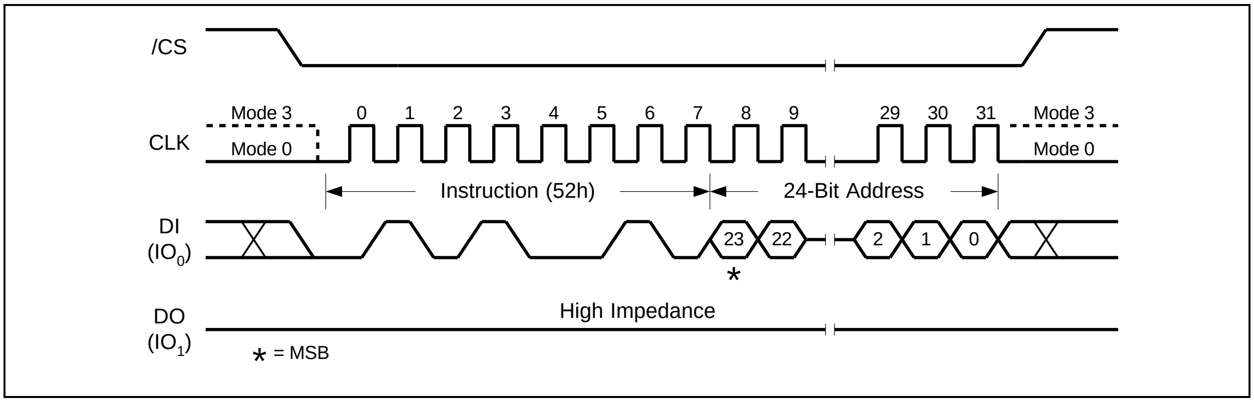



Figure 32a. 32KB Block Erase Instruction

8.2.18 **64KB Block Erase (D8h)**

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 33a & 33b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of $t_{BE}$ (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

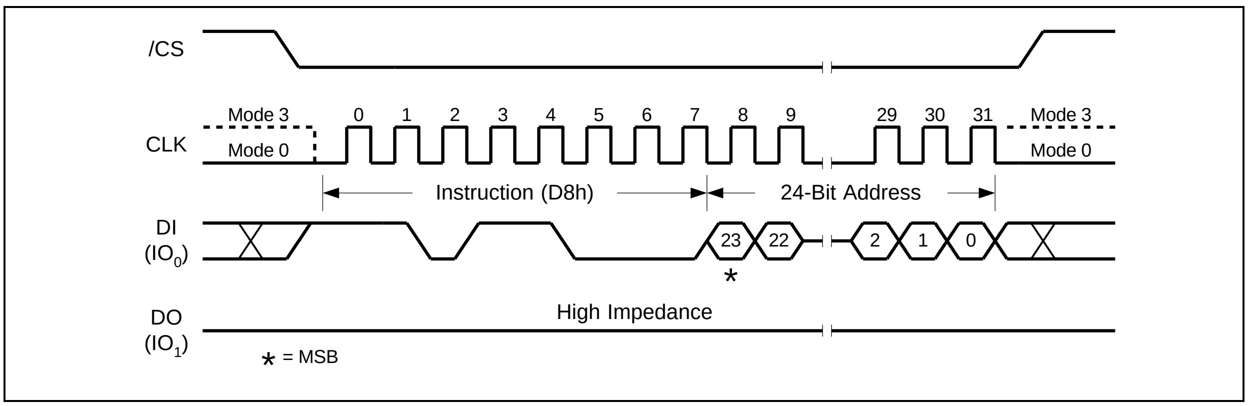



Figure 33a. 64KB Block Erase Instruction

#### 8.2.19 **Chip Erase (C7h / 60h)**

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 34.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of $t_{CE}$ (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any memory region is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

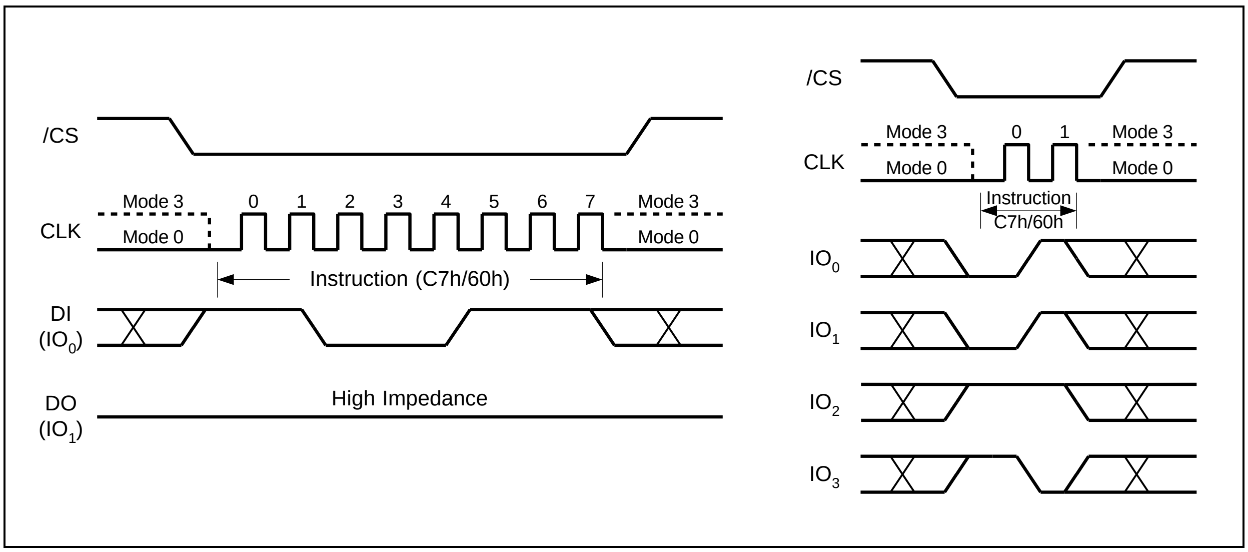



Figure 34. Chip Erase Instruction for SPI Mode

### 8.2.20 Erase / Program Suspend (75h)

The Erase/Program Suspend instruction “75h”, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program/erase data to, any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in Figure 35a & 35b.

The Write Status Register instruction (01h) and Erase instructions (20h, 52h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored. The Write Status Register instruction (01h) and Program instructions (02h, 32h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program or Quad Page Program operation.

The Erase/Program Suspend instruction “75h” will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of “$t_{SUS}$” (See AC Characteristics) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within “$t_{SUS}$” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75h” is not issued earlier than a minimum of time of “$t_{SUS}$” following the preceding Resume instruction “7Ah”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.

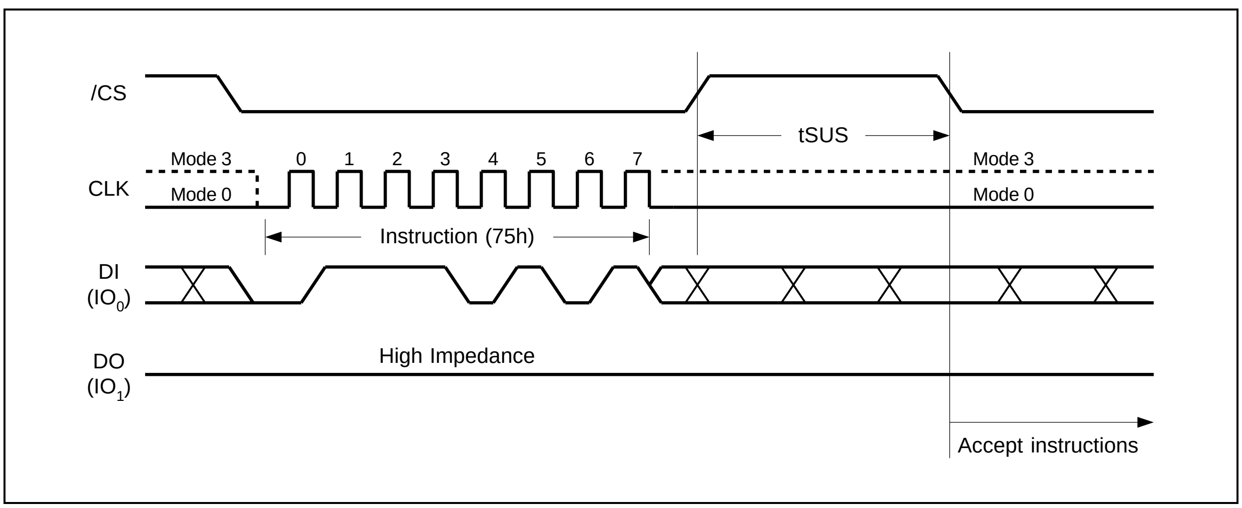



Figure 35a. Erase/Program Suspend Instruction

#### 8.2.21 Erase / Program Resume (7Ah)

The Erase/Program Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 36a & 36b.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of “$t_{SUS}$” following a previous Resume instruction.

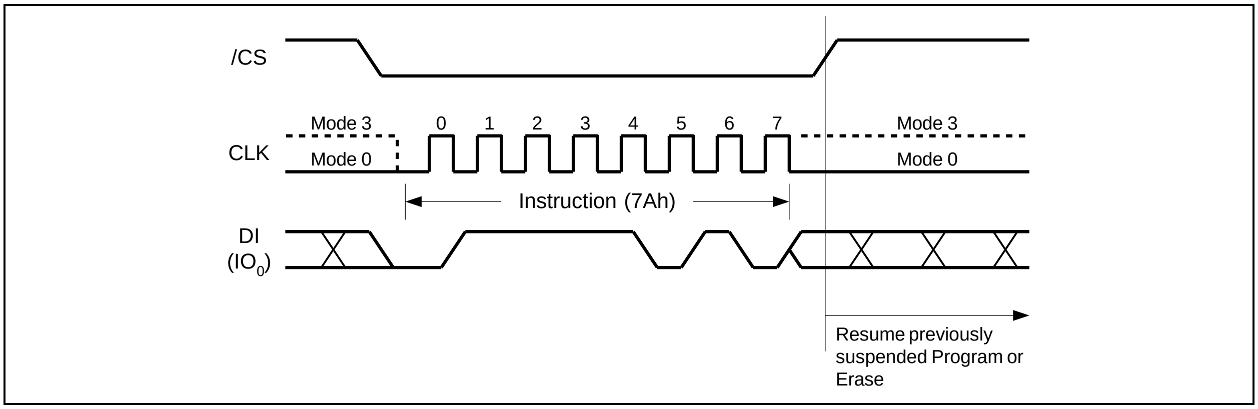



Figure 36a. Erase/Program Resume Instruction

8.2.22 **Power-down (B9h)**

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in Figure 37a & 37b.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of tDP (See AC Characteristics). While in the power-down state only the Release Power-down (ABh), Software Reset(66h/99h) instructions, Hardware Reset and JEDEC Reset which restore the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

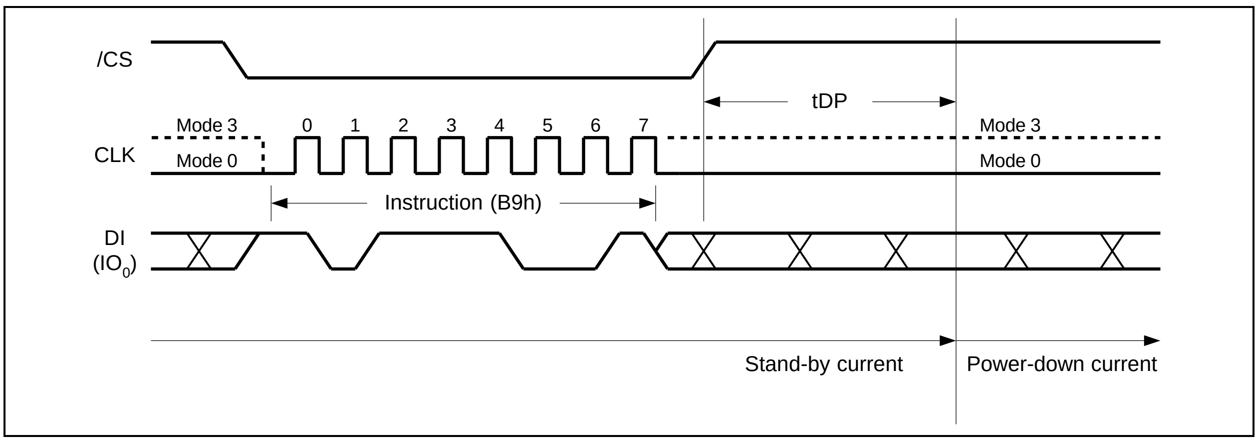



Figure 37a. Deep Power-down Instruction

### 8.2.23 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code "ABh" and driving /CS high as shown in Figure 38a & 38b. Release from power-down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code "ABh" followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first. The Device ID value for the W25Q33PW is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

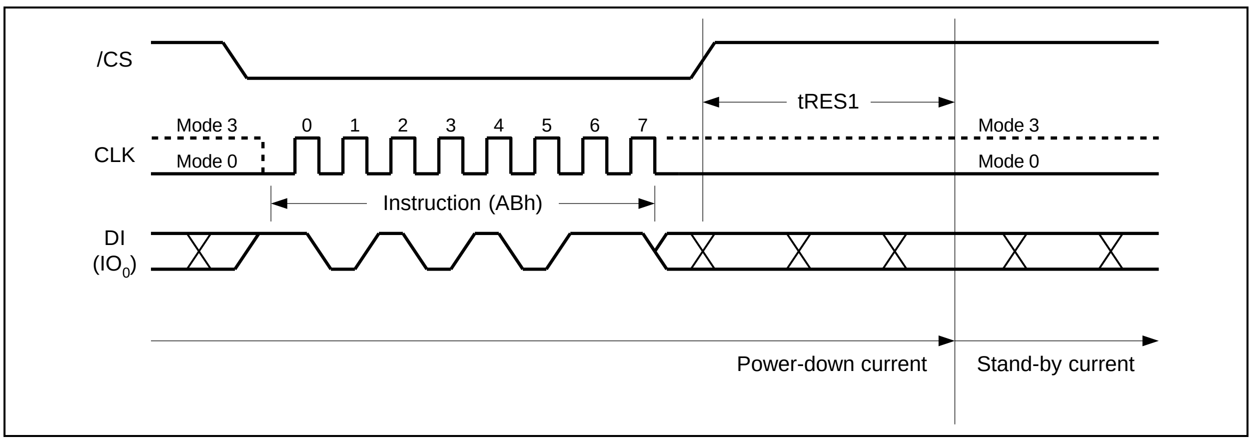



Figure 38a. Release Power-down Instruction

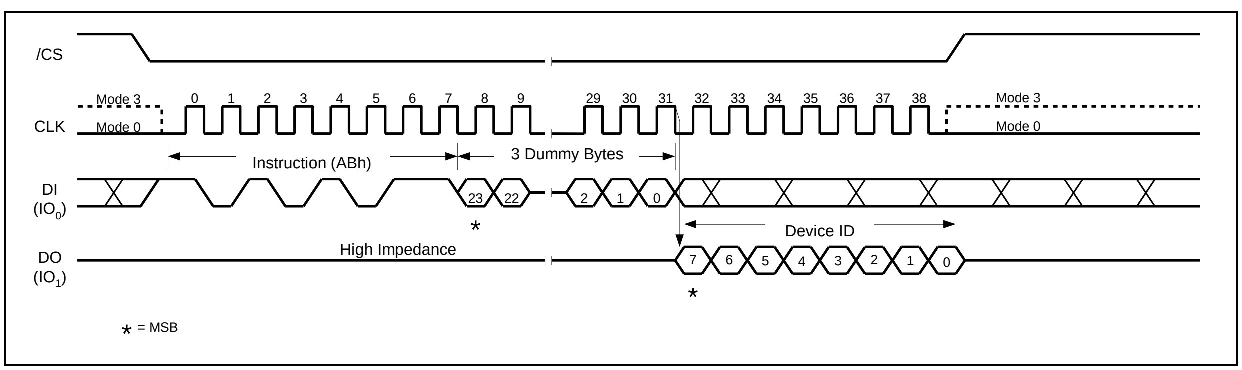



Figure 38c. Device ID Instruction

8.2.24 **Read Manufacturer / Device ID (90h)**

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 39. The Device ID values for the W25Q33PW are listed in Manufacturer and Device Identification table. The instruction is completed by driving /CS high.

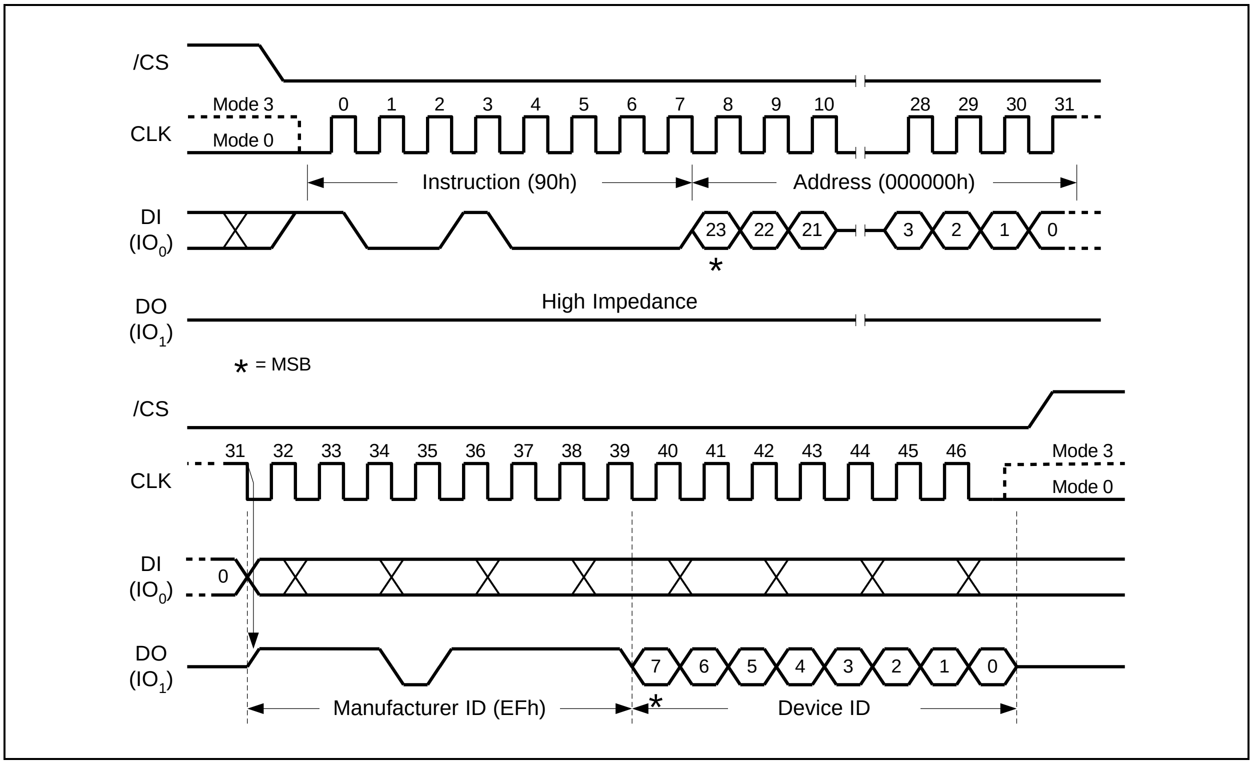



Figure 39. Read Manufacturer / Device ID Instruction

## 8.2.25 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "92h" followed by a 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in Figure 40. The Device ID values for the W25Q33PW are listed in Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

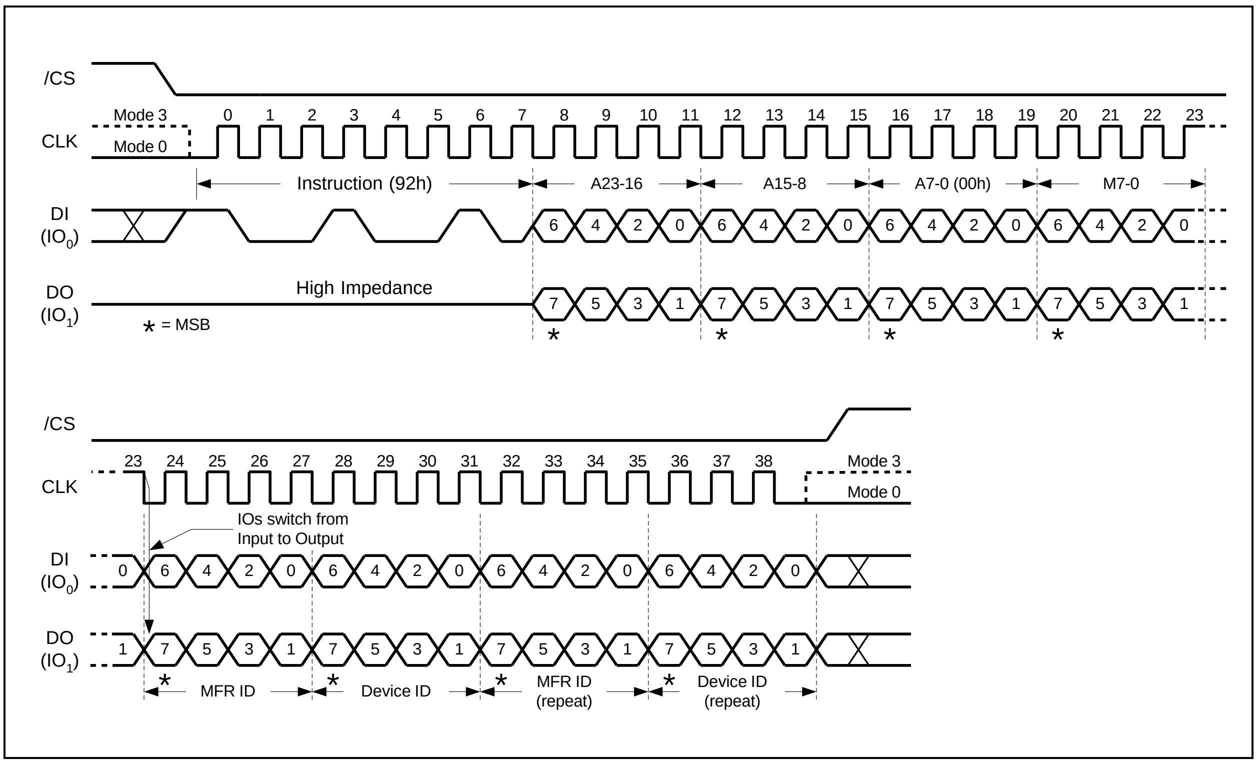



Figure 40. Read Manufacturer / Device ID Dual I/O Instruction

Note:
The "Read Instruction Bypass Mode" bits M(7-0) must be set to Fxh to be compatible with Fast Read Dual I/O instruction.

### 8.2.26 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "94h" followed by a four clock dummy cycles and then a 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 41. The Device ID values for the W25Q33PW are listed in Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

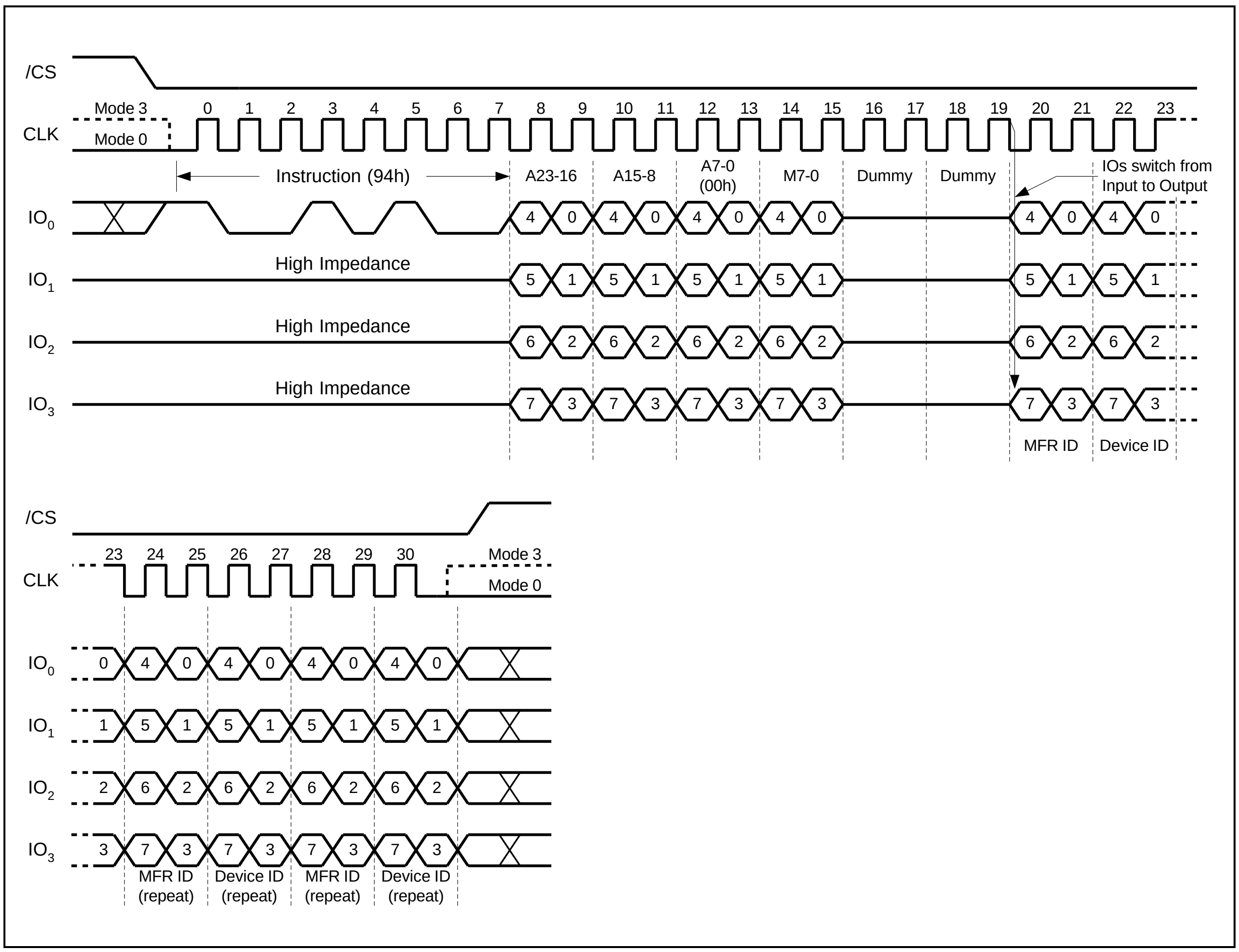



Figure 41. Read Manufacturer / Device ID Quad I/O Instruction

Note:
The "Read Instruction Bypass Mode" bits M(7-0) must be set to Fxh to be compatible with Fast Read Quad I/O instruction.

8.2.27 **Read Unique ID Number (4Bh)**

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each W25Q33PW device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by a four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in Figure 42.

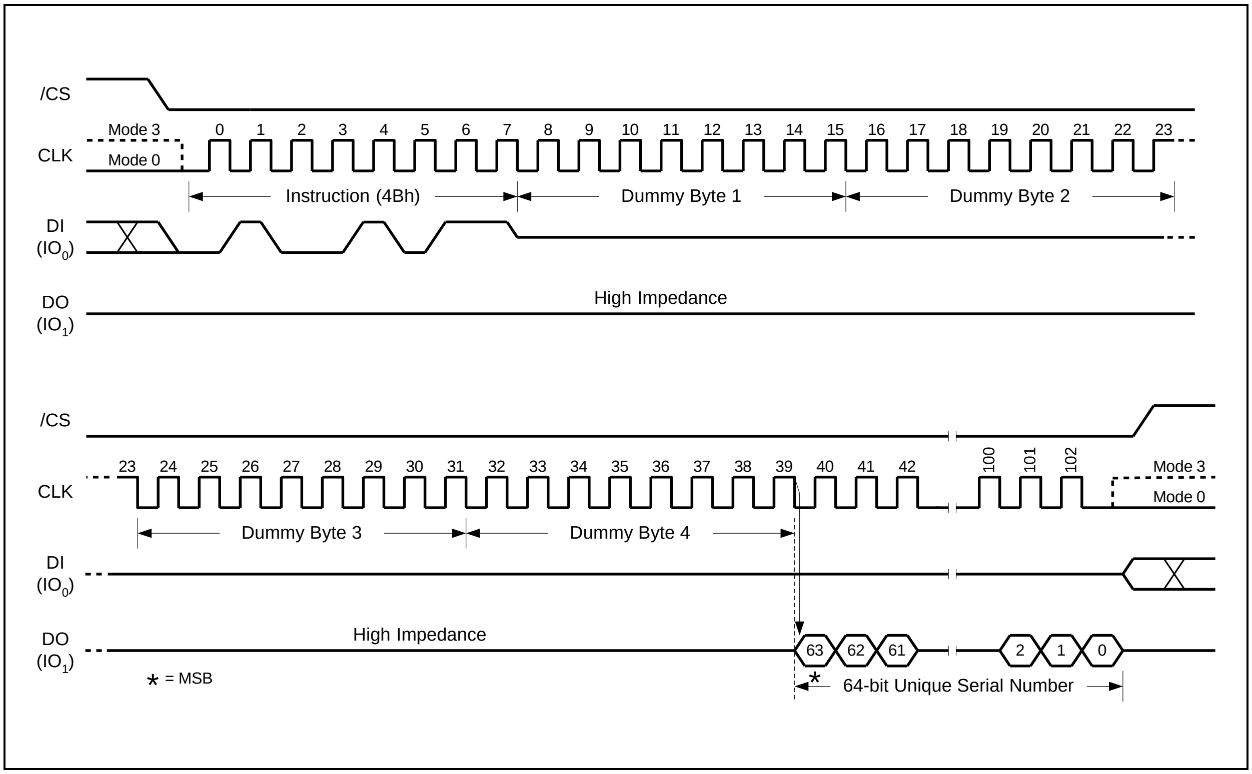



Figure 42. Read Unique ID Number Instruction

8.2.28 **Read JEDEC ID (9Fh)**

For compatibility reasons, the W25Q33PW provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 43a & 43b. For memory type and capacity values refer to Manufacturer and Device Identification table.

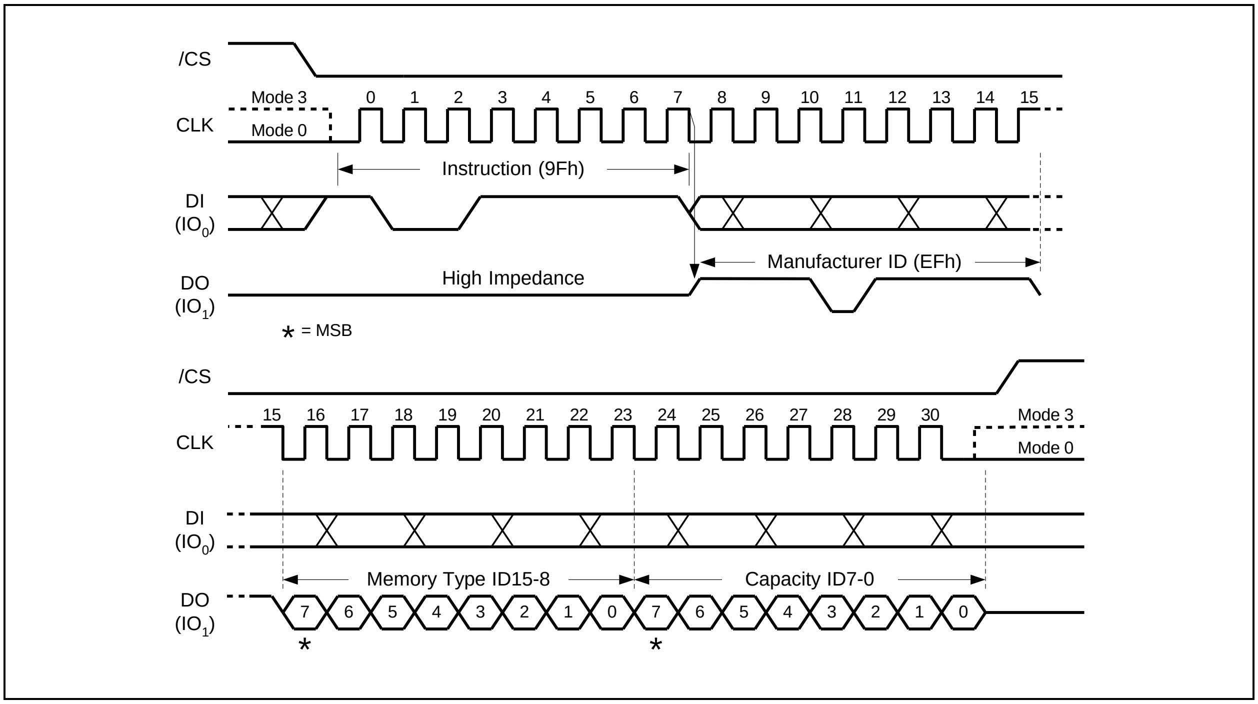



Figure 43a. Read JEDEC ID Instruction

### 8.2.29 Read SFDP Register (5Ah)

The W25Q33PW features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified, but more may be added in the future. The Read SFDP Register instruction is compatible with the SFDP standard initially established in 2010 for PC and other applications, as well as the JEDEC standard JESD216 that is published in 2011. Most Winbond SpiFlash Memories shipped after June 2011 (date code 1124 and beyond) support the SFDP feature as specified in the applicable datasheet.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code "5Ah" followed by a 24-bit address (A23-A0)(1) into the DI pin. Eight "dummy" clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in Figure 44. For SFDP register values and descriptions, please refer to the Winbond Application Note for SFDP Definition Table.

Note 1: A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

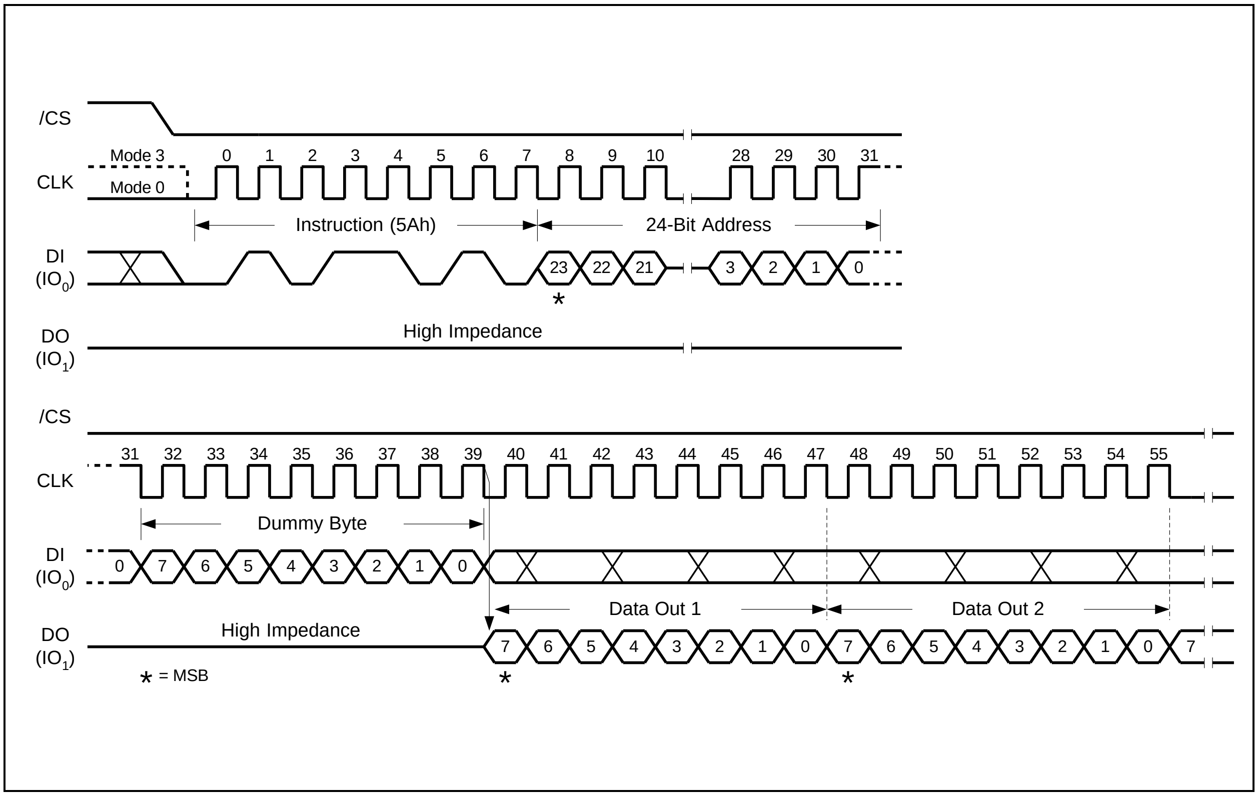



Figure 44. Read SFDP Register Instruction Sequence Diagram

### 8.2.30 Erase Security Registers (44h)

The W25Q33PW offers three 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "44h" followed by a 24-bit address (A23-A0) to erase one of the three security registers.

| ADDRESS | A23-16 | A15-12 | A11-8 | A7-0 |
|---|---|---|---|---|
| Security Register #1 | 00h | 0 0 0 1 | 0 0 0 0 | Don't Care |
| Security Register #2 | 00h | 0 0 1 0 | 0 0 0 0 | Don't Care |
| Security Register #3 | 00h | 0 0 1 1 | 0 0 0 0 | Don't Care |

The Erase Security Register instruction sequence is shown in Figure 45. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation will commence for a time duration of $t_{SE}$ (See AC Characteristics). While the Erase Security Register cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Erase Security Register instruction to that register will be ignored (Refer to "Security Register Lock Bits" for detail descriptions).

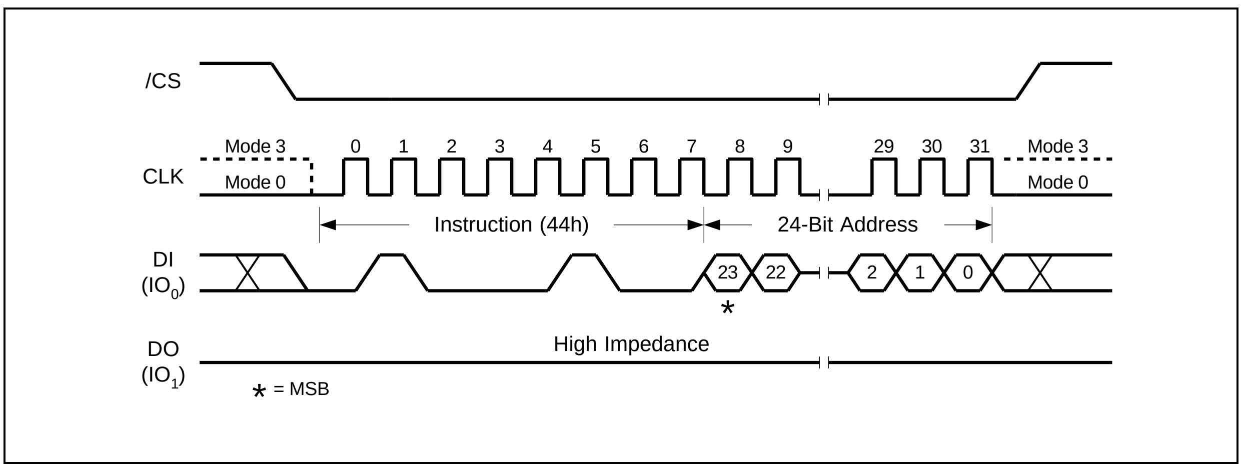



Figure 45. Erase Security Registers Instruction

### 8.2.31 Program Security Registers (42h)

The Program Security Register instruction is similar to the Page Program instruction. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Register Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code "42h" followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

| ADDRESS | A23-16 | A15-12 | A11-8 | A7-0 |
|---|---|---|---|---|
| Security Register #1 | 00h | 0 0 0 1 | 0 0 0 0 | Byte Address |
| Security Register #2 | 00h | 0 0 1 0 | 0 0 0 0 | Byte Address |
| Security Register #3 | 00h | 0 0 1 1 | 0 0 0 0 | Byte Address |

The Program Security Register instruction sequence is shown in Figure 46. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Program Security Register instruction to that register will be ignored (See Security Register Lock Bits" for detail descriptions).

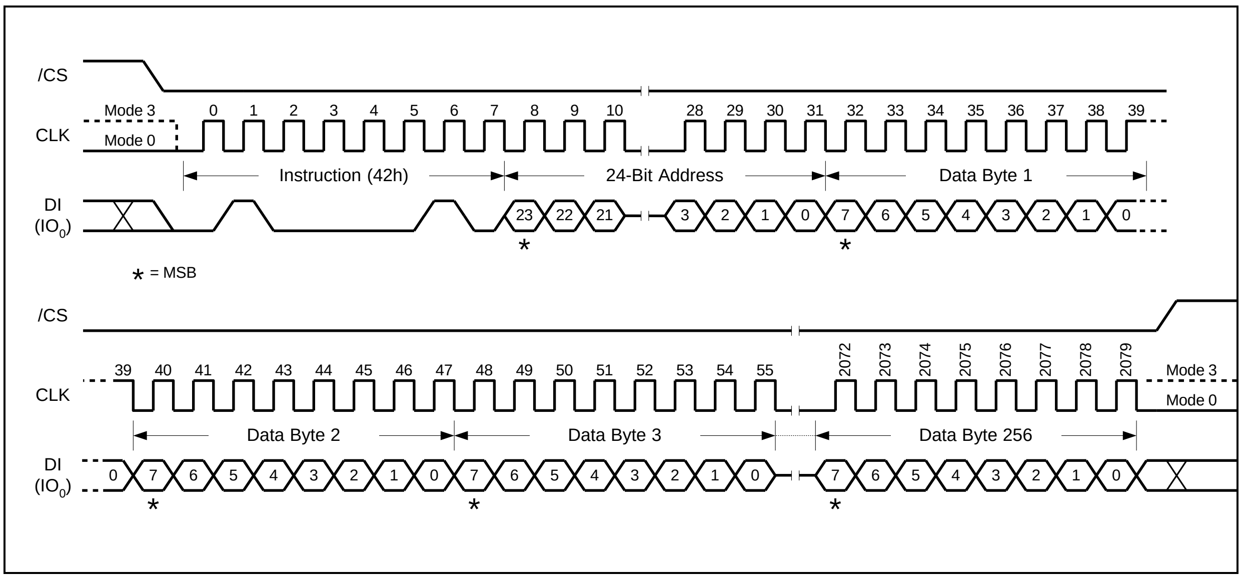



Figure 46. Program Security Registers Instruction

### 8.2.32 Read Security Registers (48h)

The Read Security Register instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from one of the four security registers. The instruction is initiated by driving the /CS pin low and then shifting the instruction code "48h" followed by a 24-bit address (A23-A0) and eight "dummy" clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte address FFh), it will reset to address 00h, the first byte of the register, and continue to increment. The instruction is completed by driving /CS high. The Read Security Register instruction sequence is shown in Figure 47. If a Read Security Register instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Security Register instruction allows clock rates from D.C. to a maximum of $F_R$ (see AC Electrical Characteristics).

| ADDRESS | A23-16 | A15-12 | A11-8 | A7-0 |
|---|---|---|---|---|
| Security Register #1 | 00h | 0 0 0 1 | 0 0 0 0 | Byte Address |
| Security Register #2 | 00h | 0 0 1 0 | 0 0 0 0 | Byte Address |
| Security Register #3 | 00h | 0 0 1 1 | 0 0 0 0 | Byte Address |

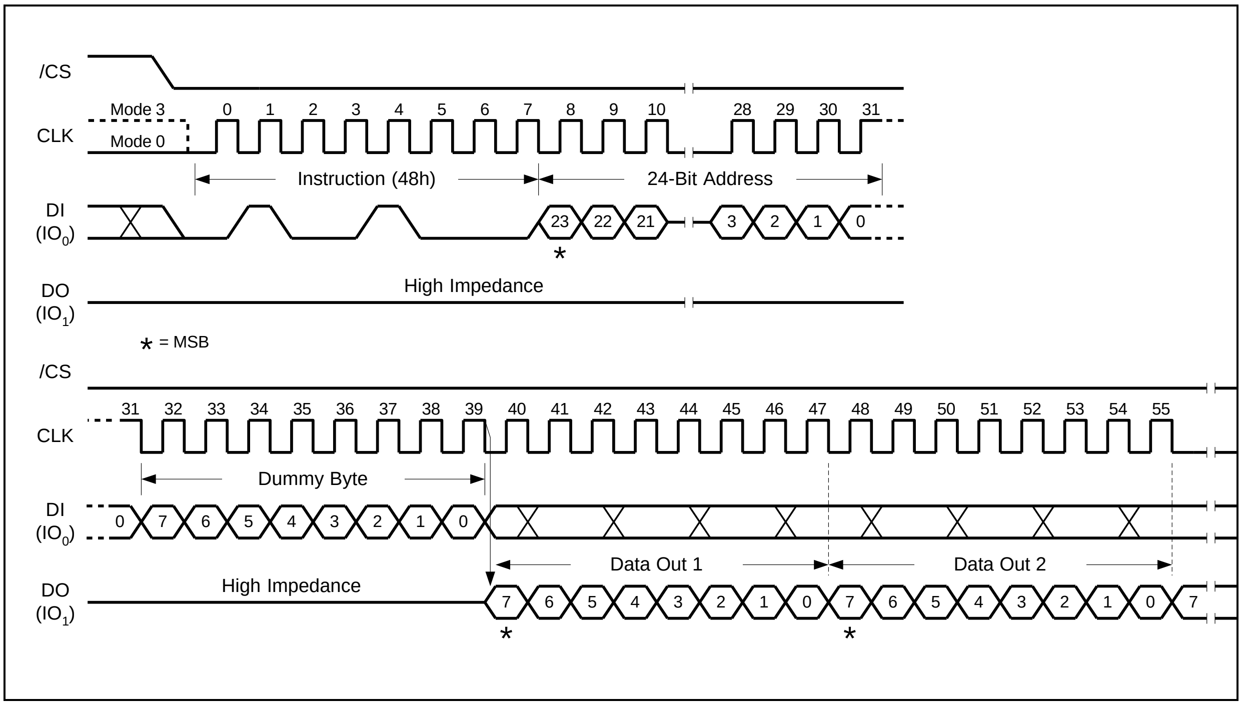



Figure 47. Read Security Registers Instruction

### 8.2.34 Set Read Parameters (C0h)

“Set Read Parameters (C0h)” instruction is used to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency. This is accomplished by setting the number of dummy clocks and wrap length configurations for set of selected instructions. Set Read Parameters (C0h) instruction writes to the Read Parameter Register (P[7:0]).

In SPI mode, SPI Set Read Parameters (C0h)" instruction writes to ‘Dummy Clocks’ P[6:4] bits only, while it will ignore P[1:0] bits input as they are don’t care in SPI mode. The Set Read Parameters instruction sequence is shown in Figure 36.

The dummy clocks for various Fast Read instructions in Standard/Dual/Quad SPI mode are fixed, except for ”Fast Read Quad I/O (EBh)”. Please refer to the Instruction Tables 2 or details. “Wrap Length” for the SPI ”Fast Read Quad I/O (EBh)” instruction is set by W6-4 bit with the “Set Burst with Wrap (77h)” instruction.

The default Parameter Read “Dummy Clocks” and “Wrap Length“ settings for selected SPI instruction after power up or reset are defined on the tables below. After power up or reset, Read Parameter bits are reset to 000h. Detailed Read Parameter bits configuration are also shown below.

| P6 – P4 | Dummy Clocks (SPI: EBh) | MAX. READ FREQ.[(1)] |
|---|---|---|
| 0 0 0 | 6(Default) | 104MHz |
| 0 0 1 | 6 | 104MHz |
| 0 1 0 | 6 | 104MHz |
| 0 1 1 | 8 | 133MHz |
| 1 0 0 | 10 | 133MHz |
| 1 0 1 | 12 | 133MHz |
| 1 1 0 | 14 | 133MHz |
| 1 1 1 | 16 | 166MHz |

**Notes**:
1. Required address alignment and start address for Reads: LSB A[1:0]=00b

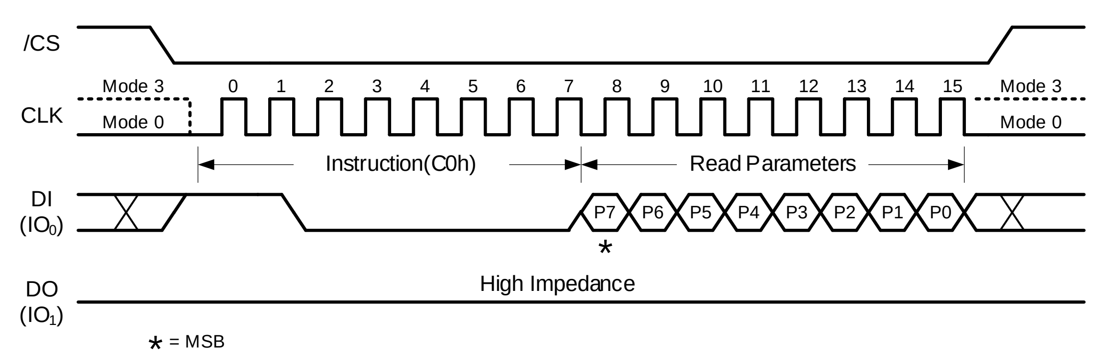



Figure 48a. Set Read Parameters Instruction

* SPI Set Read Parameters(C0h) instruction writes to “Dummy Clock” P[6:4] bit only. It will ignore Warp Length P[0:1] bits input was they are don’t care in SPI mode.

### 8.2.35 Enable Reset (66h) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the W25Q33PW provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Read parameter setting (P7-P0), Read Instruction Bypass Mode bit setting (M7-M0) and Wrap Bit setting (W6-W4).

"Enable Reset (66h)" and "Reset (99h)" instructions can be issued in either SPI mode. To avoid accidental reset, both instructions must be issued in sequence. Any other instructions other than "Reset (99h)" after the "Enable Reset (66h)" instruction will disable the "Reset Enable" state. A new sequence of "Enable Reset (66h)" and "Reset (99h)" is needed to reset the device. Once the Reset instruction is accepted by the device, the device will take approximately tRST=30us to reset. During this period, no instruction will be accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset instruction sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset instruction sequence.

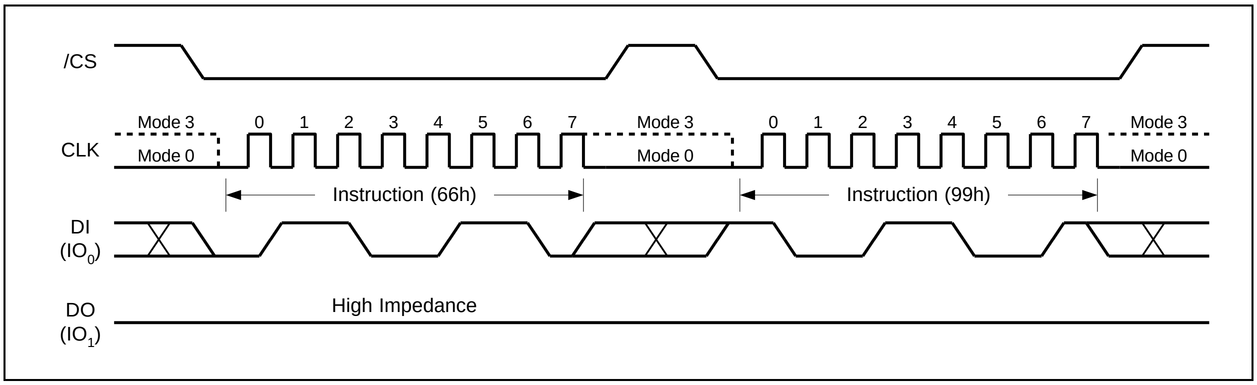



Figure 53a. Enable Reset and Reset Instruction Sequence

#### 8.2.36 Clear Buffer(81h)

The Clear Buffer instruction allows all data in the buffer to be written as "1". A Write Enable instruction is not required and the instruction is initiated by driving the /CS pin low and then shifting the instruction code "81h" and a 24-bit address (A23-A0) to the DI pin. The /CS pin must be held low while instruction and address are transferred to the device. Then by driving /CS pin high, clearing the buffer with all "1". The Clear Buffer instruction sequence is shown in Figure 54a.
After Release Power-down(ABh), a clear buffer command must be issued.”

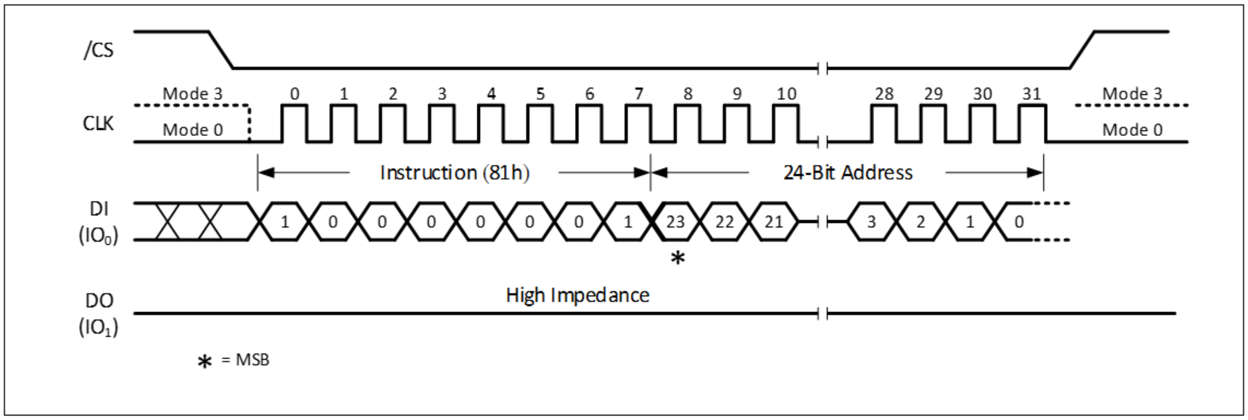



Figure 54a. Clear Buffer

### 8.2.37 **Write Buffer(82h)**

The Write Buffer instruction allows to write from 1 byte to 256 bytes of data to the buffer. A Write Enable instruction is not required, and the instruction is initiated by driving the /CS pin low and then shifting the instruction code "82h" followed by a 24-bit address (A23-A0) and at least one data byte to the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being transferred to the device. The Write Buffer instruction sequence is shown in Figure 54b.

To write the entire 256-byte buffer, the last address byte (the 8 least significant address bits) must be set to 0. The first 16 most significant address bits can be any address. If the last address byte is not zero, and the number of clocks exceeds the remaining buffer length, the addressing is wrapped to the beginning of the buffer. In some cases, less than 256 bytes (partial buffer) can be written without affecting other bytes within the buffer. One condition for performing a partial-buffer write is that the number of clocks cannot exceed the remaining buffer length. If more than 256 bytes are sent to the device, the addressing is wrapped to the beginning of the buffer, overwriting previously sent data.

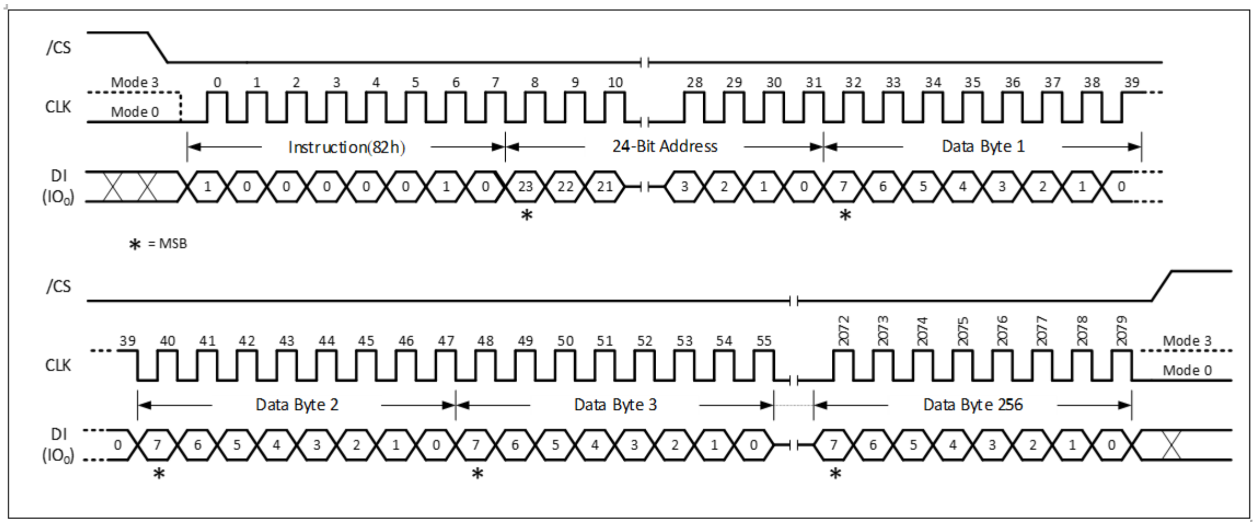



Figure 54b. Write Buffer

### 8.2.38 Read Buffer(83h)

The Read Buffer instruction allows one or more data bytes to be sequentially read from the buffer. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “83h” followed by a 24-bit address (A23-A0) and an 8-bit dummy into the DI pin. The code and address bits are latched on the rising edge of CLK. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with the most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire buffer can be accessed with a single instruction as long as clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in Figure 54c. If a Read Buffer instruction is issued while an Erase, Program or Write cycle is in progress (BUSY=1), the instruction is ignored and will not have any effects on the current cycle. The Read Buffer instruction allows clock rates from D.C. to a maximum of fR (see AC Electrical Characteristics).

The Read Buffer (83h) instruction is only supported in Standard SPI mode.

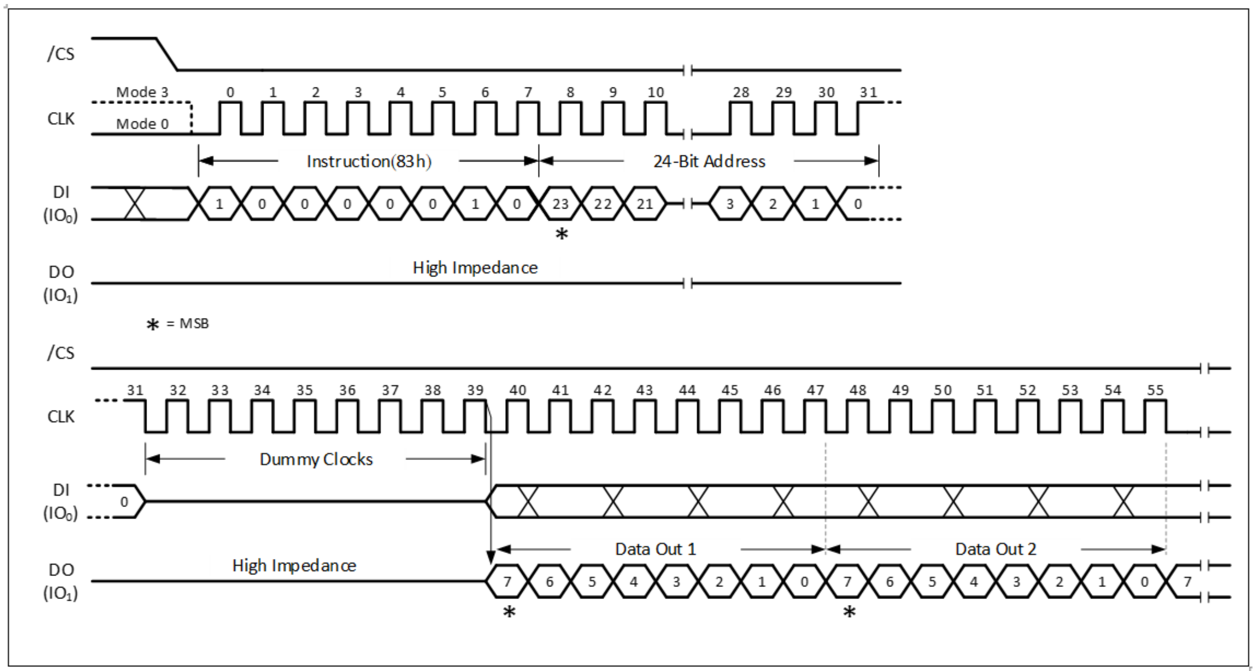



Figure 54c. Read Buffer

### 8.2.39 **Program Buffer(8Ah)**

The program buffer instruction will program the buffer content into the physical memory page that is specified in the instruction. A Write Enable instruction must be executed before the device will accept the Program Buffer instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “8Ah” followed by a 24-bit address (A23-A0) into the DI pin as shown in Figure 54d.

After /CS is driven high to complete the instruction cycle, the self-timed Program Buffer instruction will commence for a time duration of tPP (See AC Characteristics). While the Program Buffer cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit.

The BUSY bit is a 1 during the Program Buffer cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Program Buffer cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Program Execute instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP2, BP1, and BP0) bits.

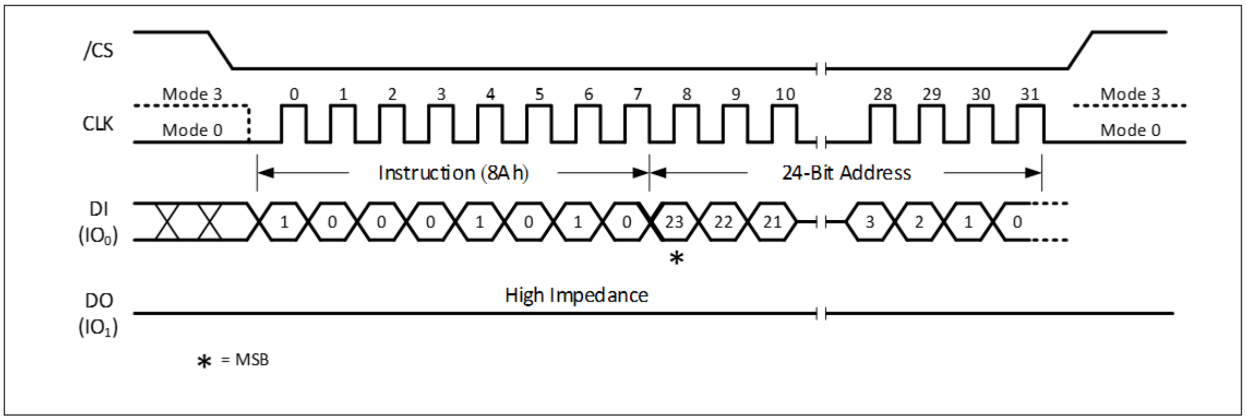



Figure 54d. Program Buffer

8.2.40 **Load Buffer(8Bh)**

The Load Buffer instruction will write the contents of the physical memory page specified in the instruction to the buffer. A Write Enable instruction is not required, and the instruction is initiated by driving the /CS pin low then shifting the instruction code "8Bh" followed by a 24-bit address (A23-A0), and then driving /CS high as shown in Figure 54e.

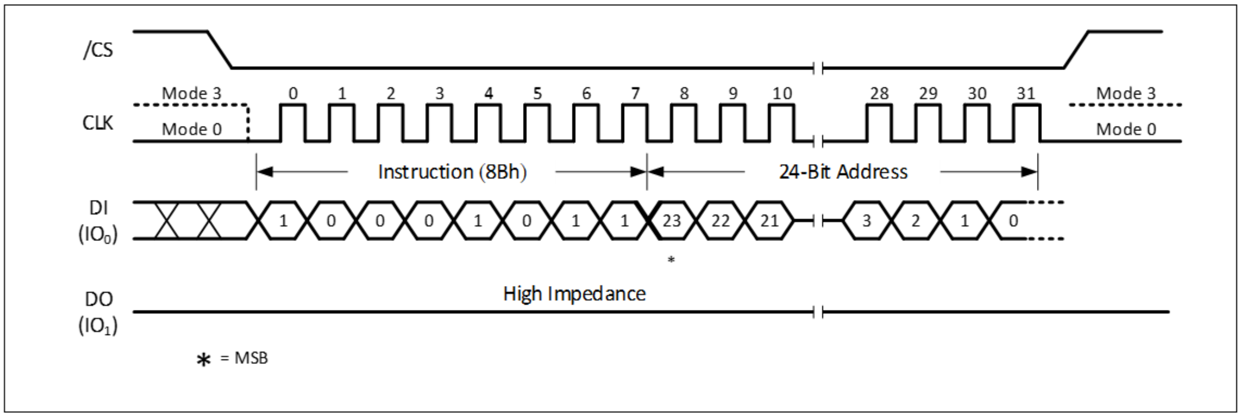



Figure 54e. Load Buffer

# 9. ELECTRICAL CHARACTERISTICS

## 9.1 Absolute Maximum Ratings [1]

| PARAMETERS | SYMBOL | CONDITIONS | RANGE | UNIT |
|---|---|---|---|---|
| Supply Voltage | VCC | | –0.6 to 2.5 | V |
| Voltage Applied to Any Pin | $V_{IO}$ | Respect to VSS | –0.6 to VIO+0.4 | V |
| Transient Voltage on any Pin | $V_{IOT}$ | <20nS Transient Respect to VSS | –2.0V to VIO+2.0V | V |
| Storage Temperature | $T_{STG}$ | | –65 to +150 | °C |
| Lead Temperature | $T_{LEAD}$ | | See Note [2] | °C |
| Electrostatic Discharge Voltage | $V_{ESD}$ | Human Body Model[3] | –2000 to +2000 | V |

**Notes:**

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

## 9.2 Operating Ranges

| PARAMETER | SYMBOL | CONDITIONS | SPEC | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| Supply Voltage[1] | VCC | $F_R$ = 166MHz $f_R$ = 84MHz | 1.65 | 1.95 | V |
| Ambient Temperature, Operating | $T_A$ | Industrial | –40 | +85 | °C |

**Note:**

1. VCC voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.

## 9.3 Power-Up Power-Down Timing and Requirements

| PARAMETER | SYMBOL | SPEC | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| VCC (min) to /CS Low | tVSL[(1)] | 20 | | µs |
| Time Delay Before Write Instruction | tPUW[(1)] | 5 | | ms |
| Write Inhibit Threshold Voltage | $V_{WI}$[(1)] | 1.0 | 1.4 | V |
| The minimum duration for ensuring initialization will occur | tPWD[(1)] | 100 | | µs |
| VCC voltage needed to below $V_{PWD}$ for ensuring initialization will occur | $V_{PWD}$[(1)] | | 0.8 | V |

**Note:**

1. These parameters are characterized only.

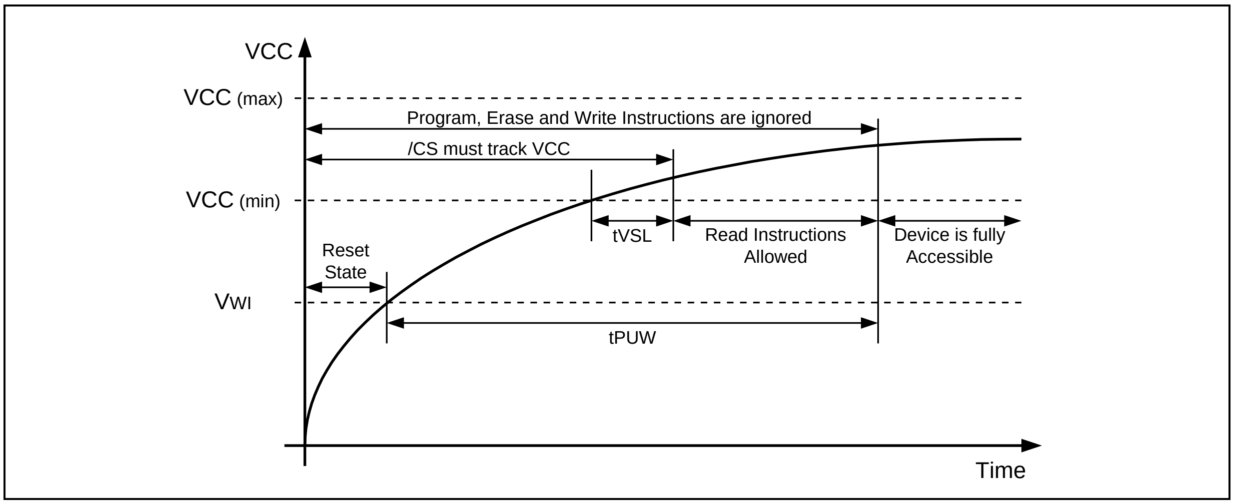



Figure 58a. Power-up Timing and Voltage Levels

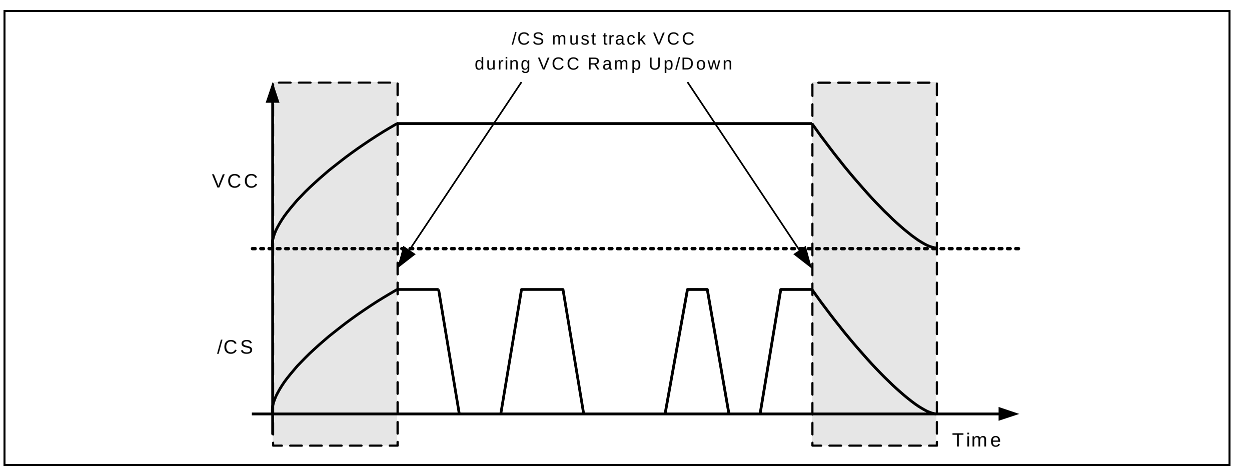



Figure 58b. Power-up, Power-Down Requirement

### 9.3.1 Power Cycle Requirement

For power cycle, the system must not initial the power-up sequence until Vcc drops down to $V_{PWD}$ and keeps a $t_{PWD}$ for device to initialize correctly.

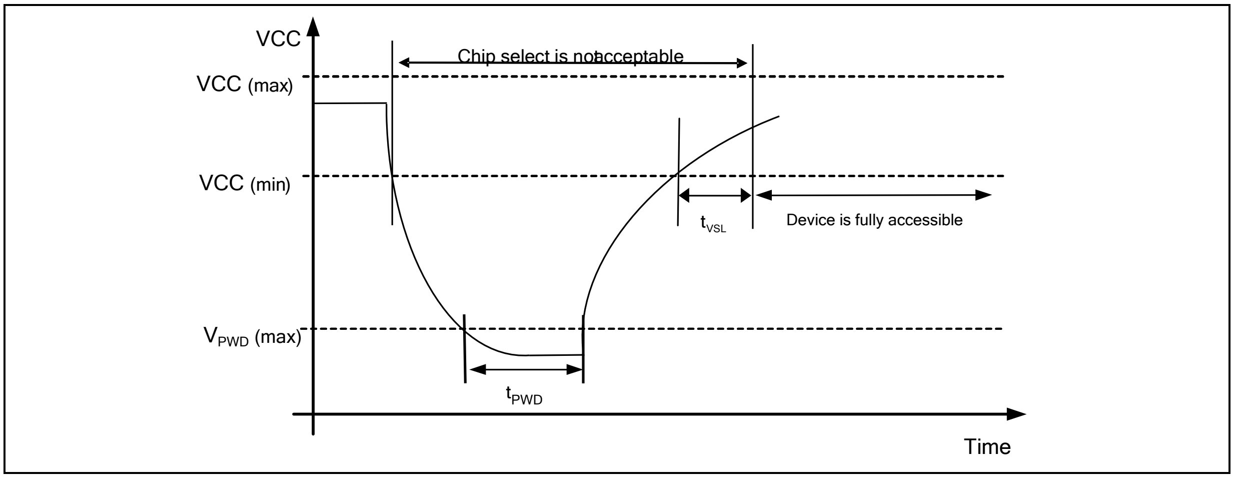



Figure 58c. Power Cycle Requirement

## 9.4 DC Electrical Characteristics-

| PARAMETER | SYMBOL | CONDITIONS | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Input Capacitance | CIN(1) | VIN = 0V | | | 6 | pF |
| Output Capacitance | Cout(1) | VOUT = 0V | | | 8 | pF |
| Input Leakage | ILI | | | | ±2 | µA |
| I/O Leakage | ILO | | | | ±2 | µA |
| Standby Current | ICC1 | /CS = VCC, VIN = VSS or VCC | | 5 | 10 | µA |
| Power-down Current | ICC2 | /CS = VCC, VIN = VSS or VCC | | 0.1 | 5 | µA |
| Read Data / Dual /Quad 50MHz Current | ICC3 | C = 0.1 VCC / 0.9 VCC DO = Open | | 3 | 5 | mA |
| Read Data / Dual Output / Quad Output Read 84MHz Current | Icc3 | C = 0.1 VCC / 0.9 VCC DO = Open | | 4 | 6 | mA |
| Read Data / Dual Output / Quad Output Read 104MHz Current | Icc3 | C = 0.1 VCC / 0.9 VCC DO = Open | | 5 | 8 | mA |
| Read Data / Dual Output / Quad Output Read 133MHz Current | Icc3 | C = 0.1 VCC / 0.9 VCC DO = Open | | 7 | 12 | mA |
| Quad Output Read 166MHz Current | Icc3 | C = 0.1 VCC / 0.9 VCC DO = Open | | 8 | 14 | mA |
| Write Status Register Current | Icc4 | /CS = VCC | | 8 | 15 | mA |
| Page Program Current | Icc5(2) | /CS = VCC | | 8 | 15 | mA |
| Sector/Block Erase Current | Icc6 | /CS = VCC | | 8 | 15 | mA |
| Chip Erase Current | Icc7 | /CS = VCC | | 8 | 15 | mA |
| Input Low Voltage | Vil | | -0.5 | | VCC x 0.3 | V |
| Input High Voltage | Vih | | VCC x 0.7 | | | V |
| Output Low Voltage | Vol | Iol = 100 µA | | | 0.2 | V |
| Output High Voltage | Voh | Ioh = –100 µA | VCC – 0.2 | | | V |

**Notes:**

1. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 1.8V.
2. Checker Board Pattern.

## 9.5 AC Measurement Conditions

| PARAMETER | SYMBOL | SPEC | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Load Capacitance | $C_L$ | | 30 | pF |
| Input Rise and Fall Times | $T_R$, $T_F$ | | 5 | ns |
| Input Pulse Voltages | $V_{IN}$ | 0.1 VCC to 0.9 VCC | | V |
| Input Timing Reference Voltages | IN | 0.3 VCC to 0.7 VCC | | V |
| Output Timing Reference Voltages | OUT | 0.5 VCC to 0.5 VCC | | V |

**Note:**

1. Output Hi-Z is defined as the point where data out is no longer driven.

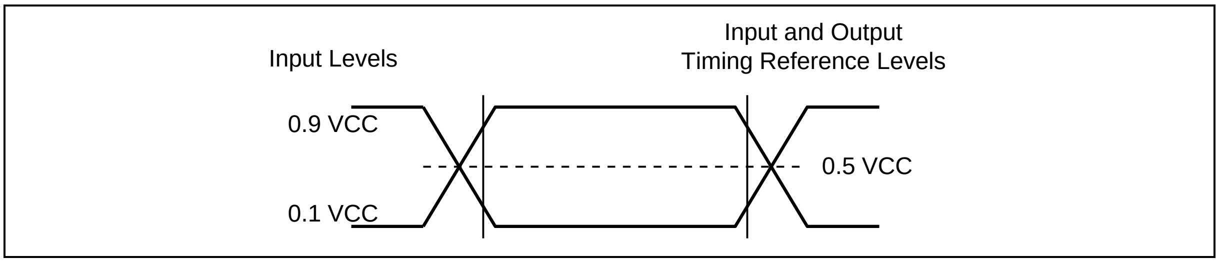



Figure 59. AC Measurement I/O Waveform

## 9.6 AC Electrical Characteristics

| DESCRIPTION | SYMBOL | ALT | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Clock frequency for Read Data with EBh-16 dummy(6) | $F_R$ | $f_{C1}$ | D.C. | | 166(5) | MHz |
| Clock frequency for Read Data with EBh-6 dummy(6) | $F_R$ | $f_{C1}$ | D.C. | | 104(5) | MHz |
| Clock frequency except for Read Data (03h) | $F_R$ | $f_{C1}$ | D.C. | | 133(5) | MHz |
| Clock frequency for Read Data instruction (03h) | $f_R$ | | D.C. | | 84(5) | MHz |
| Clock High, Low Time for all instructions except for Read Data (03h) | $t_{CLH}$, $t_{CLL}$(1) | | 45%PC | | | ns |
| Clock High, Low Time for Read Data (03h) instruction | $t_{CRLH}$, $t_{CRLL}$(1) | | 45%PC | | | ns |
| Clock Rise Time peak to peak | $t_{CLCH}$(2) | | 0.1 | | | V/ns |
| Clock Fall Time peak to peak | $t_{CHCL}$(2) | | 0.1 | | | V/ns |
| /CS Active Setup Time relative to CLK | $t_{SLCH}$ | $t_{CSS}$ | 5 | | | ns |
| /CS Not Active Hold Time relative to CLK | $t_{CHSL}$ | | 3 | | | ns |
| Data In Setup Time | $t_{DVCH}$ | $t_{DSU}$ | 2 | | | ns |
| Data In Hold Time | $t_{CHDX}$ | $t_{DH}$ | 2 | | | ns |
| /CS Active Hold Time relative to CLK | $t_{CHSH}$ | | 3 | | | ns |
| /CS Not Active Setup Time relative to CLK | $t_{SHCH}$ | | 3 | | | ns |
| /CS Deselect Time (for Read) | $t_{SHSL1}$ | $t_{CSH}$ | 10 | | | ns |
| /CS Deselect Time (for Erase or Program or Write) | $t_{SHSL2}$ | $t_{CSH}$ | 50 | | | ns |
| Output Disable Time | $t_{SHQZ}$(2) | $t_{DIS}$ | | | 7 | ns |
| Clock Low to Output Valid | $t_{CLQV}$ | $t_V$ | | | 4.5 | ns |
| Output Hold Time | $t_{CLQX}$ | $t_{HO}$ | 1 | | | ns |

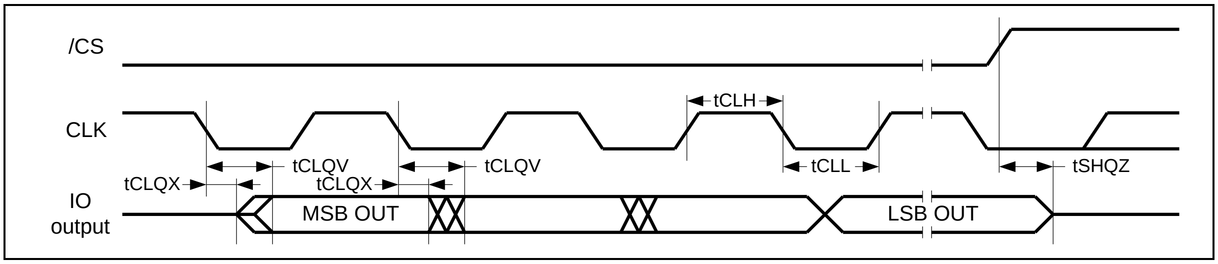
Continued – next page

| DESCRIPTION | SYMBOL | ALT | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Write Protect Setup Time Before /CS Low | $t_{WHSL}$(3) | | 20 | | | ns |
| Write Protect Hold Time After /CS High | $t_{SHWL}$(3) | | 100 | | | ns |
| /CS High to Power-down Mode | $t_{DP}$(2) | | | | 3 | µs |
| /CS High to Standby Mode without ID Read | $t_{RES1}$(2) | | | | 10 | µs |
| /CS High to next Instruction after Suspend | $t_{SUS}$(2) | | | | 20 | µs |
| /CS High to next Instruction after Reset | $t_{RST}$(2) | | | | 30 | µs |
| /RESET pin Low period to reset the device | $t_{RESET}$(2) | | 1(5) | | | µs |
| /CS Low for JEDEC Reset Signaling | $t_{CSL}$ | | 500 | | | nS |
| /CS High for JEDEC Reset Signaling | $t_{CSH}$ | | 500 | | | nS |
| Setup Time for JEDEC Reset Signaling | $t_S$ | | 5 | | | nS |
| Hold Time for JEDEC Reset Signaling | $t_D$ | | 5 | | | nS |
| Internal Reset Time for JEDEC Reset Signaling | $t_{RST2}$ | | | | 100 | mS |
| Write Status Register Time | $t_W$ | | | 2 | 15 | ms |
| Page Program Time | $t_{PP}$ | | | 0.25 | 1.2 | ms |
| Sector Erase Time (4KB) | $t_{SE}$ | | | 30 | 400 | ms |
| Block Erase Time (32KB) | $t_{BE1}$ | | | 100 | 800 | ms |
| Block Erase Time (64KB) | $t_{BE2}$ | | | 120 | 1000 | ms |
| Chip Erase Time | $t_{CE}$ | | | 12 | 40 | s |

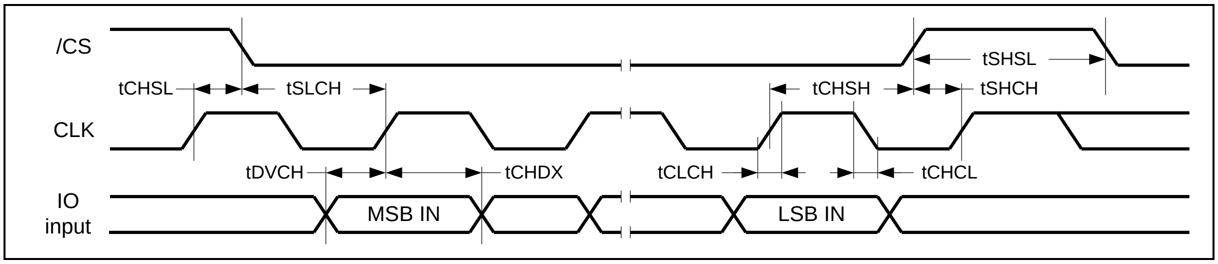
**Notes:**

1. Clock high or Clock low must be more than or equal to 45%Pc. Pc=1/$fC_{(MAX)}$.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when SRP=1.
4. It's possible to reset the device with shorter $t_{RESET}$ (as short as a few hundred ns), a 1us minimum is recommended to ensure reliable operation.
5. Typ value tested on sample basis and specified through design and characterization data. $T_A$ = 25° C, VCC = 1.8V, 50-ohm driver strength.
6. For details, please refer to "Set Read Parameters (C0h)".

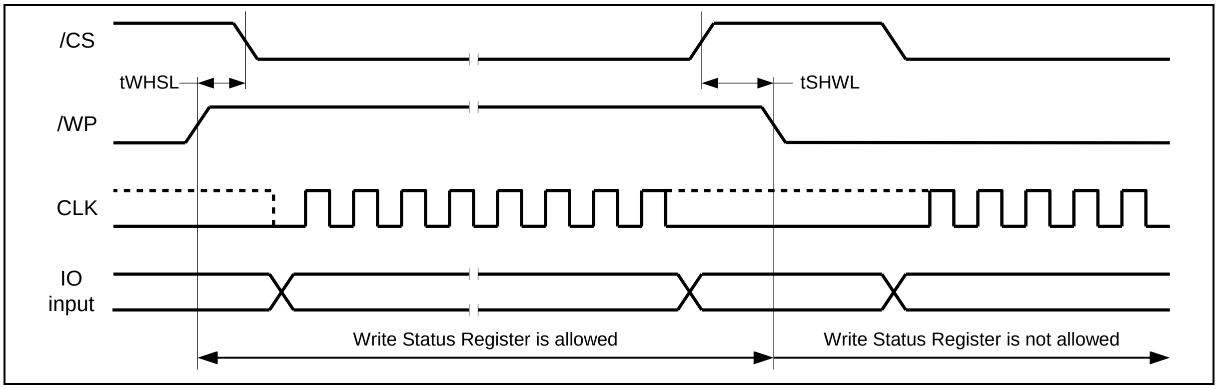
## 9.7 Serial Output Timing




## 9.8 Serial Input Timing

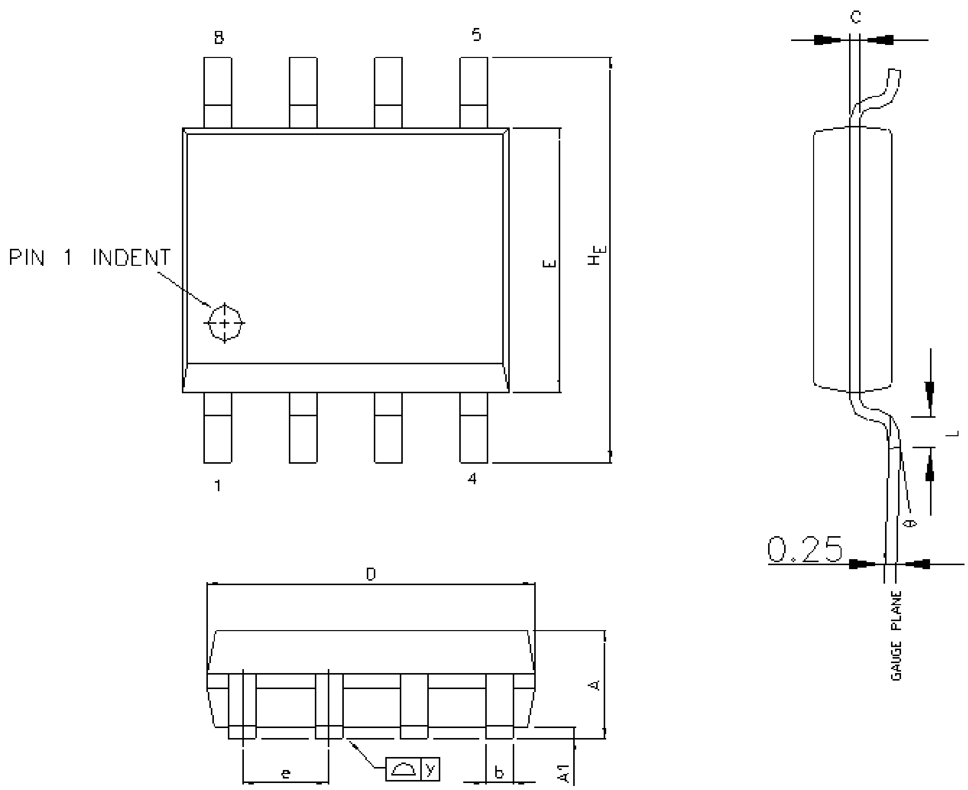



## 9.9 WP Timing



## 10. PACKAGE SPECIFICATIONS

### 10.1 8-Pin SOIC 150-mil (Package Code SN)

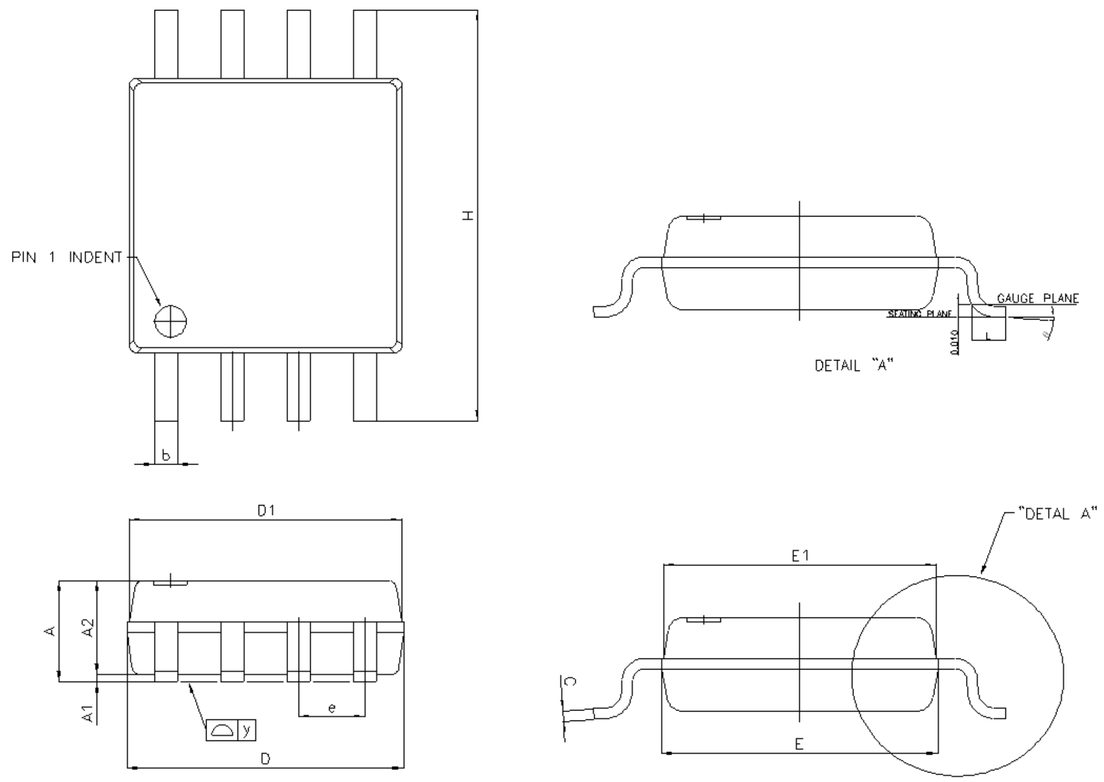



| SYMBOL | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 1.35 | 1.60 | 1.75 | 0.053 | 0.062 | 0.069 |
| A1 | 0.10 | 0.15 | 0.25 | 0.004 | 0.006 | 0.010 |
| b | 0.33 | 0.41 | 0.51 | 0.013 | 0.016 | 0.020 |
| C | 0.19 | 0.20 | 0.25 | 0.0075 | 0.0078 | 0.0098 |
| D | 4.80 | 4.85 | 5.00 | 0.188 | 0.190 | 0.197 |
| E | 3.80 | 3.90 | 4.00 | 0.150 | 0.153 | 0.157 |
| $H_E$ | 5.80 | 6.00 | 6.20 | 0.288 | 0.236 | 0.244 |
| e | 1.27BSC | | | 0.050BSC | | |
| L | 0.40 | 0.71 | 1.27 | 0.016 | 0.027 | 0.050 |
| y | --- | --- | 0.10 | --- | --- | 0.004 |
| θ° | 0° | --- | 10° | 0° | --- | 10° |

Note:

1. Control dimensions are in millimeter.
2. Both the package length and width do not include the mold flash. (Refer JEDEC MS-012)

## 10.2 8-Pin SOIC 208-mil (Package Code SS)

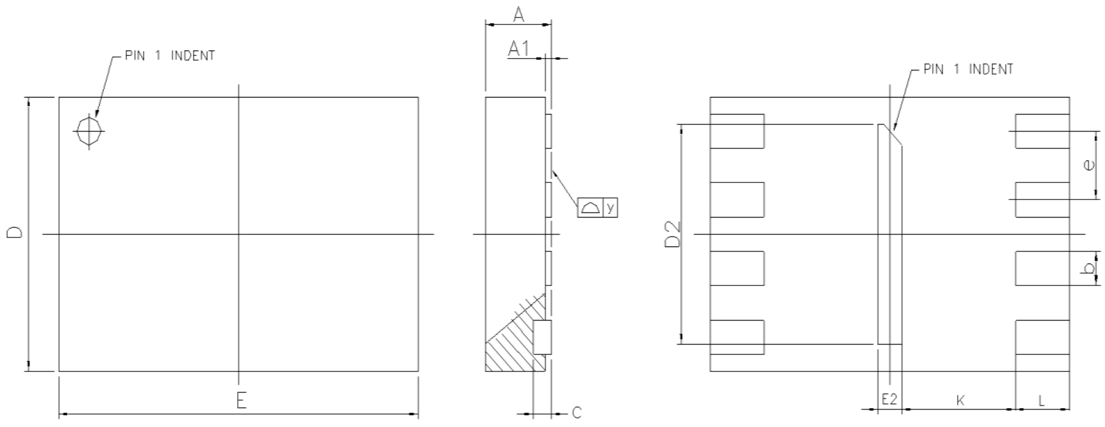



| Symbol | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 1.75 | 1.95 | 2.16 | 0.069 | 0.077 | 0.085 |
| A1 | 0.05 | 0.15 | 0.25 | 0.002 | 0.006 | 0.010 |
| A2 | 1.70 | 1.80 | 1.91 | 0.067 | 0.071 | 0.075 |
| b | 0.35 | 0.42 | 0.48 | 0.014 | 0.017 | 0.019 |
| C | 0.19 | 0.20 | 0.25 | 0.007 | 0.008 | 0.010 |
| D | 5.18 | 5.28 | 5.38 | 0.204 | 0.208 | 0.212 |
| D1 | 5.13 | 5.23 | 5.33 | 0.202 | 0.206 | 0.210 |
| E | 5.18 | 5.28 | 5.38 | 0.204 | 0.208 | 0.212 |
| E1 | 5.13 | 5.23 | 5.33 | 0.202 | 0.206 | 0.210 |
| e | 1.27 BSC | | | 0.050 BSC | | |
| H | 7.70 | 7.90 | 8.10 | 0.303 | 0.311 | 0.319 |
| L | 0.50 | 0.65 | 0.80 | 0.020 | 0.026 | 0.031 |
| y | --- | --- | 0.10 | --- | --- | 0.004 |
| θ | 0° | --- | 8° | 0° | --- | 8° |

Note:

1. Control dimensions are in millimeter.
2. Both the package length and width do not include the mold flash. (Refer JEDEC MS-012)

## 10.3 8-Pad XSON 2x3x0.4-mm (Package Code XH)

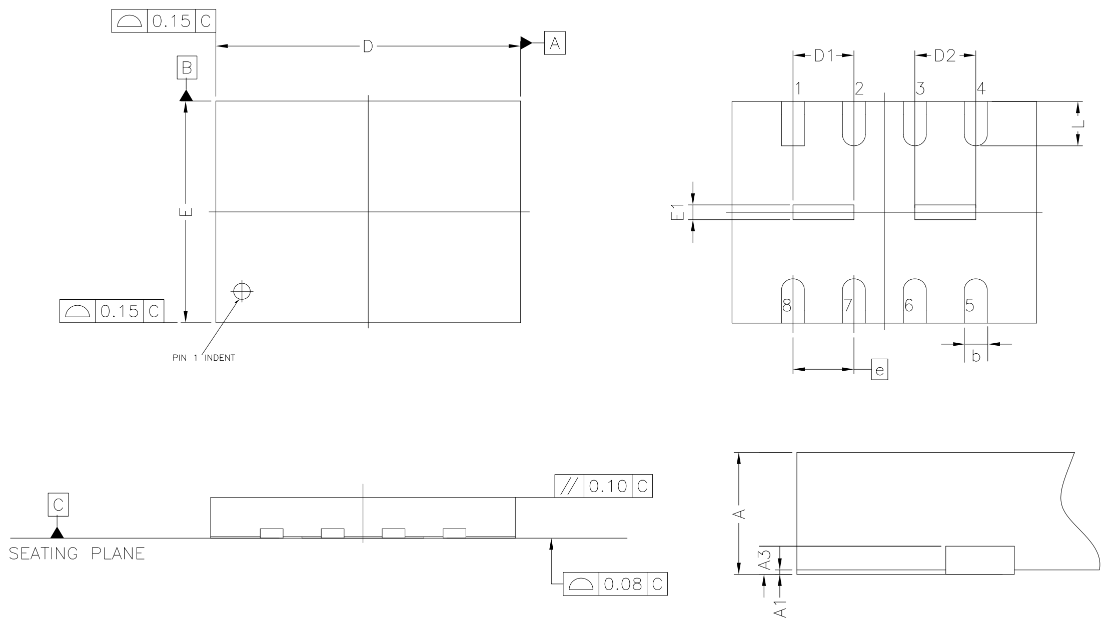



| Symbol | Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | 0.30 | 0.35 | 0.40 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.20 | 0.25 | 0.30 |
| C | --- | 0.127 Ref. | --- |
| D | 1.90 | 2.00 | 2.10 |
| D2 | 1.55 | 1.60 | 1.65 |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 0.15 | 0.20 | 0.25 |
| e | --- | 0.50 | --- |
| K | 0.95 Ref. | | |
| L | 0.40 | 0.45 | 0.50 |
| y | 0.00 | --- | 0.075 |

Note:

The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (VSS pin). Avoid placement of exposed PCB vias under the pad.

## 10.4 8-Pad USON 4x3-mm (Package Code UU)




| Symbol | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.50 | 0.55 | 0.60 | 0.020 | 0.022 | 0.024 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| A3 | --- | 0.15 | --- | --- | 0.006 | --- |
| b | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| D | 3.90 | 4.00 | 4.10 | 0.153 | 0.157 | 0.161 |
| D1 | 0.70 | 0.80 | 0.90 | 0.027 | 0.031 | 0.035 |
| D2 | 0.70 | 0.80 | 0.90 | 0.027 | 0.031 | 0.035 |
| E | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E1 | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| e | 0.80 BSC | | | 0.031 BSC | | |
| L | 0.55 | 0.60 | 0.65 | 0.022 | 0.024 | 0.026 |

### Notes:

1. Advanced Packaging Information; please contact Winbond for the latest minimum and maximum specifications.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. The metal pad area on the bottom center of the package is connected to the device ground (VSS pin). Avoid placement of exposed PCB vias under the pad.

## 10.5 Ordering Information

W[1] 25Q 33P W xx[2] I x

**Company Prefix**

W = Winbond

**Product Family**

25Q = SpiFlash Serial Flash Memory with 4KB sectors, Dual/Quad I/O

**Product Number / Density**

33P = 32M-BIT

**Supply Voltage**

w = 1.65V to 1.95V

**Package Type**

SN = 8-pin SOIC 150-mil
XH = 8-pad XSON 2x3x0.4-mm
SS = 8-pin SOIC 208-mil
UU = 8-pad USON 4x3mm

**Temperature Range**

I = Industrial (-40°C to +85°C)

**Special Options**[3,4]

Q = With QE = 1 (Fixed) in Status register-2.

Notes:

1. The "W" prefix is not included on the part marking.
2. Only the 2nd letter is used for the part marking; WSON package type ZP are not used for the part marking.
3. Standard bulk shipments are in Tube (shape E). Please specify alternate packing method, such as Tape and Reel (shape T) or Tray (shape S), when placing orders.
4. All devices are in compliance of RoHS, Halogen free, TSCA, REACH.

## 10.6 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the W25Q33PW SpiFlash Memory. Please contact Winbond for specific availability by density and package type. Winbond SpiFlash memories use a 12-digit Product Number for ordering. However, due to limited space, the Top Side Marking on all packages uses an abbreviated 10-digit number.

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **SS**<br>SOIC-8 208mil | *32M-BIT* | W25Q33PWSSIQ | 25Q33PWSIQ |
| **SN**<br>SOIC-8 150mil | *32M-BIT* | W25Q33PWSNIQ | 25Q33PWNIQ |
| **XH**<br>XSON 2x3x0.4mm | *32M-BIT* | W25Q33PWXHIQ | BWywH<br>IQxxxx |
| **UU**<br>USON-8 4x3mm | *32M-BIT* | W25Q33PWUUIQ | Q33UUIQ |

Note:

1. These package types are special order, please contact Winbond for more information.
2. “yw” is date code

## 11. REVISION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| A | 11/15/2024 | | New Create "Preliminary" |
| B | 12/25/2024 | 63 | Removed "Preliminary"<br>Updated ICC3(max.) @50MHz/84MHz |
| C | 01/08/2025 | 4,8,66,67 | Added JEDEC Reset Information |
| | | | |
| | | | |

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