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COMBINING ISD33xxx/4002/4003 DEVICES,

WITH WINBOND MICROCONTROLLERS

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1. Introduction

This Application Note was prepared for our Customers to facilitate engineering and quick starting with microprocessor circuits including ISD devices based on Winbond processors, series 80C51. The program code provided here includes basic procedures of data exchange between ISD device and microcontroller via SPI interface and of monitoring operating mode of ISD device as well. Each user may at his option use and customize the portions or the whole program outlined below.

Due to a double-byte word being entered into ISD, the program outlined below may by used for the following devices:

- **ISD 33060 – 33240**
- **ISD 4002 – 4003.**

2. Electric interconnections between microcontroller and ISD device

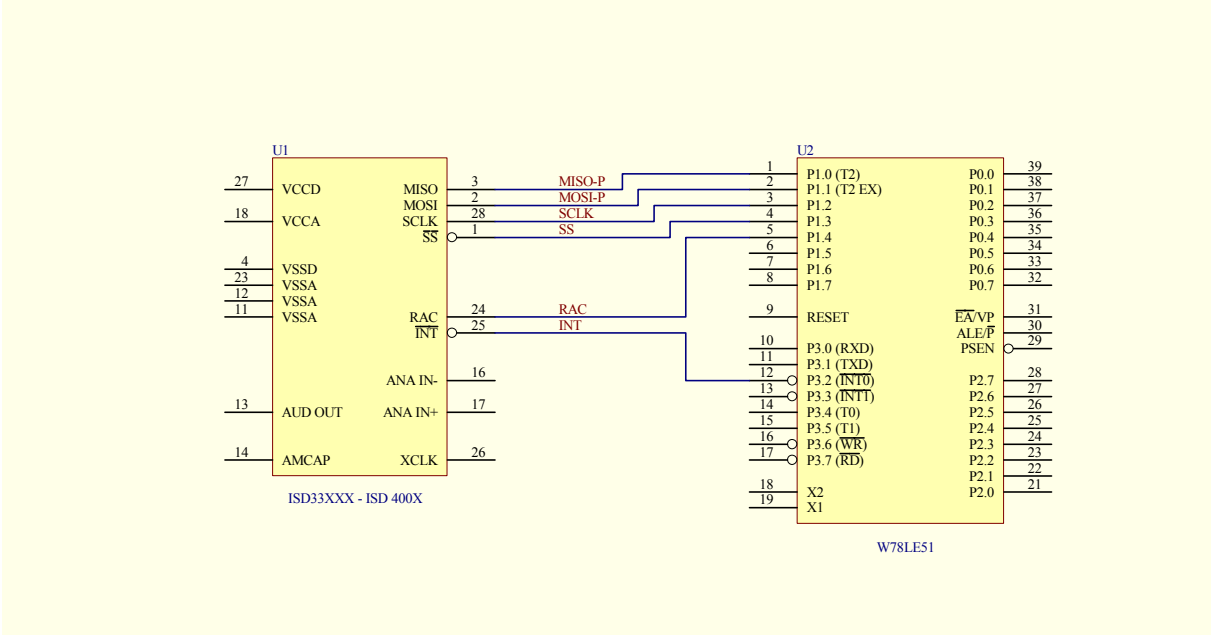

Fig.1. Interconnections between ISD device and microcontroller.

The SPI interface requires four lines to be provided for ISD device:

- **MISO** (*"Master in Slave out"*) – data transferred from ISD Slave to microntroller Master,
- **MOSI** *("Master out Slave in")* – data transferred from microcontroller to ISD device,
- **SCLK** *("Serial Clock")* – timing signal generated by microcontroller for SPI port,
- **SS** *("Slave Select")* – signal to activate SPI port of ISD device.

Additional connections of ISD device:

- **RAC** *("Row Address Clock")* – signal which represents one row of ISD memory. Transition to L-level indicates approaching the end of row being played back or recorded. This is an open drain type output.
- **INT** *("Interrupt")* – signal which goes low when ISD device detects End of Message Marker (**EOM** – *"End of Message") or when available ISD memory space is exceeded (**OVF** – "Overflow")*. This is an open drain type output. The INT signal may

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be cleared by successive read sequence for SPI port. Instruction *"RINT"* may be used to read the status of interrupt calling flags.

In above example, both microcontroller and ISD device are operating with the same supply voltage of **2.7 ÷ 3.3 V**. In case when the microcontroller is supplied with **5 V**, an appropriate voltage converter shall be used in **MISO** line as outlined in ***ChipCorder* Data Book**.

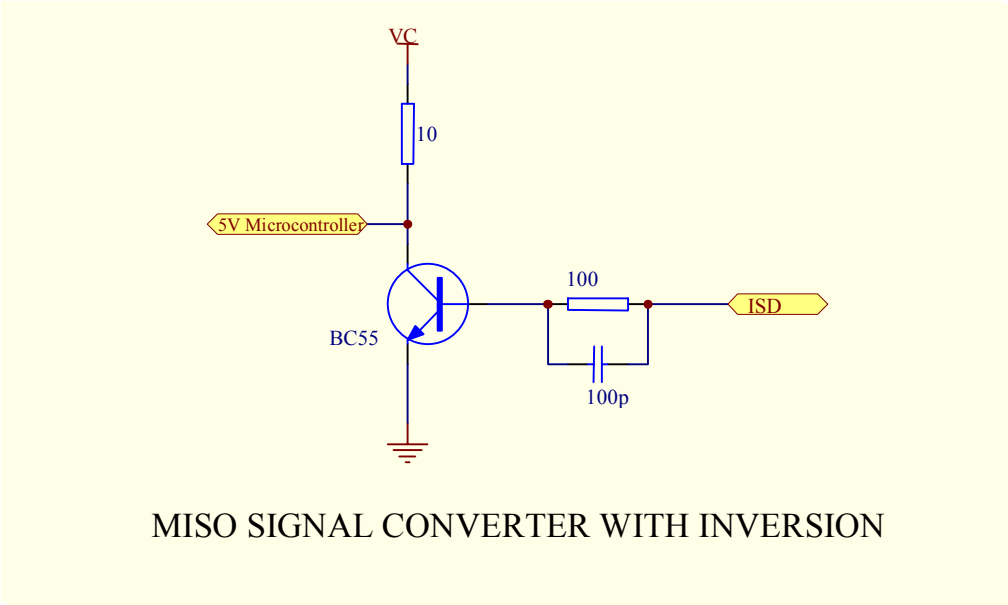

Fig.2. Voltage converter between microcontroller and ISD device.

If the converter of Figure 2 is used, the bits received by microcontroller from **MISO** port shall be negated (inversion). All other ports may be directly connected to the microcontroller supplied with +**5V**.

3. Start from specified address

To start with playing back or recording from specified address in ISD memory, enter the **SETPLAY (SETREC)** command. The LH edge of **SS** signal causes the address from MOSI register to be entered into internal row counter. Playback/record is run only for the ISD memory row addressed. Upon reaching the end of current row, the system stops and generates interrupt with OVF marker. If you want to proceed with playing back/recording through successive rows of ISD memory, enter **PLAY (RECORD)** command before the end of current row.

An example of program code portion to call PLAY operation from specified address through successive rows of ISD memory:

```
1. MOV  A,#SETPLAY     ; command "PLAY" from address specified
2. LCALL POLEC         ; placing the command
3. LCALL SPI           ; transferring the command with address to ISD
4. MOV A,#PLAY         ; proceeding with "PLAY" until EOM or OVF
5. LCALL POLEC         ; placing data for ISD
6. LCALL SPI           ; recording/playing back to/form ISD
```

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- Row 1: accumulator is loaded with "**SETPLAY"** command code defined as **11100000B.**
- Row 2: the **"POLEC"** procedure called out uses the accumulator contents and composes the final form of two bytes being sent to ISD. The less significant byte include the lower portion of ISD memory address. The more significant byte includes logical sum of the higher portion of address and ISD command code from accumulator. The contents of **"POLEC"** routine can by found at the end of this document.
- Row 3: the **"SPI"** communication procedure ensures, via simulation on SPI interface at microcontroller ports, data exchange between microcontroller and ISD device. Bytes being entered to ISD: MOSI (H) and MOSI+1 (L). Bytes being received from ISD: MISO (H) and MISO+1 (L). The contents of this procedure is included in an example provided at the end of this document.

  Note! Now, ISD device is in a single-row-playback mode. If you want to continue playing back through successive memory rows, you need to enter **"PLAY"** command before the end of current row.

- Row 4: like for the row No.1: command code **"PLAY" 11110000b.**
- Rows 5 and 6: like for rows 2 and 3 – setting up and transmitting a double-byte word to ISD.

4. System Stop/Power Down

A segment of program shown below represents the stop sequence for ISD device composed of three portions: (i) stop/pause of current operation (**"STOP"),** (ii) reading address after device stoppage and (iii) turning off the device (**"STOPPWRDN"**).

```
1. MOV    A.#STOP          ; command "STOP"
2. LCALL POLEC             ; placing the command
3. LCALL SPI               ; transferring the command to ISD
4. LCALL TIME              ; waiting c. 100 ms to stop the device
5. MOV    A,#STOPPWRDN     ; command "STOP" and power down
6. LACAL POLEC             ; placing the command
7. LCALL SPI               ; reading the address upon stoppage and power
                             down
```

- Row 1: accumulator is loaded with "**STOP"** command code defined as **00110000B.**
- Rows 2 and 3: similar to the previous clause.
- Row 4: calling "TIME" procedure causes generation of program delay during waiting until ISD is stopped.
- Rows 5, 6, and 7: transfer of command **"STOP POWER DOWN"** is combined with reading the address of ISD memory upon device stoppage.

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5. Modifying the playback/record address in RUN mode

In some applications, there is a need to make a jump to another (not just the next one) address of ISD memory while running playing back or recording a message. Respective steps to be made in the following orders:

a) before the end of playing back/recording of current row of ISD memory, enter the instruction **"SETPLAY"** or **"SETREC"** including the row address wherefrom you want to continue playback/record. The ISD device does not jump immediately but will continue to play back/record till the end of current row. At this time, the microcontroller shall read the status at **RAC** output. When the output goes low, it means the end of current row is approached. When **RAC** returns to high level, the current row is completed and a jump is made to the new ISD memory address.
b) following transition is made to play/record a new row, if you want to play/record consecutive rows of ISD memory, enter **"PLAY**" or **"REC"** command before the end of new row. If you want to make successive jump in ISD memory, repeat the procedure of item a) above.

6. Exemplary program

The program given below includes examples outlined above except the address modification during playing back/recording which has not been use here. In its main loop **"PETLA"**, the program checks the contents of **ROZKAZ** variable and performs respective command strings in ISD device. The **SPI** subprogram, which is used to exchange data between microcontroller and ISD device, may be used only without inverting converter for MISO signal (both ISD and microcontroller have the same supply voltage). At the end you can find the **SPI_K** procedure for the system with inverting converter for MISO signal (Fig.2).

Code examples:

```
;PDW "MARTHEL"
;declarations:

POWERUP         EQU   00100000B    ;ISD setup codes
SETPLAY         EQU   11100000B
PLAY            EQU   11110000B
SETREC          EQU   10100000B
REC             EQU   10110000B
SETMC           EQU   11101000B
MC              EQU   11111000B
STOP            EQU   00110000B
STOPPWRDN       EQU   00010000B
RINT            EQU   00110000B

;commands for main loop:

ISDPLAY         EQU   01      ;playing from address
ISDRECORD       EQU   02      ;recording from address
ISDSTOP         EQU   03      ;stop
ISDMC           EQU   04      ;fast forward from address

;ports declarations
```

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```
SS              EQU     P1.3    ;Slave Select
SCLK            EQU     P1.2    ;Clock
MOSI_P          EQU     P1.1    ;Master Out Slave In
MISO_P          EQU     P1.0    ;Master In Slave Out
RAC             EQU     P1.4    ;RAC signal

;data segment:

dseg at 30h

MISO:           DS 2    ;bytes read from ISD H-L
MOSI:           DS 2    ;bytes written to ISD H-L
ADRESISD:       DS 2    ;ISD read address H-L
ADRES:          DS 2    ;ISD written address H-L
RACBLOK:        DS 1    ;RAC check blocking flag
ROZKAZ:         DS 1    ;command for main loop
TRYB:           DS 1    ;ISD actual mode (last command)

cseg at 0

LJMP                    MAIN    ;jump to main loop

cseg at 03h

LJMP    INT0_SERV       ;INT0 interrupt service

MAIN:

;Main loop
;---------------------------------------------------------------------
PETLA:          MOV     A,ROZKAZ

SPR1:           CJNE    A,#ISDPLAY,SPR2      ;command checking
                MOV     TRYB,A          ;ISD in PLAY mode
                LCALL   WAKEUP          ;ISD wake up
                MOV     A,#SETPLAY      ;"PLAY" from address command
                LCALL   POLEC           ;preparing data
                LCALL   SPI             ;SPI data writing/reading
                MOV     A,#PLAY         ;"PLAY" continuation through the next rows
                LCALL   POLEC           ;preparing data
                LCALL   SPI             ;SPI data writing/reading
                MOV     ROZKAZ,#0       ;clearing command
                JMP     PETLA           ;main loop

SPR2:           CJNE    A,#ISDRECORD,SPR3
                MOV     TRYB,A          ;ISD in RECORD mode
                LCALL   WAKEUP
                MOV     A,#SETREC       ;recording from address
                LCALL   POLEC
                LCALL   SPI
                MOV     A,#REC          ;recording continuation through rows
                LCALL   POLEC
                LCALL   SPI
                MOV     ROZKAZ,#0
                JMP     PETLA

SPR3:           CJNE    A,#ISDSTOP,SPR4
                MOV     TRYB,A          ;ISD in STOP mode
```

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```
                MOV   A,#STOP       ;"STOP" command
                LCALL POLEC
                LCALL SPI
                LCALL TIME          ;timeout about 100 ms
                MOV   A,#STOPPWRDN
                LCALL POLEC         ;reading STOP address and power down
                LCALL SPI
                LCALL ADRISD        ;read data correction
                MOV   ROZKAZ,#0
                JMP   PETLA         ;main loop

;Fast forward through ISD memory. ISD stopping by EOM or OVF marker and generating interrupt.

SPR4:           CJNE  A,#ISDMC,SPR5
                MOV   A,TRYB        ;ISD mode checking
                CLR   C
                SUBB  A,#ISDMC      ;MC continuation if the next MC command
                JZ    SPR4_SK       ;jump to the MC continuation from the current address
                MOV   TRYB,#ISDMC   ;ISD in MC mode
                LCALL WAKEUP
                MOV   A,#SETMC      ;MC from the address command
                LCALL POLEC
                LCALL SPI           ;writing command
SPR4_SK:
                MOV   A,#MC         ;MC continuation
                LCALL POLEC
                LCALL SPI
                MOV   ROZKAZ,#0
                JMP   PETLA

;RAC checking and current address increment:

SPR5:
                JNB   RAC,SPR6      ;clearing RAC flag after the end of RAC pulse
                MOV   RACBLOK,#0
                JMP   PETLA

SPR6:           MOV   A,TRYB        ;ISD mode checking
                CJNE  A,#ISDMC,POM  ;don't count RAC pulses, if MC mode
                JMP   PETLA         ;main loop if MC mode
POM:            MOV   A,RACBLOK
                JNZ   W             ;only 1 time in 1 RAC pulse
                INC   RACBLOK
                MOV   A,ADRESISD+1  ;ISD address increment
                ADD   A,#1
                MOV   ADRESISD+1,A
                MOV   A,ADRESISD
                ADDC  A,#0          ;carry bit
                MOV   ADRESISD,A

W:              JMP   PETLA

WAKEUP:         MOV   A,#POWERUP    ;wake up of ISD
                LCALL POLEC
                LCALL SPI
                LCALL TIME
                RET

;timeout about 100 ms
```

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```
TIME:   MOV   R7,#0
        MOV   R6,#180
SKK:    DJNZ  R7,$          ;256*2*180*1.085 us; Q=11.0592 MHz
        DJNZ  R6,SKK        ;without the rest
        RET



;INT0 service:

INT0_SERV:
        PUSH  ACC
        MOV   A,#RINT
        LCALL POLEC
        LCALL SPI           ;reading of ISD interrupt flag
        LCALL ADRISD        ;ISD data correction
        MOV   A,MISO+1      ;flags on the lowest significant positions
        JNB   ACC.1,OVF     ;jump if the memory overflow
        POP   ACC
        RETI

OVF:    MOV   TRYB,#0               ;ISD in STOP mode
        MOV   A,#STOPPWRDN          ;power down
        LCALL POLEC
        LCALL SPI
        POP   ACC
        RETI

;ISD data correction to remove EOM & OVF from the address:
; R4, R5, R7, ACC changed

ADRISD: CLR   C
        MOV   R7,#2
        MOV   R4,MISO
        MOV   R5,MISO+1
PRZES:  MOV   A,R4
        RRC   A
        MOV   R4,A
        MOV   A,R5
        RRC   A
        MOV   R5,A
        DJNZ  R7,PRZES
        MOV   A,R4
        CLR   ACC.7         ;clearing OVF
        CLR   ACC.6         ;clearing EOM
        MOV   R4,A
        MOV   ADRESISD,R4           ;H
        MOV   ADRESISD+1,R5         ;L
        RET

;ISD SPI interface:

;registers:
;R2 -> MOSI (H)
;R3 -> MOSI+1 (L)
;R4 -> MISO (H)
;R5 -> MISO+1 (L)
;R2, R3, R4, R5, R7 changed
```

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```
SPI:        MOV   R2,MOSI       ;data to send
            MOV   R3,MOSI+1

            CLR   SCLK
            MOV   R7,#8
            CLR   SS            ;chip selection
BAJT_L:
            CLR   SCLK
            MOV   A,R5          ;MISO+1 (L)
            MOV   C,MISO_P
            RRC   A
            MOV   R5,A          ;MISO+1 (L)
            MOV   A,R3          ;MOSI+1 (L)
            RRC   A
            MOV   MOSI_P,C
            MOV   R3,A          ;MOSI+1 (L)
            SETB  SCLK
            DJNZ  R7,BAJT_L
            MOV   R7,#8
BAJT_H:
            CLR   SCLK
            MOV   A,R4          ;MISO (H)
            MOV   C,MISO_P
            RRC   A
            MOV   R4,A          ;MISO (H)
            MOV   A,R2          ;MOSI (H)
            RRC   A
            MOV   MOSI_P,C
            MOV   R2,A          ;MOSI (H)
            SETB  SCLK
            DJNZ  R7,BAJT_H
            SETB  SS            ;end of transmission

            MOV   MISO,R4       ;received data
            MOV   MISO+1,R5
            RET

;ISD data preparing:

;ISD command in ACC
;ISD address in ADRES & ADRES+1
;result in MOSI (HIGH)  MOSI+1 (LOW)

POLEC:      MOV   MOSI+1,ADRES+1    ;low byte of ISD SPI command
            ORL   A,ADRES           ;ISD command “OR” high byte of ISD address
            MOV   MOSI,A
            MOV   ADRESISD,ADRES
            MOV   ADRESISD+1,ADRES+1        ;backup of actual ISD address
            RET


;ISD SPI interface  (MISO inversion):

;R2 -> MOSI (H)
;R3 -> MOSI+1 (L)
;R4 -> MISO (H)
;R5 -> MISO+1 (L)
;R2, R3, R4, R5, R7 changed
```

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```
SPI_K:      MOV   R2,MOSI       ;data for sending
            MOV   R3,MOSI+1

            CLR   SCLK
            MOV   R7,#8
            CLR   SS            ;chip selection
BAJT_L:
            CLR   SCLK
            MOV   A,R5          ;MISO+1 (L)
            MOV   C,MISO_P
            CPL   C             ;MISO inversion
            RRC   A
            MOV   R5,A          ;MISO+1 (L)
            MOV   A,R3          ;MOSI+1 (L)
            RRC   A
            MOV   MOSI_P,C
            MOV   R3,A          ;MOSI+1 (L)
            SETB  SCLK
            DJNZ  R7,BAJT_L
            MOV   R7,#8
BAJT_H:
            CLR   SCLK
            MOV   A,R4          ;MISO (H)
            MOV   C,MISO_P
            CPL   C             ;MISO inversion
            RRC   A
            MOV   R4,A          ;MISO (H)
            MOV   A,R2          ;MOSI (H)
            RRC   A
            MOV   MOSI_P,C
            MOV   R2,A          ;MOSI (H)
            SETB  SCLK
            DJNZ  R7,BAJT_H
            SETB  SS            ;end of transmission

            MOV   MISO,R4       ;received data
            MOV   MISO+1,R5
            RET
```