1.8V 512M-BIT
OCTAL-DDR FLASH MEMORY WITH ECC

BYTE-WIDE DDR FLASH MEMORY

Publication Release Date: Nov 10, 2024
Revision B

winbond

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1. GENERAL DESCRIPTIONS

The W35T51NW (512M-bit) Octal-DDR SpiFlash memory features the Xccela Flash bus interface which delivers the highest synchronous byte-wide (8-bit) data bandwidth for code and data storage memory solutions for embedded applications. While providing maximum performance with low signal count, the 35T family offers flexibility and burst speed superior than embedded-type memory execution on an external synchronous bus interface. It is ideal for executing code directly from the Octal-DDR SpiFlash while it can also be used for data storage. The device operates on a single 1.65V to 2.0V power supply with current consumption as low 1µA during power-down mode.

The W35T51NW supports Standard Serial Peripheral Interface (SPI) and 8-bit I/O (Octal) interface as well as Double Data Rate (DDR): Serial Clock (CLK), Chip Select (/CS), Serial Data (IO_7, IO_6, IO_5, IO_4, IO_3, IO_2 (/WP), IO_1, IO_0), /Reset, and Data Strobe (DS) for BGA packages. Clock frequencies of up to 200MHz are supported with DDR Data Strobe allowing equivalent clock rates of 400MHz x 8 for DDR Octal I/O Read commands. The transfer rate outperforms traditional Synchronous SPI/Dual SPI/Quad SPI memories and standard Asynchronous 8 and 16-bit Parallel Flash memories.

For Read operations, nonvolatile and volatile configuration register values control the device operational settings such as the IO mode configuration, the number of dummy clock cycles, wrap mode configuration, output buffer drive strength, address mode configuration, and Execute-in-Place (XIP) mode setting. In DDR IO mode, data transmission is on both clock edges (rising/falling) and on eight data lines, so legacy 8-bit (Byte) SPI commands are supported with only one clock cycle to latch in the command opcode. The Data Strobe (DS) pin optimizes the device operation when latching data with a DDR speed of up to the maximum frequency (200 MHz).

The W35T51NW memory array is organized in 256-byte programmable pages along with erasable 4KB sectors, 32KB / 64KB blocks, or the entire chip. There are 262,144 programmable pages and 1 to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase), or the entire chip (chip erase). The W35T51NW has 16,384 erasable 4KB sectors and 1,024 erasable 64KB blocks respectively. The small 4KB sectors benefit applications that require configuration and parameter data storage. Suspend and Resume commands provide ways to temporarily halt and resume program or erase operations.

The W35T51NW has three 1KB Security Registers separate from the main memory that users can read, program, erase, or permanently lock. A Write Protect (/WP) pin is a programmable option to protect against writes to the Status Register. Memory Protection is offered with traditional Status Register Block Protection bits. The device supports JEDEC standard Manufacturer and Device ID with an additional 3-byte device ID Configuration. Additionally, the device supports JEDEC - Serial Flash Data Parameter (SFDP).

The ECC enabled W35T51NW has additional features related to ECC and Reset functionality. These features are supplemented to support and enhance device performance in highly intensive industrial and automotive operating environment. The W35T51NW supports 1-bit ECC every 16-byte alignment and offers both internal ECC Status and an external pin to monitor the ECC error. A Reset status output pin is also provided to monitor the initiated hardware reset and software reset status.

2. FEATURES

- **New Octal DDR SpiFlash Memories**
  - W35T51NW: 512M-bit / 64M-byte
- **Supported Synchronous Bus Interface**
  - Byte-Wide (x8) Multiplexed Synchronous IO
  - Single Data Rate (SDR) and Double Data Rate (DDR)
  - DDR Bus Mode
    - Octal Double Data Rate (ODDR) protocol: CLK, /CS, IO[7:0], DS, /Reset
  - Extended SPI (SDR Bus Mode)
    - Octal SPI (OSPI) and OSPI DDR protocol : CLK, /CS, IO[7:0] /WP, /Reset
    - Standard SPI protocol (SPI): CLK, /CS, IO_0, IO_1, /WP, /Reset
- **Clock Frequency**
  - 166 MHz SDR max (166 MB/s)
  - 200 MHz DDR max (400 MB/s) with Data Strobe (DS)
- **Read Modes via Volatile and Nonvolatile Register Settings**
  - Continuous Read Data Burst after Standard Command + Address + Dummy Cycles (C-A-D) Input
  - Execute-in-Place (XIP) Continuous Read Data Burst after Address + Dummy Cycles (A-D)
  - 16/32/64 Byte Wrap Around Read Data Burst after C-A-D Input
- **On-Chip ECC[1]**
  - 1-Bit Correction every 16-Bytes
  - Internal ECC Status Bits error indicator
  - Interrupt Output pin flag (/INT) to monitor error during Read
- **Address Modes**
  - 3-Byte and 4-Byte Addressing Mode to access memory address greater than 128Mb
- **Low Power, Wide Temperature**
  - Single 1.65 to 2.0V supply
  - 40mA Read current (typ.)
  - <15µA Standby Power-down (typ.)
  - <1µA Power-down (typ.)
  - -40°C to +85/+105°C operating range
- **Highest Performance SpiFlash**
  - Min. 100K Program-Erase cycles[2]
  - More than 20-year data retention[3]
- **Flexible Memory Architecture with 4KB sectors**
  - Uniform Sector/Block Erase (4K/32K/64K-Byte)
  - Erase whole chip (Chip Erase)
  - Program 1 to 256 byte per programmable page[1]
  - Erase/Program Suspend & Resume
- **Power-up Status Detection**
  - Fail/Safe power-up hardware monitor (/INT)
  - Fail/Safe power up state on Registers (BUSY Bit / READY Flag)
- **Reset Options**
  - Hardware Reset (/Reset)
  - JEDEC Hardware Reset
  - Software Reset
  - Reset Output pin (/RSTO)
- **Security Registers**
  - Three 1K-Byte Security Registers
  - Read accessible
  - Programmable and Erasable with lock options
  - Permanent Lock option
- **Data Integrity Check**
  - Cyclic Redundancy Check (CRC) at rest to check on accidental changes to raw data
  - Cyclic Redundancy Check (CRC) in transit to monitor data integrity during high speed data transmission
- **Memory Protection**
  - Hardware Write-Protect with protection range control by Block Protection and Top/Bottom Status Register bits
- **Device ID**
  - 6-Bytes JEDEC Read ID
- **Unique ID**
  - 16-Bytes Unique ID
- **Serial Flash Discovery Parameter (SFDP)**
  - 1K-Byte SFDP
- **Space Efficient Packaging[4]**
  - 24-ball TFBGA 8x6-mm
  - Contact Winbond for KGD and other options

Notes:

1. To maintain the ECC operation (ECC On Status) on aligned 16-byte memories across the full memory range (on LSB address A[3:0] = 0000b to 1111b) during reads, one time programming of one byte up to 16 bytes of data per aligned 16-Byte memory is required. More than one time programming on aligned 16-byte memories will turn off ECC functionality (ECC Off status) automatically on those affected aligned 16-byte memories during reads. An Erase is to recover back ECC operations (ECC On Status) of these affected aligned memories during read.
2. More than 100,000 Block Erase/Program cycles for Industrial temperature.
3. Data retention time will reduce significantly after extensive Program/Erase cycling at high temperature.
4. Not all package types are available for ordering. Please contact Winbond sales for detailed information.

3. BLOCK DIAGRAM

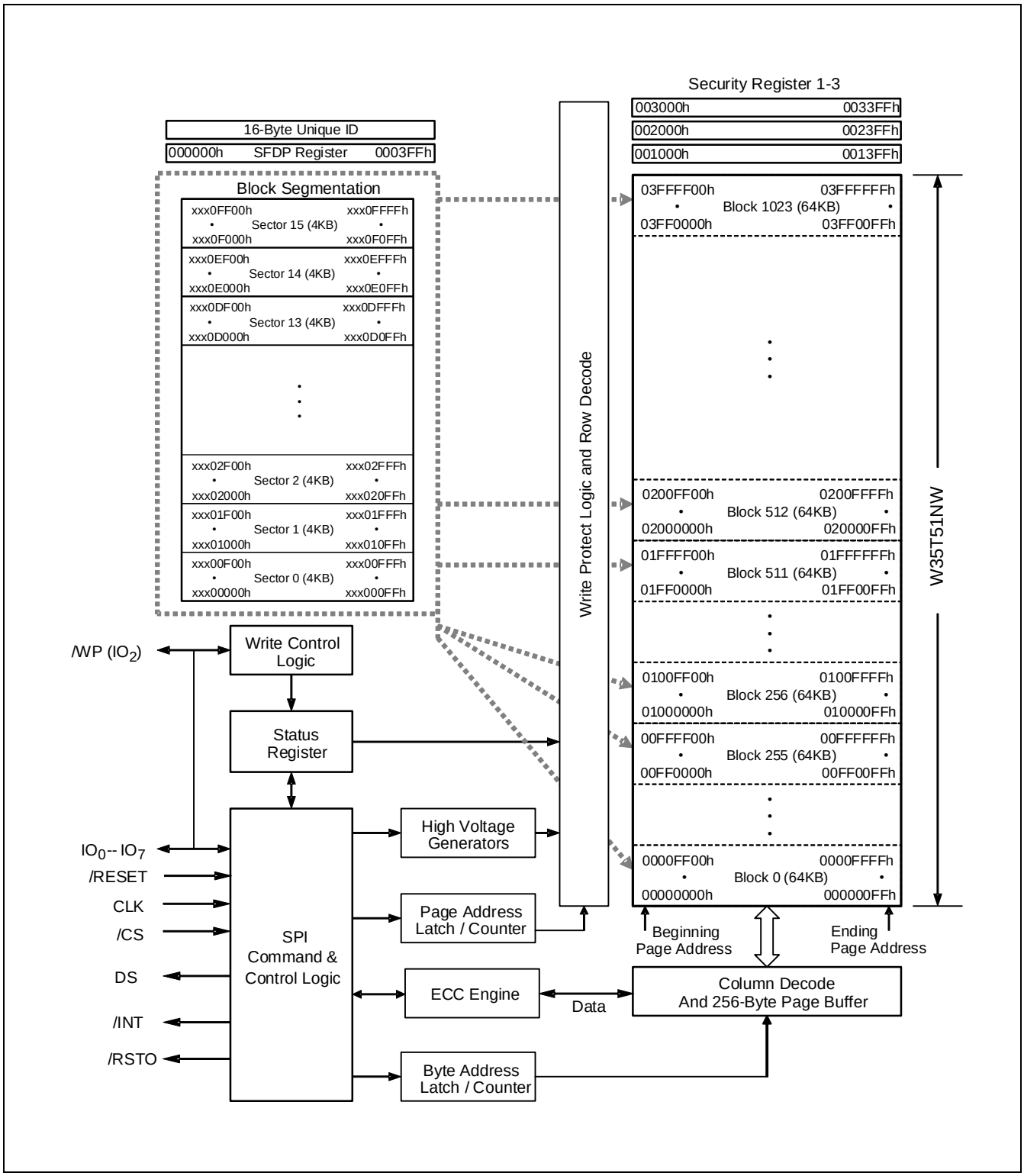


Figure 1. W35T51NW Serial Flash Memory Block Diagram

4. PIN DESCRIPTIONS

4.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS pin is high, the device is deselected and the Data Input Output (IO0, IO1, IO2, IO3, IO4, IO5, IO6, IO7) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS pin is asserted the device will be selected, power consumption will increase to active levels and commands can be initiated to write and read from the device. After power-up, /CS pin must transition from high to low before a new command will be accepted. The /CS pin input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 19-2). If needed, a pull-up resistor on the /CS pin can be used to accomplish this.

4.2 Serial Clock (CLK)

The Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See Device Operations"). In Extended SPI (SDR mode), data input is latched on the rising edge of CLK and data output is shifted out on the falling edge of CLK. In DDR mode, both data input and output are latched and shifted out on the rising and falling edge of CLK.

4.3 Data Input Output (IO0, IO1, IO2, IO3, IO5, IO5, IO6, IO7)

The W35T51NW supports standard Single Data Rate (SDR) mode (using either SPI or Octal SPI), and Octal DDR operation. In SDR mode, Standard SPI commands use the unidirectional IO0 (input) pin to serially write commands, addresses, or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional IO1 (output) to read data or status from the device on the falling edge of CLK. Octal SPI commands use the bi-directional IO[7:0] pins to serially write commands (command input on IO0), addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

Octal DDR mode operations also use bi-directional IO[7:0] pins using the rising and falling edge of CLK to latch in the input command, address, and data. Data output on IO[7:0] pins is shifted out on the falling and rising edge of CLK.

4.4 Write Protect (/WP)

When the device is in SDR mode, the Write Protect (/WP) pin can be used to protect the Status Register against any writes (program or erase). It is used as a hardware protect pin against writes to the setting of Status Register’s Block Protect TB, BP3, BP2, BP1 and BP0 bits. The /WP pin is active low. Status Register Bit 7 (SRP) set to ’1’ (default) enables Write Protection. When /WP is driven low and SRP bit is set to ‘1’, the Status Register nonvolatile bits (TB, BP3, BP2, BP1, BP0) are read-only and the Write Status Register command will be ignored. Driving the /WP pin high will exit the hardware write protection mode.

In ODDR Mode, /WP pin functionality is disabled and the Status Register SRP bit will have no function, thus the /WP pin is an IO2 pin in this mode.

4.5 Data Strobe (DS)

The Data Strobe (DS) pin is required to support DDR clock speeds higher than 133MHz. It is an output pin signal to aid validating and synchronizing data output for the host at higher clock speeds. The DS pin is used during read operations and it is not used during program, erase, or write operations. It is configured by a Non-Volatile Configuration Register (NVCR) or Volatile Configuration Register (VCR) Address 00h, the IO Mode Configuration (IOC), set to FFh in SDR mode or E7h in ODDR mode (Bit 5 set to ‘1’).

When the DS pin is enabled, the device drives the DS output pin low from a high impedance state after the CS pin is asserted and the first input clock is shifted in. The read command sequence continues until the

IO pins transition from input to data output sequence. At the same time the DS pin toggles simultaneously to synchronize every data output transition on either the falling edge of the clock during extended SPI or both edges of the clock during DDR. Once the /CS pin is driven high after a read sequence, the DS pin will go back to a high impedance state.

The DS pin is not driven and is in high impedance when it is disabled by a NVCR-IOC and VCR-IOC Address of 00h setting, the IO Mode Configuration, with a value of DFh in SDR mode or a value of C7h in ODDR mode (Bit 5 = '0').

4.6 Hardware Reset (/RESET)

The hardware /RESET pin allows the device to be reset by the host controller. When the /RESET pin is high, the device is in normal operating mode. Hardware reset is initiated by driving the /Reset pin low for a minimum of 50 ns (tRLRH). A successful hardware reset will reset the device to its default power-up state that includes resetting its Volatile Configuration Register bits setting, volatile Status Register, and Flag Registers. The device will use the non-Volatile Configuration Register settings as the default device configuration from hardware reset. The /RESET pad is tied with a weak pull-up internally, so this pin can be left floating if not used.

A hardware reset during an active Program or Erase operation aborts the write operation; furthermore, the target address range of the write operation may be corrupted or lost due to the aborted erase or program operation. When the internal reset is initiated, the /RSTO pin is driven low and the device will take approximately tRST time (30us max) to reset. During this period, no command will be accepted by the device. Once the internal reset is completed, the /RSTO pin will transition from low to high impedance and device is readily accessible. It is recommended to perform a verification of the memory and perform the appropriate actions to recover from the aborted erase or program operation.

4.7 Reset Output (/RSTO)

The Reset Output pin is provided to the system hardware designers to determine if the flash device is busy performing device initialization or internal reset. The /RSTO pin will be pulled low through the Open-Drain connection during the device power-on-reset (POR) period and after a POR failure occurrence. It can also be driven low by either a software reset command, a hardware reset by the /Reset pin, or a JEDEC Hardware reset.

During the power-up sequence, the device has a fail/safe detect monitoring sequence that after a POR the device offers a hardware status using the /RSTO pin. During the Vcc ramp up and before tVSL time (Vcc min to /CS Low Time), the /RSTO pin will be driven low. During Vcc ramp up until tVSL time, no command will be accepted by the device.

If the device initialization is successful, the /RSTO pin transitions from a low to a high impedance state after tVSL time. If the device initialization fails including a possible wrong I/O configuration during power-up, the /RSTO pin will remain low after the device gets out of POR indicating the failure. The BUSY bit of the Status Register is set to '1'; the WEL bit of the Status Register is '0'; and the READY Flag (RF) of the Flag Register is cleared to '0' when a power-up initialization failure occurs. These register bits are accessible if the device I/O configuration setup is still intact. The power cycle timing with the /RSTO pin is shown in Figure 19-3.

After the initiation of the reset sequence (software and hardware), no command will be accepted by the device while the /RSTO pin is pulled low internally. The /RSTO pin will transition from low to high impedance after internal reset completion, and the device is readily accessible. In case of a power-up initialization failure, an initiation of a reset sequence will only clear the power-up initialization error flags of "/RSTO pin=Low, BUSY=1, WEL=0, and RF=0" to "/RSTO pin=high impedance, BUSY=0, WEL=0, and RF=1; and it will not recover from the power-up initialization error. Depending on the type of initialization error, a device power off/on cycle may or may not recover the power on reset error, and the device may not be fully operational. Please check the Fail/Safe Power-Up Detection and Interface Recovery section for details on power up detection.

4.8 Interrupt Output (/INT)

The Interrupt Output pin is provided to the system hardware designers to determine the ECC status during any Read operation. When the internal ECC engine is disabled (ECC=0 in Extended Register), the /INT pin is also disabled. When ECC is enabled (ECC=1 in Extended Register), the /INT pin will be pulled low during any 16-Byte (128-Bit) Read data output period in which an ECC event has occurred. Depending on the INT bit setting in the Extended Register, the /INT pin can be used to represent either a SEC (Single Error Correction) or a DED (Double Error Detection). The Interrupt Output pin is an Open-Drain connection.

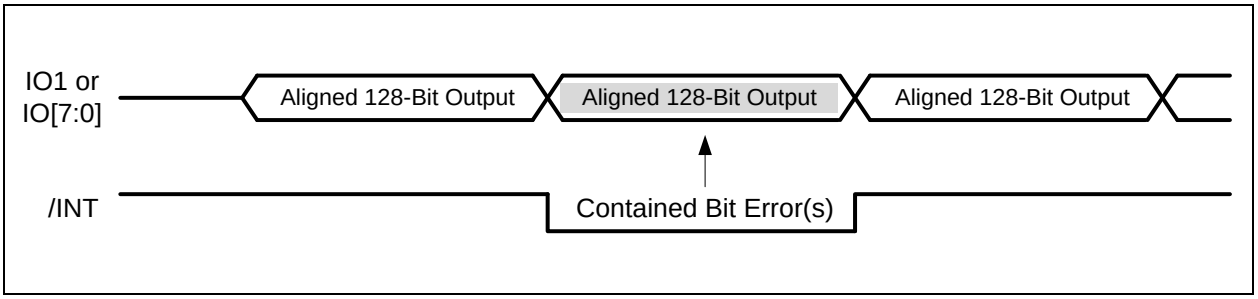


Figure 2. Interrupt Output Pin ECC Event Waveform

5. PACKAGE TYPES AND PIN CONFIGURATIONS

The W35T51NW is offered in a 24-ball, 5x5 ball array, 8x6-mm TFBGA (package code TB) as shown on Figure 3-1. Package diagrams and dimensions are illustrated at the end of this datasheet.

5.1 Industrial Grade Ball Configuration TFBGA 8x6-mm (5x5 Ball Array)

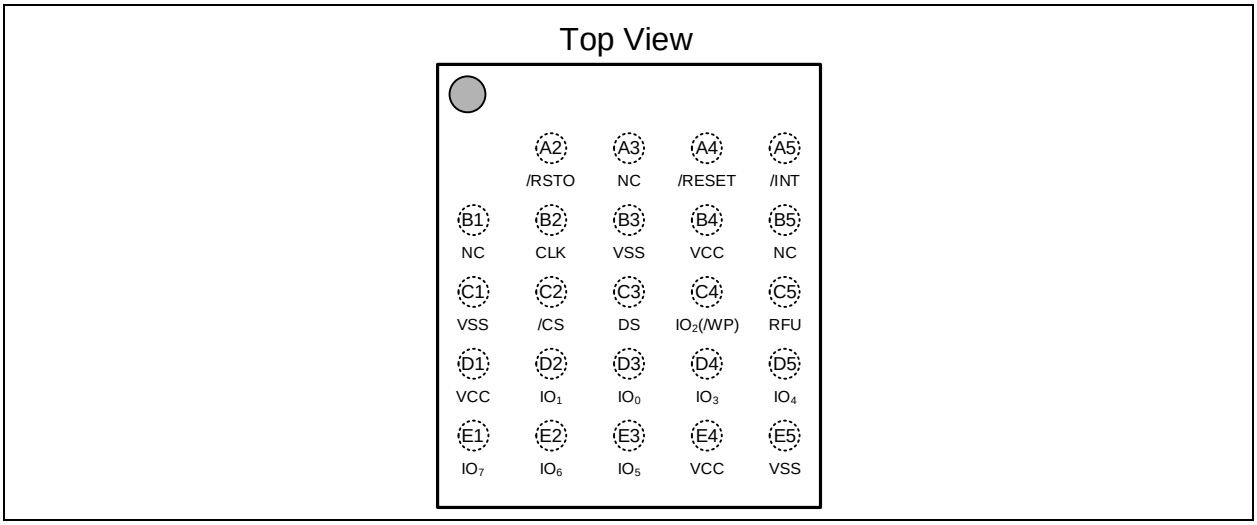


Figure 3-1. W35T51NW Ball Assignments, 24-ball (5x5 ball array) TFBGA 6x8-mm (Package Code TB)

5.2 Ball Description TFBGA 8x6-mm

BALL NO.	PIN NAME	I/O	FUNCTION
A2	/RSTO	O (Open-Drain)	Reset Output. Upon completion of internal power-on-reset, the /RSTO signal will transition from Low to high impedance. At this point, the external pull-up resistance will pull /RSTO High indicating that flash is idle and ready.
A4	/RESET	I	Reset Input(3)
A5	/INT	O (Open-Drain)	Interrupt Output. When Low, indicating that an internal event has occurred.
B2	CLK	I	Serial Clock Input
B3, C1, E5	VSS		Ground.
B4, D1, E4	VCC		Power Supply.
C2	/CS	I	Chip Select
C3	DS	O	Data Strobe. Required for clock speed higher than 133MHz.
C4	IO2 (/WP)	I/O	Data Input Output 2 (Write Protect Input)(1,2)
C5	RFU		Reserved for future use(4).
D2	IO1	I/O	Data Input Output 1(1,2)
D3	IO0	I/O	Data Input Output 0(2)
D4	IO3	I/O	Data Input Output 3(2)
D5	IO4	I/O	Data Input Output 4(2)
E1	IO7	I/O	Data Input Output 7(2)
E2	IO6	I/O	Data Input Output 6(2)
E3	IO5	I/O	Data Input Output 5(2)
A3, B1, B5	NC		No Connect

Notes:

1. IO0 and IO1 are used for Standard SPI commands.
2. IO0 – IO7 are used for Octal Read commands. /WP is configurable by Status Register bit 7 (SRP).
3. The /RESET pin is a dedicated hardware reset pin regardless of device settings. If the reset pin function is not used, this pin can be left floating in the system. This pad is internally tied to a weak pull-up.
4. This pin can be left floating in the system.

6. FUNCTIONAL DESCRIPTIONS

6.1 Device Operations

The W35T51NW powers up either in Execute-in-Place (XIP) Mode or Standard Command Mode based on the Non-Volatile Configuration Register values settings transferred to the Volatile Configuration Register settings and Internal Configuration Register. The diagram in Figure 4 illustrates the device memory read operations.

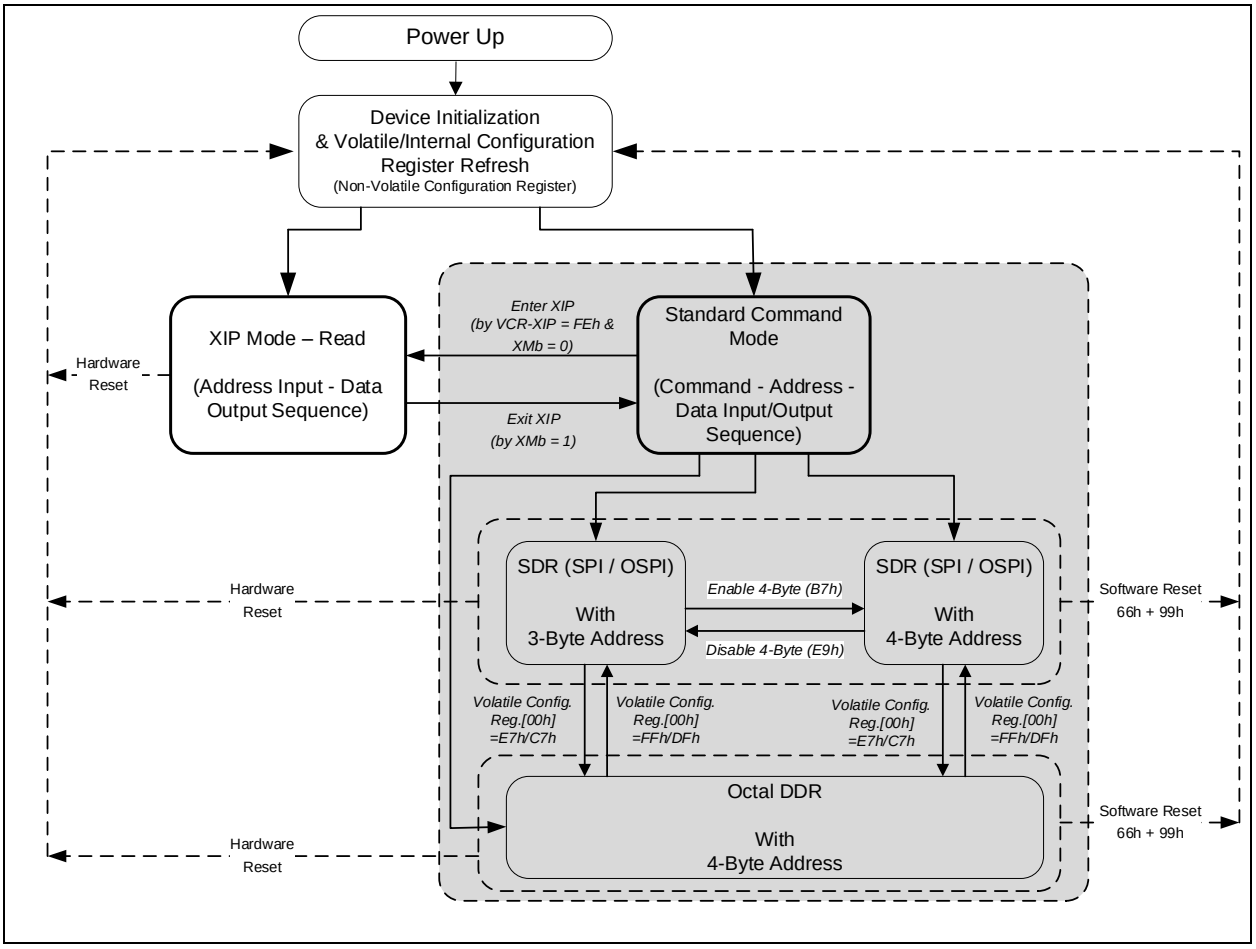


Figure 4-1. W35T51NW Serial Flash Memory Operation Diagram

When the device powers up in XIP Mode, the device is in a special read memory only configuration and the device expects to have the Address input and set Dummy CLK cycles before output read data shifts out of the device. The device will not recognize any of the valid command sequences until the device exits XIP mode by setting the XIP Mode (XMb) bit to '1' during the XIP Read sequence. XIP mode boot will be default until modified by the Write Non-Volatile Configuration Register Address [05h] to 'FFh' after exit of XIP Mode. XIP mode is detailed in Section 6.5 Execute-in-Place (XIP) Mode.

When powering up from Standard Command Mode, the device operates in typical Command based protocol. The device supports a set of Commands detailed in Section 8.1 Command Set Table and in Section 9 Command Cycles. In this mode, the device supports read memory/registers, program memory,

erase memory, write registers, suspend/resume, and other commands. Standard commands are supported in one of the following IO Mode Configurations from the Non-Volatile Configuration Register setting:

- Single Data Rate (SDR) in Standard SPI and Octal SPI using 3-Byte Address Mode
- Single Data Rate (SDR) in Standard SPI and Octal SPI using 4-Byte Address Mode
- Octal Double Data Rate (ODDR) restricted with 4-Byte Address Mode only

The operational IO Mode Configuration is shared by the following commands related to read/program/erase memory and read/write to registers. After power up, the device operation is configurable by writes to the Volatile Configuration Register that is reflected into the Internal Configuration Register; and the device operates instantly based on the written Volatile Configuration Register values settings without the need of a reset or power cycle. A change in the configuration settings using the Non-Volatile Configuration Register will need a power cycle or a reset to take effect. Detailed information on Non-Volatile/Volatile Configuration Register settings and related commands are covered in Sections 7.4, 7.5, 9.3.5, and 9.3.6.

6.2 Extended SPI – Single Data Rate (SDR) Bus Interface

The W35T51NW supports standard SPI, Octal SPI, and Octal SPI with Address/Data Output DDR interfaces. The Extended SPI (SDR) protocols start with a single bit SPI command input. Depending on the command being used, it can transition to single, octal, single DDR or octal DDR during the address and data transmission. The SDR Bus interface (SPI/OSPI/OSPI DDR) requires the Non-Volatile/Volatile Configuration Register Address 00h to be set to either FFh with DS or DFh without DS (see Non-Volatile Configuration Register and Volatile Configuration Register section for details).

6.2.1 Standard SPI Commands

The W35T51NW is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input Output 0 (IO0 / Input only) and Serial Data Input Output (IO1 / Data Output only). Standard SPI commands use IO0 as an input pin to serially write commands, addresses or data to the device on the rising edge of CLK. The IO1 pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 is the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS. Note that Mode 3 is only supported in the SDR interface and not during ODDR.

6.2.2 Octal SPI (OSPI) Commands

The W35T51NW supports Octal SPI (OSPI) operation when using commands such as “Fast Read Octal Output (8Bh / 7Ch)”, and “Fast Read Octal I/O (CBh / CCh)”. These commands allow data to be transferred to and from the device up to eight times the rate of an ordinary SPI Serial Flash. The Octal Read commands offer a significant improvement in random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Octal SPI commands IO0 and IO1 become bidirectional IO pins; /WP pin becomes the bidirectional IO2 pin; IO3, IO4, IO5, IO6, and IO7 pins also become bidirectional; that comprise a total 8-pin (byte-wide) of synchronous data IO.

6.2.3 DDR OSPI Read Commands (1-1d-8d and 1-8d-8d SDR Mode)

To effectively improve SPI/OSPI read operation throughput without increasing the serial clock frequency, The W35T51NW introduces multiple Double Data Rate (DDR) Read during the address input and data output phase of the command sequence supported in SPI/OSPI DDR Read commands. The byte-wide single bit command code is still latched into the device on the rising edge of the serial clock similar to all other SPI/OSPI commands. Once a DDR command code is accepted by the device, the address input and data output will be latched on both the rising and falling edges of the serial clock. The DDR OSPI command is 9Dh (1-1d-8d), and the DDR OSPI I/O command is FDh (1-8d-8d).

6.3 Octal Double Data Rate (ODDR) Bus Interface

The W35T51NW supports an Octal Double Data Rate (ODDR) bus interface. The ODDR protocol starts with an 8-bit (byte-wide) synchronous bus interface on both the rising and falling edge of CLK (DDR) from the command input, address input and data input/output sequences. When in ODDR mode, all commands are supported in DDR mode sequence that maximizes data transmission to meet Execute-in-Place (XIP) type code or data execution. The ODDR Bus interface mode requires the Non-Volatile/Volatile Configuration Register Address 00h to be set to either E7h with DS or C7h without DS (see Non-Volatile Configuration Register and Volatile Configuration Register section for details).

6.4 3-Byte / 4-Byte Address Modes

The W35T51NW supports two types of Address Modes – 3-Byte or 4-Byte Addressing in SDR mode. 3-Byte Address Mode is backward compatible with older generations of serial flash memory that only support up to 128M-bit of data. Using a 3-byte address to start a read in the lower 128Mb region, a user can read to the end of the 512Mb array and then wrap-around back to address-0. 3-byte address program or erase functions are limited to the lower 128Mb. The 4-Byte Address Mode is designed to support Serial Flash Memory devices from 256M-bit to 32G-bit. In ODDR mode, only the 4-byte Address mode is supported where Non-Volatile Configuration Register Address 00h (NVCR-IOC) or Volatile Configuration Register Address 00h (VCR-IOC) setting is E7h or C7h (ODDR mode).

If the NVCR-IOC setting is in SDR mode, the default Address mode setting from power up is based on the Non-Volatile Configuration Register Address 05h (NVCR-AM) value transferred to the Volatile Configuration Register Address 05h (VCR-AM). If the Non-Volatile/Volatile Register value is FFh (factory default), the 3-Byte Address mode is enabled. If the Non-Volatile/Volatile Register value is FEh, the 4-Byte Address mode is enabled. The Non-Volatile Address Mode Configuration Register is configurable by the Write Non-Volatile Configuration Register which takes into effect after a reset or power-up. The Volatile Configuration Register is configurable by Write Volatile Configuration Register which takes into effect on the fly.

Another method to switch between 3-Byte or 4-Byte Address Modes is by using the “Enter 4-Byte Mode (B7h)” or the “Exit 4-Byte Mode (E9h)” commands. Enter 4-Byte Mode or Exit 4-Byte Mode commands are detailed in the Commands and Command Cycles sections.

If the Non-Volatile Configuration Register Address 00h setting is in ODDR mode, the device is automatically set as 4-Byte Address mode after power up. The Address mode setting of the Non-Volatile Configuration and Volatile Configuration Register Address 05h will be ignored, although the Non-Volatile Configuration Register Address 05h setting is transferred to the Volatile Configuration Register Address. The value of the Volatile Configuration Register Address 05h will be activated if the IO Mode Configuration is switched to SDR mode on the fly.

The current operating address mode status is always shown by the Flag Register Address Mode Flag (AMF) Bit 0 (F0). When AMF bit = ‘0’, the device is in 3-Byte Address Mode. When AMF bit = ‘1’, the device is operating in 4-Byte Address Mode. Any valid changes on the Address mode setting either by a command sequence, writes to VCR-AM, or switching the IO Mode Configuration will trigger a status update on the AMF bit. The following conditions are valid operating modes that can update the AMF bit: a) SDR mode using either command sequence or writes to VCR-AM; b) switching the IO Mode Configuration from ODDR mode to SDR (or vice versa) if the VCR-AM address 05h is in 3-Byte address setting.

6.5 Execute-in-Place (XIP) Mode

The Execute-in-Place (XIP) mode takes full advantage of the synchronous 8-I/O data lines by eliminating the Command opcode during read access. This reduces the random memory access time by just sending either a 3-Byte or 4-Byte Address and the dummy cycles synchronously before the data output shifts out on the IO pin(s).

The device enters XIP mode either by the Non-Volatile Configuration Register Address 06h (NVCR-XIP Configuration) setting from power- up or reset, or by configuring the Volatile Configuration Register Address

06h (VCR-XIP Configuration) to enable XIP mode after power-up. When the device is in XIP mode, it will not recognize any commands as the device expects a valid synchronous Address and Dummy Cycle input sequence once the device is activated (/CS pin asserted), it will then start shifting out the data stream from the target address input. XIP mode has to be exited before valid commands are recognized and acknowledged by the device. XIP mode is terminated by setting the XIP Mode bit to '1' in the read command sequence (XIP mode bit is discussed in more details in the XIP Mode Bit section).

Once the device XIP setting is exited or if the device starts with XIP disabled from power-up or reset and the host requires operation in XIP mode, the XIP mode is enabled or disabled by configuring the VCR-XIP Configuration. Once it is enabled, enter/exit XIP mode is controlled/performed using the Read Command, Address and the XIP Mode Bit sequence.

6.5.1 XIP Mode Bit

If XIP mode is enabled either through NVCR-XIP or VCR-XIP Configuration, the XIP Mode bit (XMb) is the first IO0 bit input of the Dummy Cycle after the last Address Byte or Bit input in the read sequence. The state of XIP mode bit during the current input sequence controls and determines whether the device remains in XIP mode or exits the XIP mode on the next /CS pin assertion. If XMb is '0', the device will remain in XIP mode. If XMb is '1', the device exits XIP mode with /CS de-assertion and will expect valid command based sequences with the command input on the next /CS assertion.

6.5.2 NVCR-XIP Configuration

XIP Mode Entry from Power cycle or Reset

The Non-Volatile Configuration Register Address 06h (NVCR-XIP Configuration) controls the device XIP configuration from power-up or reset. The default NVCR-XIP Configuration value from the factory is 'FFh' and in this setting, XIP is disabled. Other defined NVCR-XIP values such as FEh, FDh, or F8h, will set the device in XIP mode (check the NVC-Register for detailed XIP settings). If the device NVCR-XIP Configuration is in XIP mode from power-up or reset, the device expects Address and Dummy Cycle input (no need for Command Code) for direct boot access to the stored code or data in the flash. If the DS pin is enabled, DS pin toggling signals the data output transition from the starting target address and incremented by the CLK input sequentially. Once the device is powered-up and if the XMb input is driven to '1' during an XIP read access, the device exits XIP mode when /CS is de-asserted. While the power is on, re-entering XIP can be achieved by using the Volatile Configuration XIP Configuration setting method. Performing a power cycle or reset will bring the device back to the NVCR-XIP mode configuration.

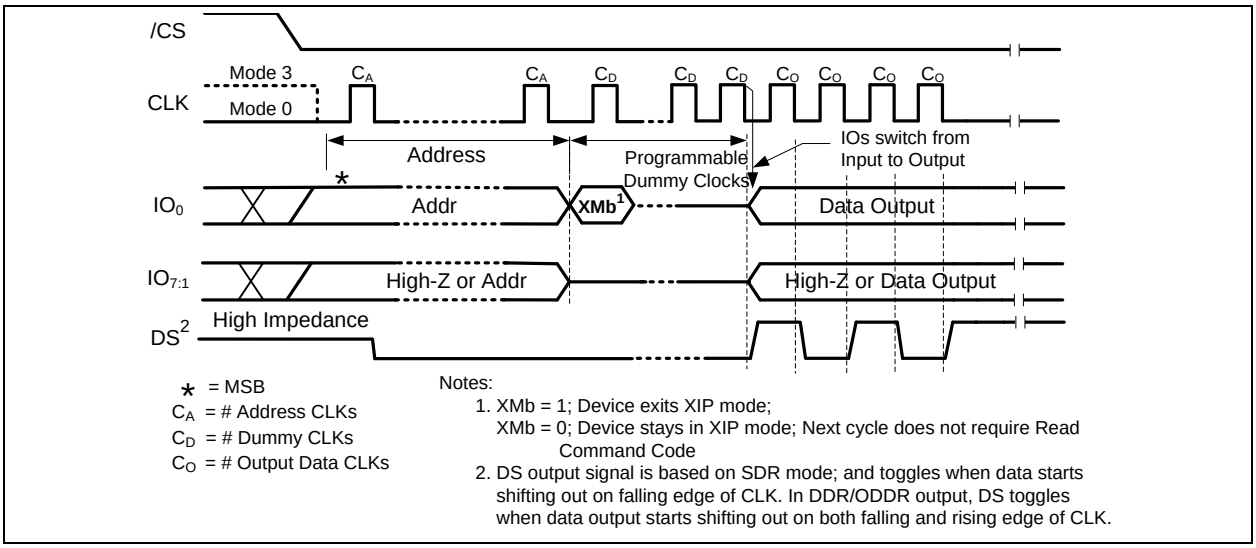


Figure 4-2. XIP Mode Entry from Non-Volatile Configuration Register Address 06h (NVCR-XIP)
(From Power-up, Reset or next XIP read cycle when XMb=0 from previous XIP read cycle)

6.5.3 VCR-XIP Configuration

The device can switch back and forth from normal operating mode to XIP configuration using the Volatile Configuration Register XIP Configuration (VCR-XIP) Address 06h. The default value from power up or reset of the VCR-XIP is 'FFh', with XIP being disabled. To enable XIP mode using VCR-XIP, first write 'FEh' on VCR-XIP, then issue a Fast Read command and drive XMb to '0' on IO0 during the dummy cycle input sequence. If the DS pin is enabled, DS pin toggling signals the data output transition from the starting target address and incremented by CLK input sequentially. This will place the device in XIP mode once the /CS pin is driven high and on the next read memory cycle, only the Address and Dummy Cycle input is required on /CS assertion (Read Command opcode is not needed). However, the device will not recognize and execute valid commands in XIP mode. To exit XIP mode, the XMb has to be driven to '1' on the next XIP read sequence and VCR-XIP is automatically set to 'FFh' disabling the XIP mode. To enable XIP again by VCR approach, write 'FEh' data to VCR-XIP and start a Fast Read command (C-A-D) with XMb=0.

The supported XIP mode read commands are Octal DDR Read commands (all read commands except for 03h and 13h); Fast Read SDR commands SPI Read (0Bh/0Ch), Octal SPI (8Bh / 7Ch), and Octal I/O (CBh / CCh); and Fast Read DDR Single-Address-Input and Octal Output (9Dh) and Fast Read DDR Octal I/O (FDh) commands. The device can enter XIP mode via VCR-XIP when the device is in Program/Erase Suspend mode.

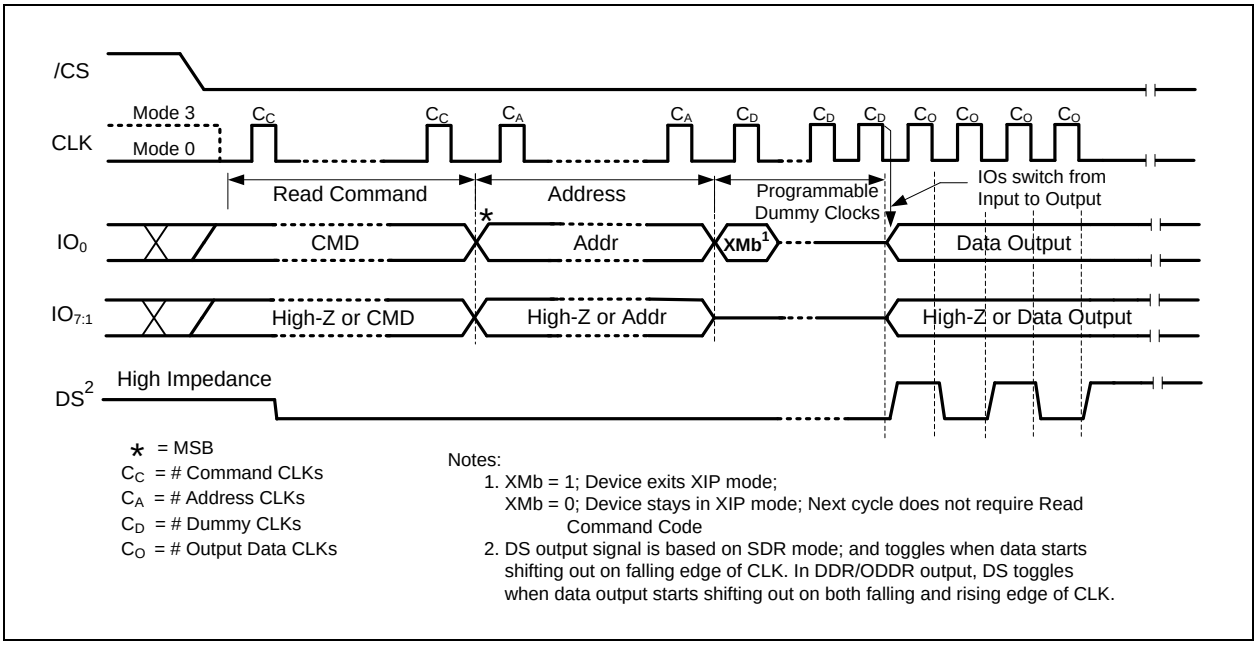


Figure 4-3. XIP Mode Entry From Volatile Configuration Register Address 06h (VCR-XIP)

6.5.4 Exit XIP Recovery Sequences after Host and Device Synchronization Error

When the device is in XIP mode, there is no way to determine the current operating status of the device except when the device exits XIP mode; then device can accept normal command operations (Command-Address-Data). When XIP mode is used in an application, there can be instances where the interface between the controller and device gets out of sync. This out of sync incident could be due to accidental reset or power disruption of the interfacing host controller or multiple host controllers with different I/O mode configuration access to the device. in these cases, a way to exit XIP mode is by setting the XMb to '1' during XIP Mode read memory access.

Due to the number of I/O Mode Configurations, and the number of sequences the device supports in XIP mode (ODDR Read, Octal SPI 3-Byte and 4-Byte Address, and SPI with 3-Byte and 4-Byte Address), a specific exit sequence to start with the least number of CLK input sequence is recommended first and the most number of CLK input sequence is last. This specific sequence is required to Exit XIP due to possible bus contention risk when the device's actual XIP configuration setting (I/O Mode, Address and Dummy cycle sequence) is shorter than a longer or longest XIP read memory sequence.

A case example is by comparing XIP ODDR Read and XIP SPI with 4-Byte Address number of CLK cycles (using 16 CLK Dummy Cycles) before data output. XIP ODDR Read may start shifting out data after 19th CLK on both falling and rising edge of CLK (Number of CLK count is from 1). If IO0 is being driven high or low as an input during this period until the 33rd CLK using SPI with 4-Byte Address sequence, then the bus contention on IO0 will be imminent when the data starts shifting out after the 19th CLK.

The required sequence on exiting XIP mode by setting XMb to '1' is defined using the exact sequence from 'a' to 'e'. This sequence does not reset or interrupt any ongoing operations. Once XIP is exited, the host controller can perform a Software Reset sequence to reset the device.

a) Drive /CS pin low; drive IO0 high ('1') for a duration of 3 CLK cycles; and drive /CS pin high before the 4th CLK (XIP-ODDR). This is followed by the next sequence b.
b) Drive /CS pin low; drive IO0 high ('1') for a duration of 4 CLK cycles; and drive /CS pin high before the 5th CLK (XIP-OSPI with 3-Byte Address). This is followed by the next sequence c.
c) Drive /CS pin low; drive IO0 high ('1') for a duration of 5 CLK cycles; and drive /CS pin high before the 6th CLK (XIP-OSPI with 4-Byte Address). This is followed by the next sequence d.
d) Drive /CS pin low; drive IO0 high ('1') for a duration of 25 CLK cycles; and drive /CS pin high before the 26th CLK (XIP-SPI with 3-Byte Address). This is followed by the next sequence e.
e) Drive /CS pin low; drive IO0 high ('1') for a duration of 33 CLK cycles; and drive /CS pin high before the 34th CLK (XIP-SPI with 4-Byte Address).

The above sequence is illustrated in Figure 4-4 below. This sequence will only exit indeterminate XIP mode by setting XMb to '1'. It does not reset the device or interrupt an ongoing internal Program/Erase operation. After terminating XIP mode, the host controller should regain control of the interface and perform the required operations either by doing further interface recovery, power loss recovery, software reset sequence or hardware reset for full device recovery.

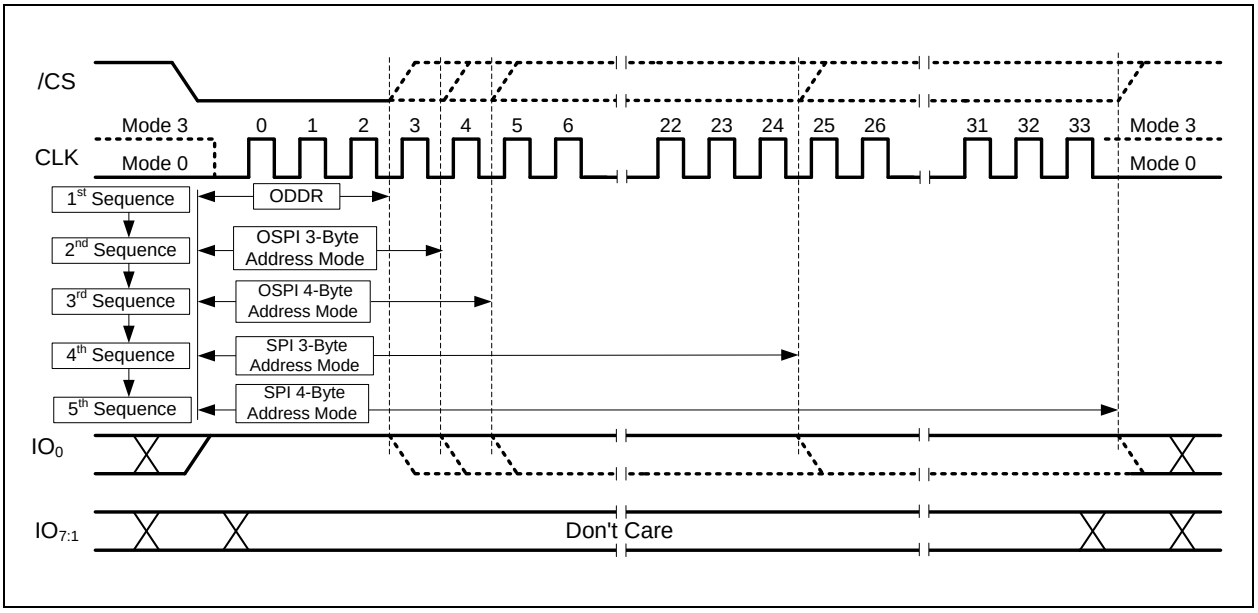


Figure 4-4. Exit XIP Sequence

6.6 Fail/Safe Power-up Detection and Interface Recovery

The W35T51NW supports a hardware mechanism that detects possible power on reset initialization success or failure. If a POR failure occurs, there are steps to detect if the failure is permanent or recoverable by power cycling. Repeated recovery attempt failures gives system designers the option to detect a permanent power-up defect.

There are certain situations in which the device operation can hang-up and become out of sync with multiple host MCUs. While performing critical operations, the device can be interrupted by accidental power loss or I/O configuration corruption caused by one of the unstable host MCUs. In these instances, the device can go to an indeterminate state of I/O Mode configurations, settings, and interfaces the device supports. To regain communication with the device, there are methods that can restore the predefined settings outlined in the next sections.

6.6.1 Fail/Safe Power up Detection

During power-up, the device goes through a power on reset process (POR) that performs internal initialization steps including the setting of the I/O configuration. Within the POR process, each step during the initialization is monitored. The monitored POR initialization steps will determine either success or failure of the POR process. When the device comes out of POR, a POR success or failure flag is reflected on the hardware /RSTO pin after power up completion. The combination of the /RSTO pin state and the values of BUSY bit, the WEL bit and the Ready Flag (RF) will indicate whether the power-up process is normal or a POR initialization failure has occurred.

After power-up and during device operations, a stable power supply on Vcc is required to maintain normal operations. A voltage drop on Vcc below the V_{PWD} level may trigger the power on reset initialization steps. It is also required that if Vcc drops below V_{PWD}, a minimum t_{PWD} time to ensure the device gets re-initialized properly. Once the Vcc ramp up is resumed and as Vcc is restored to its normal operating level, the device will go through the same power on reset initialization steps again.

After POR, the hardware /RSTO pin will determine the fail/safe status of the power-up initialization process. If device initialization is successful during power-up or power on reset, the /RSTO pin will transition from low to high impedance state and the device can resume normal operations. If the device initialization fails including possible incorrect I/O configuration during power-up, the /RSTO pin is continuously driven low after the device gets out of reset.

The Status Register's Busy bit and the Flag Register's Ready Flag bit will also capture the fail/safe status of the power up initialization. After a successful power on reset, the device can resume with normal operations – BUSY=0, WEL=0, and RF=1. If POR initialization failure occurs, it may be possible the I/O configuration is corrupted and an access to the Status Register and Flag Register will fail to read valid data. In this case, an Interface Recovery is an option to recover the default interface.

In the case of a POR failure, the /RSTO pin is continuously driven low, BUSY=1, WEL=0, and RF=0 after a power-up. The device will not be able to resume normal operations such as read, program or erase memory. A re-initiation of a power off and on cycle on the device is required to check if the power-up initialization failure is permanent or it can be recovered accordingly. A repeated occurrence of the power-up initialization error may indicate the device exhibits a permanent type of failure, may not be fully functional, and requires to be checked/tested. A software reset, hardware reset, or a JEDEC Hardware Reset initiated to the device will not re-initialize the POR steps; the reset(s) will only clear the POR status failure, and checking/reading back the /RSTO pin and BUSY, WEL, and RF bits after reset will display the wrong device POR state (false status).

6.6.2 Interface Recovery based on Non-Volatile Configuration Settings

The device can perform a two-step method for interface recovery if the device Non-Volatile Configuration Register setting is known to be preserved and reliable from a previous successful power up cycle or reset. This specific two-step method will only restore the predefined interface setting from the Non-Volatile Configuration Register states and transfer them to the Volatile Configuration Register state which will reflect on the device operation. There is no reset of the device nor any interruption to any ongoing operations. The recommended two-step method for interface recovery is shown below -

- The first step is to execute the Exit XIP Recovery Sequence as detailed on Section 6.5.4 and Figure 4-4 (on the previous section). This is a five step method in exiting XIP mode by driving IO0 to '1' until XIP Mode Bit (XMb) is passed on each of the supported XIP IO Mode Configurations (ODDR, OSPI with 3-Byte or 4-Byte Address, and SPI with 3-Byte or 4-Byte Address).
- The second step is to restore the Non-Volatile Configuration setting to the Volatile Configuration Register state to be the active interface mode. This is performed by driving the /CS pin low, followed by driving IO[7:0] pins high ('FFh') for 16 CLK cycles, and subsequently driving the /CS pin high before the 17th CLK activates the Non-Volatile Configuration Register setting to the Volatile Configuration Register. Figure 4-5 illustrates the Interface Recovery Sequence.

This two-step step method must be executed in the defined order and tSHSL2 must be at least 30ns for the duration of each sequence.

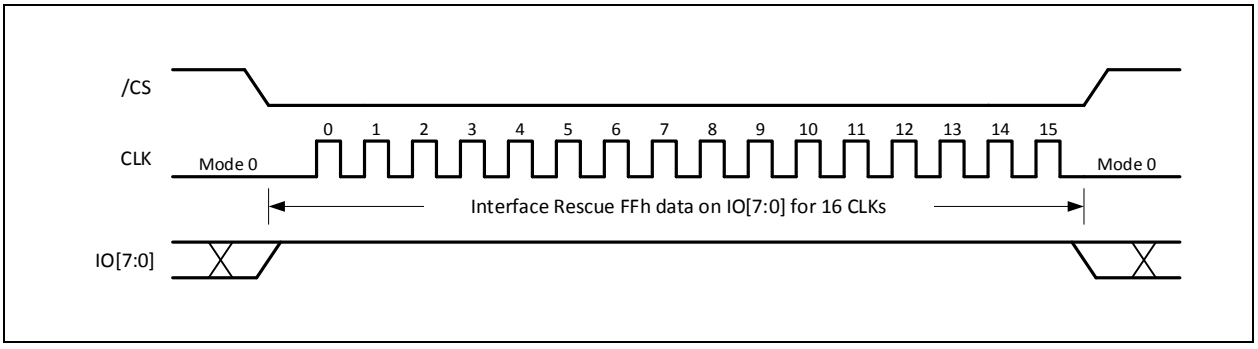


Figure 4-5. Interface Recovery Sequence

6.6.3 Power Loss Interface Recovery

If power interruption happens during a Write Non-Volatile Configuration Register command cycle (on IO Mode Configuration, XIP Mode Configuration, others), chances are the device powers up in an indeterminate state with the Non-Volatile Configuration being corrupted. In this condition, the device must be restored to a predefined SDR state based on the reset default settings of the Volatile Configuration Register.

A second method is based on power loss recovery primarily when Write to Non-Volatile Configuration Register is accidentally interrupted by a power glitch. This is also a two-step method that will restore interface operations based on the reset setting of the Volatile Configuration Register that will be reflected on the device operation. There is no reset on the device nor any interruption to ongoing operations. The recommended two-step method for interface recovery is shown below -

- The first step is to execute the Exit XIP Recovery Sequence as detailed in Section 6.5.4 and Figure 4-4 (on the previous section). This is a five step method used to exit XIP mode by driving IO0 to '1' until XIP Mode Bit (XMb) is passed on each of the supported XIP IO Mode Configurations (ODDR, OSPI with 3-Byte or 4-Byte Address, and SPI with 3-Byte or 4-Byte Address).
- The second step is to restore and reset the Volatile Configuration Register setting to the default power on state to be the active interface mode. This is performed by driving the /CS pin low, followed by driving IO[7:0] pins high ('1') for 8 CLK cycles, and subsequently driving the /CS pin high before the 9th CLK activates the device operation based on the Volatile Configuration Register power on reset setting (IO mode configuration is in SDR mode). Figure 4-6 illustrates the Power Loss Interface Recovery Sequence.

This two-step method must be executed in the defined order and tSHSL2 must be at least 30ns for the duration of each sequence. After the interface recovery is completed, it is recommended to issue and complete the interrupted Write Non-Volatile Configuration Register settings to properly setup the power on state configuration mode configuration of the device. Note that only Mode 0 is supported.

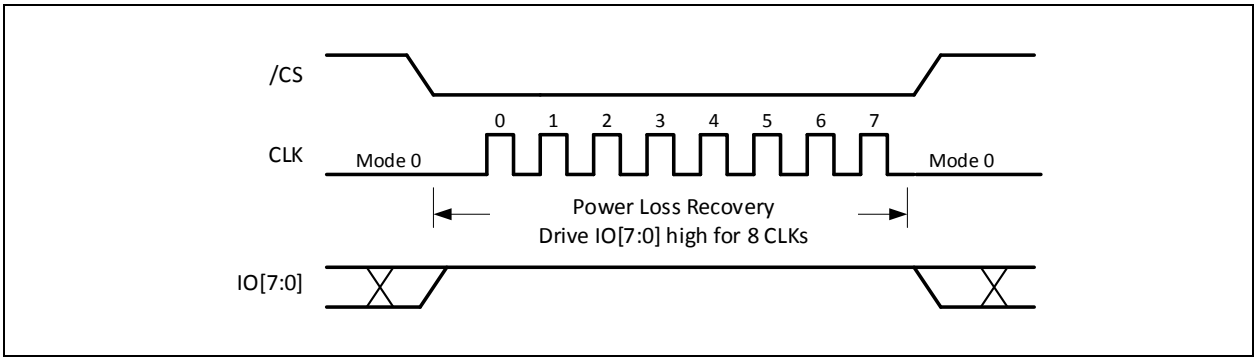


Figure 4-6. Power Loss Interface Recovery

6.7 Data Learning Pattern (DLP)

The W35T51NW supports a data learning pattern stored in the Data Learning Pattern (DLP) Register. The data learning pattern can be utilized by the host as a benchmark in validating data transfers across the 8-I/O interface at higher frequencies of >133MHz in SDR and >66MHz in ODDR mode. The benchmark data is a set of predefined data pattern that is used for read validation at the higher speeds. The device can transmit a minimum of 128 CLK cycles (SDR mode) or 64 CLK cycles (ODDR mode) of data bits containing either 16 or 128 Bytes on the data lines depending on the IO Mode Configuration settings of SDR or ODDR. Based on the sampling validation results, the host controller can fine-tune the trigger test point for the I/O data lines to offset the timing variation required by a given application.

Every application has specific board level loading characteristics and the loading effect causes system propagation delay that can result in error during data transfers and sampling of data by the host. Tuning the Data Learning Pattern can be a useful tool in this area, since it can calibrate a window for latching in valid data.

The DLP Register is a 256-byte register from address 00h to FFh. The W35T51NW supports specific DLP commands to access the DLP Register in SDR/ODDR mode:

- Read DLP (23h, 8Ch, 9Ch)
- Program DLP Register (40h, 78h)
- Erase DLP Register (B8h)

The DLP Register is pre-programmed with non-volatile data from the factory. The DLP Register is read accessible by Read DLP commands (23h, 8Ch, 9Ch). Wrap-around to the lowest memory is supported when highest address byte location is reached during read DLP. The pre-programmed data covers most of the worst case output mode transitions. The non-volatile data pattern is erasable and user can program it with a customized pattern fitting their application. The pre-programmed pattern is the same as the *e*·MMC HS200 standard twice. The following is a pre-programmed tuning data learning pattern:

- FF0F FF00 FFCC C3CC C33C CCFF FEFF FEEF
- FFDF FFDD FFFB FFFB BFFF 7FFF 77F7 BDEF
- FFF0 FFF0 0FFC CC3C CC33 CCCF FEFF FFEE
- FFFD FFFD DFFF BFFF BBFF F7FF F77F 7BDE
- FF0F FF00 FFCC C3CC C33C CCFF FEFF FEEF
- FFDF FFDD FFFB FFFB BFFF 7FFF 77F7 BDEF
- FFF0 FFF0 0FFC CC3C CC33 CCCF FEFF FFEE
- FFFD FFFD DFFF BFFF BBFF F7FF F77F 7BDE

DLP Register is readable, programmable, and erasable by the corresponding Read DLP, Program DLP Register, and Erase DLP commands. The DLP sequence is initiated with a command, 24/32-Bit address, and with or without data input/output depending on the initiated command. Please refer to Section 9.13 Data Learning Pattern Commands for detail command sequences.

6.8 ECC Operation

Error Correction Codes (ECC) is a commonly used technique in non-volatile memory to reduce the device Bit Error Rate (BER) and to improve device reliability during the lifetime of the device. To achieve error detection and correction, redundancy data must be added to store the ECC calculation results for a given length of data. In W35T51NW, the ECC calculation is done per aligned 16-byte memory address range partition (LSB A[3:0] = 0000b to 1111b) from the lowest address (00000000h) to the highest memory address (03FFFFFFh). Every byte, up to 16 bytes of memory data being programmed in the aligned 16-byte memory address array is checked by the internal ECC engine using Single Error Correction (SEC) and Double Error Detection (DED). Using 16-Byte ECC data granularity, ECC calculation latency time is minimized, while preserving the highest level of data integrity.

The W35T51NW supports two ECC registers, the ECC Status Register and the 8-byte Advanced ECC Register. The ECC Status Register has an ECC bit (ER2) to enable and disable ECC operations and Single Error Correction (SEC), Double Error Detection (DED), Interrupt (INT), and ECC On/Off (ECCO) bits to monitor ECC events. The ECC function of the device is enabled by setting the ECC bit to '1' (default) in the ECC Status Register (ER2). When the ECC bit is cleared to '0', ECC functionality for the memory array read is disabled. The Advanced ECC Register supports the detection of ECC events at a target memory address, along with the capability to detect ECC status of each of the aligned 16-byte memory. The Advanced ECC Register has the SEC Address Captured Valid Flag (SACVF), ECC On/Off Flag (ECCOF), SEC Flag (SECF), DED Flag (DEDF), SEC Register Address, SEC Counter, DED Address Captured Valid Flag (DACVF), DED Register Address, and DED Counter.

The default value of all memory data is FFh (Erased) when the device is shipped from the factory. A "Page Program" or an "Octal Page Program" (02h, 12h, 82h, 84h, C2h, 8Eh) command can be used to program the user data into the memory array. Whether the ECC Enable bit is enabled (ECC=1) or disabled (ECC=0), ECC calculation is performed during internal programming operations and the results are stored in the redundancy or spare area of the memory array. Error correction codes are calculated and stored based per 16-byte aligned address boundaries from LSB address A[3:0] = 0000b to 1111b and applicable across the full memory. The number of programming attempts are also tracked and monitored per aligned 16-byte memory. Every aligned 16-byte memory should only be programmed once with one byte up to 16 bytes of data, so ECC functionality (ECC On status or flag) will be maintained. If any of the aligned 16-byte memory is programmed more than once, the ECC functionality of those affected (targeted) 16-byte aligned memories will automatically be turned off (ECC Off status or flag) on read operations. Programming more than once on the same location from a single bit alteration up to the aligned 16-byte segment is accepted except the ECC functionality will automatically be turned off (ECC Off status or flag) during memory reads. ECC On/Off status is shown by ECC On/Off (ECCO) status bit of the ECC Status Register and ECC On/Of Flag (ECCOF) bit of the Advanced ECC Register. An erase operation on 16-byte aligned memory locations with ECC Off status will get back the ECC On status after erase completion.

When ECC is active on an aligned 16-byte memory, read memory access to this address location is perform with the aid of the internal ECC engine which will check the ECC results stored in the spare area and apply necessary error correction or error detection to the memory array data being read out. The Single Error Correction (SEC) and Double Error Detection (DED) Bits in the ECC Status Register provides ECC status after the last Read operation to determine if the read out data has any errors or not. A Read operation can start from any byte address and continue through the entire memory array, it is not necessary to align the 16-Byte granularity boundary address to start a Read command. When ECC is inactive (disabled) on an aligned 16-byte memory, during read memory operations, read access will be directly to the memory array location without any internal ECC check for error correction or detection.

Hardware monitoring of the ECC status can also be used to detect ECC status in real time during any data output. When configured by setting INT bit of ECC Status Register (ER1) to either '0' for SEC event or '1' for DED event, the /INT (Interrupt Output) pin will be pulled low during any aligned 16-Byte data output if it contains SEC or DED events.

Additionally, an 8-byte Advanced ECC Register can also detect the ECC status of each 16-byte aligned memory across the full memory. The ECC status that can be checked on the target 16-byte aligned memory

address and successive 16-byte aligned memory includes: 1) status of ECC functionality if active or turned off (ECCOF); 2) single bit error correction event flag (SECF); 3) double bit error detection event flag (DEDF). The Advanced ECC Register can also capture the first SEC and DED events addresses, counters, and valid captured SEC and DED addresses flags from previous memory read operations.

6.9 Cyclic Redundancy Check (CRC)

The W35T51NW supports two types of Cyclic Redundancy Check (CRC). They are CRC-At-Rest for stored memory data and real-time CRC during high speed data transmission. The CRC-At-Rest assists in detecting data integrity of stored memory in advance providing an internal method in determining the integrity (stable or corrupted) of the stored data. Separately, the CRC-In-Transit aids in correcting data transmitted by means of parity check during real-time transfer.

6.9.1 CRC-At-Rest

The W35T51NW supports Cyclic Redundancy Check (CRC) at rest operation to detect abnormal changes to the programmed data during programming or after a period of time to check data integrity. The CRC calculates a fixed length 64-bit CRC code binary sequence (8-byte) for a certain range of data or the full range of the memory by using a CRC-64 polynomial equation. It is a higher performance option in verifying programmed data compared to the direct memory read access.

In the device, the 64-bit CRC code is calculated/captured internally after running a dummy CRC-At-Rest Memory command sequence targeting either the full memory or a memory range. It is stored in the CRC Register. The 64-bit (8-byte) CRC code reference in the CRC Register is read by using the Read 8-Byte CRC Code (1Bh) command. The 64-bit (8-byte) CRC code can be stored separately and can be used for comparison during the initiation of the CRC-At-Rest command. There is no special system hardware required to use CRC-At-Rest.

The CRC-64 operation follows the ECMA standard. The generating polynomial is:

$G(x) = x64 + x62 + x57 + x55 + x54 + x53 + x52 + x47 + x46 + x45 + x40 + x39 + x38 + x37 + x35 + x33 + x32 + x31 + x29 + x27 + x24 + x23 + x22 + x21 + x19 + x17 + x13 + x12 + x10 + x9 + x7 + x4 + x + 1$

Note: The data stream sequence is from LSB to MSB and the default initial CRC value is all zeros.

The device CRC-At-Rest operation generates the 64-bit CRC result of an address range up to the full memory depending on the executed command sequence. The 64-bit (8-byte) CRC result is then compared to the expected 64-bit CRC data that is used as an input in the CRC command sequence. The Flag Register Bit 4 (PF) is the status flag that signals whether the CRC operation passed or failed. If the CRC operation failed, a proper corrective action can be taken by either verifying with a normal read operation and/or performing erase/re-programming of the memory array.

The CRC command sequence for full memory range and selected address range are shown in the tables below.

CRC Command on Full Memory Range:

Command Sequence		Description
Number of Bytes	**Data Input**	
Assert /CS pin from High to Low		Start of a Command sequence
1	9Bh	CRC-At-Rest command opcode; Activate CRC
2	27h	CRC-At-Rest sub-command opcode
3	FFh	CRC operation memory range (FFh = Full Memory)
4	CRC[7:0]	1st byte of CRC Reference (expected) code value
5-10	CRC[55:8]	2nd to 7th byte of CRC Reference (expected) code value
11	CRC[63:56]	8th byte of CRC Reference (expected) code value
De-assert /CS pin		Initiate CRC operation; CRC operation starts

CRC Command on Partial Memory Address Range:

Command Sequence		Description
Number of Bytes	Data Input	
Assert /CS pin from High to Low		Start of a Command sequence
1	9Bh	CRC-At-Rest command opcode; Activate CRC
2	27h	CRC-At-Rest sub-command opcode
3	FEh	CRC operation memory range
4	CRC[7:0]	1st byte of CRC Reference (expected) code value
5-10	CRC[55:8]	2nd to 7th byte of CRC Reference (expected) code value
11	CRC[63:56]	8th byte of CRC Reference (expected) code value
12	Start Address [7:0]	Start Address of the CRC operation
13 to 14	Start Address [23:8]	
15	Start Address [31:24]	
16	Stop Address [7:0]	Stop Address of the CRC operation
17 to 18	Stop Address [23:8]	
19	Stop Address [31:24]	
De-assert /CS pin		Initiate CRC operation; CRC operation starts

6.9.2 CRC-In-Transit Mode

CRC-In-Transit mode is only supported in ODDR mode on selected commands. CRC-In-Transit is entered by either the Non-Volatile Configuration Register Address 04h (NVCR-CRC) or Volatile Configuration Register Address 04h (VCR-CRC) settings.

In CRC-In-Transit mode, there are selected commands (detailed in Section 9.14.2 CRC-In-Transit Mode) that requires a 2-byte CRC field in the command sequence during the input, output, or both input/output cycle sequences. The exact locations in the command sequence of the 2-Byte CRC Input/Output Fields are detailed on Section 9.14.2 CRC-In-Transit Mode Timing diagrams. The 2-byte CRC field is actually a transfer of a calculated byte size bitwise exclusive-OR (XOR) operation of the data before the CRC field that is either shifted in or shifted out. The CRC field uses the rising and falling edge of clock during input, while the falling and rising edge of clock during output. Thus, it becomes a calculated 2-byte CRC field value shifted two times.

During read and program memory operations in CRC-In-Transit mode, the CRC data size can be configured in 16-Byte, 32-Byte, 64-Byte, or 128-Byte partitions by the NVCR-CRC or VCR-CRC Registers settings. The following NVCR-CRC/VCR-CRC Register values indicate the CRC data size configuration: FFh: CRC-In-Transit Disable; F8h: CRC 16-Byte data partition; FAh: CRC 32-Byte data partition; FCh: CRC 64-Byte data partition; and FEh: CRC 128-Byte data partition.

During the supported CRC-In-Transit command input sequence, the byte size CRC Input field is calculated by the bitwise exclusive-OR operation of the data bytes of either the command cycle, command cycle + data cycle, command cycle + address cycle, address cycle only (XIP mode), or a 16/32/64/128 partition of each data input cycle. Separately, read commands with >=8 bytes data output will have 16/32/64/128 byte partition followed by the CRC Output Field, the calculated bitwise exclusive-OR of this data output partition. The CRC-In-Transit input command protocols with the added 2-byte CRC Input/Output Fields are as follows:

- 8d-0-0: Command cycle + CRC Input Field
- 8d-0-8d Write Registers: Command cycle + Data cycle + CRC Input Field
- 8d-8d-8d Write Registers with Address: Command cycle + Address Cycle + CRC Input Field + Data Input
- 8d-8d-0 Erase Commands: Command cycle + Address cycle + CRC Input Field
- 8d-8d-8d Program Commands: Command cycle + Address cycle + CRC Field + Data partition + CRC Field + Data partition in a repeated specified pattern.
- Read Register: Command cycle + CRC Input Field + Dummy cycle + Data Output cycle
- Read Register with Address: Command cycle + Address cycle + CRC Input Field + Dummy cycle

+ Data Output Cycle

- Read ID: Command cycle + CRC Input Field + Dummy cycle + Data Output 16/32/64/128 Byte Partition + CRC Output Field+ Data Output 16/32/64/128 Byte Partition + CRC Output Field… (in repeated data output + CRC Output Field sequence)
- Read (Memory, SFDP, Security Register, CRC Code, and DLP): Command cycle + Address cycle + CRC Input Field + Dummy cycle + Data partition + CRC Output Field + Data partition/CRC Output Field in a repeated specified data output pattern.
- XIP Read Memory:
    - XIP Entry through VCR: Command cycle + Address cycle + CRC Input Field + Dummy cycle with XIP Mode Bit (XMb bit) + Data partition + CRC Output Field + Data partition/CRC Output Field in a repeated specified data output pattern.
    - XIP Mode Entry/Exit: Address cycle + CRC Input Field + Dummy cycle with XIP Mode Bit (XMb bit) + Data partition + CRC Output Field + Data partition/CRC Output Field in a repeated specified data output pattern.

The device can detect an error during the input transmission by the 2-Byte CRC Input Field parity check and the Flag Register CRCTF Flag bit (F3) value. If a CRC-in-Transit error occurs during the input phase, the CRCTF bit is set to '1' indicating a CRC-In-Transit error during the Command input phase. The active command being initiated will not be executed due to this CRC-In-Transit error. A '0' value of the CRCTF bit indicates that the Command input phase has no error.

The data output phase error detection has to be managed by the interfacing controller with the associated 2-Byte CRC Output Field shifted out by the flash after every 16/32/64/128 byte data output partition.

Details of the supported CRC-In-Transit Commands and protocols are shown in Section 9.14.2 CRC-In-Transit Mode.

6.10 Device Operating Modes or States

The W35T51NW supports several active states and within a given active state, can either acknowledge or ignore commands such as read memory/register, program, erase, write register, suspend, or resume. The device states are broken down into several modes/states: XIP state, Standby Mode, Internal Erase Memory, Internal Program Memory, Erase Suspend Memory, Program Suspend Memory, and Internal Write to Non-Volatile Registers (includes NCVR, Security Registers, and others).

The XIP mode state is where the device access is only for read memory, and without the need for a read command code in the read sequence. No commands are recognized by the device when the device is in XIP mode. Standby Mode is when the device is accessible by standard commands. Internal Erase or Program Memory is when erase or program commands were initiated. Erase/Program Suspend are states that halt temporarily the internal erase or program operation. Internal Writes to the non-volatile registers are the program/erase or writes performed to non-volatile registers. While the device is in these operating modes or states, the device may accept or disregard commands, and the following table summarizes these functionalities.

6.10.1 Operating Modes and Allowable Commands

Commands / Operating Mode/State	Read Mem	Read Status/ Flag Reg[1]	Enter VCR-XIP Mode	Read NVCR, VCR[1]	Vol Reg Wr[1,2]	Write/ Prog/ Ers/ Reg[1,3]	Ers Mem[1]	Prog Mem[1]	Ers Sus[15]	Prog Sus[1]	Ers Res[1]	Prog Res[1]
XIP Mode	Yes	No	No	No	No	No	No	No	No	No	No	No
Standby Mode[4] (/CS high - idle)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	No
Internal Erase Mem[1,5]	No	Yes	No	No	No	No	No	No	Yes	No	No	No
Internal Program Mem[1]	No	Yes	No	No	No	No	No	No	No	Yes	No	No
Erase Suspend Mem[1,5]	Yes[7]	Yes	See Note[8]	Yes	See Note[9]	No	No	Yes[10]	No	No[10]	Yes[10]	No[10]
Program Suspend Mem[1]	Yes[7]	Yes	See Note[8]	Yes	See Note[9]	No	Yes	No	No	No	No	Yes
Internal Write to Non-Volatile Registers[6]	No	Yes	No	No	No	No	No	No	No	No	No	No

Notes:

1. Abbreviations/Acronyms: 'Mem' is abbreviation for Memory; 'Reg' is abbreviation for Register; 'Prog' is abbreviation for Program; 'Sus' is abbreviation for Suspend; 'Res' is abbreviation for Resume; 'Vol' is for Volatile; 'Wr' is abbreviation for Write; and 'Ers' is abbreviation for Erase.

   NVCR is Non-Volatile Configuration Register. VCR is Volatile Configuration Register.
2. Write register commands include: Write Volatile Configuration Register, Write Enable, Write Disable, Clear Flag Register, and other Volatile Register writes.
3. Write non-volatile register commands include: Writes Status Register, Write Non-Volatile Configuration Register, Program/Erase Security Register, Non-Volatile Block Lock Register and other Non-Volatile Register writes or erase.
4. Standby Mode indicates the device has the /CS pin high, idle and waiting for valid commands. Note the device can also be in Standby mode in XIP mode configuration, but will not acknowledge valid commands.
5. Only Sector, 32KB Block, and 64KB Block Erase can be suspended. Chip-Erase will not accept the erase suspend command.
6. Internal Non-Volatile writes include: Writes Status Register, Write Non-Volatile Configuration Register, Program/Erase Security Register, and other Non-Volatile Register writes.
7. When the device is in erase or program suspend, Read Memory access to a suspended memory range (sector, sub-block, block, or page) is accepted, but the output data maybe corrupted and undefined. When the device is in erase or program suspend, entry to XIP mode is possible using the VCR-XIP method.
8. XIP mode can only be entered if VCR-XIP is already set (VCR-XIP=FEh) before executing Suspend operations. When the device enters XIP mode in Suspend mode, device will not be able to accept Resume commands. The device has to exit XIP mode through XIP mode bit (XMb=1) during the XIP read sequence (setting VCR-XIP=FFh) before Resume command can be acknowledged. Write to VCR-XIP is not accepted while device is in suspend mode.

9. The device can accept Write Enable, Write Disable, and Clear Flag Register while in Suspend mode. Device will not accept Write Volatile Configuration Register while in Suspend mode.
10. The device can accept Program Memory outside of the suspended memory range while in the Erase Suspend mode. Programming in a suspended memory range is not recommended as it can cause data corruption. The device does not support nested Erase/Program Suspend/Resume operations..

6.11 Software Reset, Hardware Reset, and JEDEC Hardware Reset

The W35T51NW supports 3 reset methods: Software Reset sequence via Enable Reset (66h) and Reset (99h) opcodes, Hardware Reset pin, and JEDEC Hardware Reset. If a software reset or hardware reset is performed while there is any on-going Program/Erase operation, the ongoing operation will be interrupted and data corruption may happen.

6.11.1 Software Reset

The W35T51NW can be reset to the initial power-on state by a Software Reset sequence in either SDR mode or ODDR mode. This sequence requires two consecutive commands: Enable Reset (66h) & Reset (99h). If the command sequence is successfully accepted, the device will take approximately 30uS (t_{RST}) to reset. No command will be accepted during the internal reset period. Refer to Software Reset Command Sequence in the Command Cycles section for details.

6.11.2 Hardware Reset

The W35T51NW also supports a hardware /RESET pin. Driving the /RESET pin low for a minimum period of 50ns (t_{RLRH}) will reset the device to its initial power-on state. While /RESET is low, the device will not accept any commands.

The hardware /RESET pin has the highest priority among all the input signals. Driving the /RESET pin low for a minimum period of 50ns (t_{RLRH}) will interrupt any on-going external/internal operations, regardless of the state of the other SPI signals (/CS, CLK, IOs, and/or /WP). The internal reset will take approximately 30µs (t_{RST}) maximum before it is ready to accept the next command. The Hardware Reset timing diagram is illustrated in Section 10.9 Reset Timing.

6.11.3 JEDEC Hardware Reset

The JEDEC Hardware Reset sequence is another hardware scheme to reset the device to its initial power-on state. The JEDEC Hardware Reset protocol has two phases: Reset Request-Initiation and Internal Reset-Completion.

6.11.3.1 Reset Request-Initiation Phase

The Reset-Initiation Phase of the JEDEC Hardware Reset uses the rising edge of the /CS pin to latch in the data on the IO0 pin. There are 4 required low to high transition pulses on the /CS pin (similar to a synchronous clock signal) with data 5h (0101b) with the most significant bit first. The CLK pin has to remain either low or high (Mode 0 or Mode 3) during the entire Reset Request-Initiation phase. This is to prevent mix-up with standard SPI/OSPI/ODDR synchronous command protocols. After the fourth low to high transition (pulse) on the /CS pin (with data '1' on IO0), an internal reset is triggered.

6.11.3.2 Internal Reset-Completion Phase

Once the reset is triggered internally, the device will not accept any command inputs until the internal reset time (t_{RST}) of 30µs maximum is completed. The JEDEC Hardware Reset timing diagram is illustrated in Section 10.10 JEDEC Hardware Reset Protocol.

6.12 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W35T51NW provides several means to protect the data from inadvertent writes.

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable commands and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Status Register
- Write Protection using Power-down command

Upon power-up or at power-down, the W35T51NW will remain in the reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 19-1). While at reset, all operations are disabled and no commands are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related commands are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register commands. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and the t_{VSL} time delay is reached. It must also track the VCC supply level at power-down to prevent any adverse command sequence. If needed, a pull-up resistor on the /CS pin can be used to accomplish this.

After power-up, the device is automatically in a write-disabled state with the Status Register Write Enable Latch (WEL) bit set to a '0'. A Write Enable command must be issued to set the WEL bit to '1' before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register command will be accepted. After completing a program, erase or write command, the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of '0'.

Software controlled write protection is facilitated using the Write Status Register command and setting the Status Register Protect (SRP) and Block Protect (TB and BP[3:0]) bits of the Status Register. These settings allow a portion or the entire memory array to be configured as read only or protected. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down command offers an extra level of write protection as all commands are ignored except for the Exit Power-down command.

7. REGISTERS

The W35T51NW has a Status Register, Flag Register, Internal Configuration Register, Non-Volatile Configuration Register, Volatile Configuration Register, Device ID Register, SFDP Register, Unique ID, Security Registers, ECC Status Register, Advanced ECC Register, and a DLP Register. The Status and Flag Registers provide status on the availability of the flash memory array: whether the device is write enabled or disabled; the state of write protection; program or erase status and error indicator; erase/program suspend status; write to registers and CRC status; Illegal access monitor on Protected/Security register, and Current Address Mode.

The Internal Configuration Register is an internal register that is accessed only by the Non-Volatile Configuration Register, Volatile Configuration Register, and configuration related Commands. The Non-Volatile Configuration Register sets the device configuration after power-up or reset, and defines the Wrap Configuration, XIP Configuration, Address Mode Configuration, Output Driver Strength, Dummy Clock Cycle, and Bus Interface Mode settings. These non-volatile settings are then transferred to the Volatile Configuration Register, which has the identical configuration/parameters as the Non-Volatile Configuration Register, and the Internal Configuration Register during power up or the reset phase. Any configuration update during the normal operating mode can be performed instantly by initiating Write Volatile Configuration Register which will trigger an update of the Internal Configuration Register and device operating behavior. A Write Non-Volatile Configuration Register will need a power cycle or reset to activate the new configuration.

The Device ID register is expanded with both the 3-Byte JEDEC ID and an additional 3-Byte Device Configuration accessible with the JEDEC ID Read command 9Fh and Read ID command 9Eh. The SFDP Register is 1K-Byte in size and stores predefined configurations, read commands, memory block size, and other parameters. Each device is factory pre-programmed with a 16-byte Unique ID. It supports three 1KB Security Registers that are readable, programmable, or erasable with OTP lock options. The W35T51NW also has two ECC Registers, the ECC Status Register and the Advanced ECC Register, to support bit error detection and correction. The 256-byte DLP Register is also pre-programmed with a pattern used to fine tune the latching of valid data.

7.1 Status Register

The Status Register contains volatile/nonvolatile bits for write protection, volatile write enable required before any write commands, and a write in progress flag. The Write Status Register command is used to configure the device write protection features of the volatile/nonvolatile Status Register SRP, TB, and BP[3:0] bits. Write access to these Status Register bits is controlled by the Status Register Protect Bit 7 (SRP), the Write Enable command, and the state of the /WP pin. The Volatile WEL bit is set/cleared by the Write Enable command and the Write Disable command, or a program/erase/register write completion. The Status BUSY bit is a flag that provides the internal program, erase, register write or CRC-At-Rest operation status.

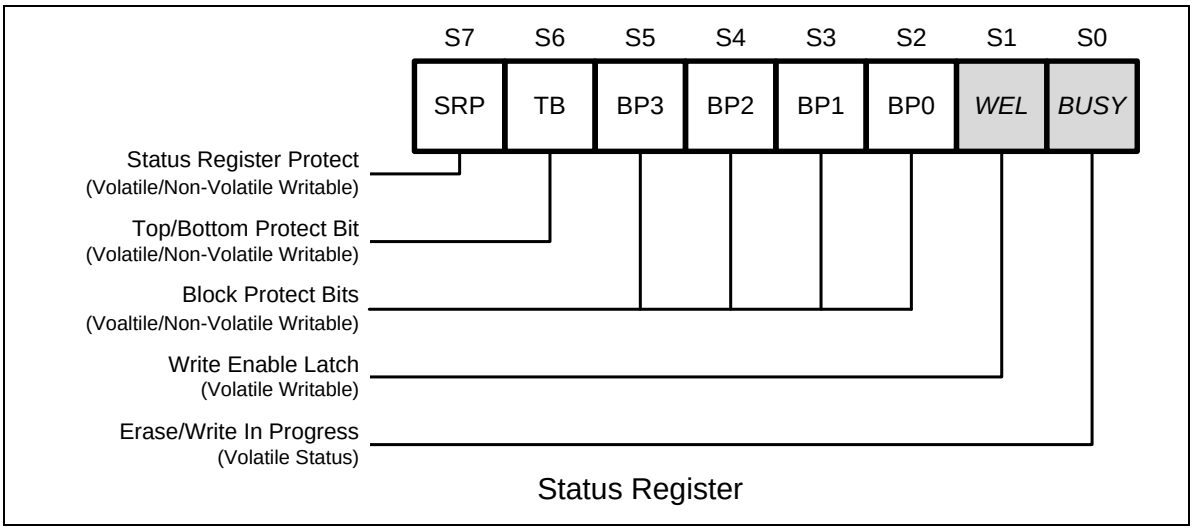


Figure 5-1. Status Register

7.1.1 Erase/Program In Progress (BUSY) – Volatile *Status*

The BUSY bit is a volatile status only bit in the Status Register (S0) that supports multiple functions. Its legacy functionality is to monitor device embedded operations (program, erase, and nonvolatile register writes). It also serves as a monitor of the CRC-At-Rest operation and as a fail/safe power on reset (POR) detection flag after a power up cycle.

The BUSY is set to a '1' (busy) state when the device is executing an internal program including program/erase Security Register/DLP Register, erase operation, or nonvolatile register writes (see t_W, t_{PP}, t_{SE}, t_{BE}, and t_{CE} in AC Characteristics). During an embedded and CRC-At-Rest operation, BUSY is '1', the WEL bit is '1', and the Ready Flag (RF) bit is '0'. During "BUSY" state (BUSY=1, RF=0), the device ignores any commands, except for Read Status Register, Erase/Program Suspend, and Software Reset (66h-99h). Hardware reset and JEDEC Hardware Reset are accepted. A power-down or reset during an embedded operation aborts the operation and can cause data corruption. After the completion of program, erase, or nonvolatile register write (embedded operation), the BUSY bit will be cleared to "0" and RF will be set to "1" indicating the device is ready to accept further commands.

The setting of the WEL bit is not required prior to executing a CRC-At-Rest operation. However, WEL bit is set to '1' as well as BUSY=1 and RF=0 during a CRC-At-Rest internal operation. After the completion of the CRC-At-Rest operation, BUSY is cleared to '0' and RF is set to '1' while WEL bit will keep its old value (either a '0' or '1') prior to the CRC-At-Rest execution.

The BUSY bit along with the RSTO pin, WEL and Ready Flag (RF) bits also function as fail/safe power-up initialization monitor flags after POR (power-up). If BUSY=0, WEL=0, RF=1 and the /RSTO pin is in high impedance after a power-up, the device status indicates that it went through a normal POR process. If the /RSTO pin remains low after POR, this signals a device power-up initialization error. If device default I/O

Mode configuration is intact and the following status bits indicate BUSY=1, WEL=0, and RF=0, this confirms a power up initialization error. A re-initiation of power off and on cycle of the device is required to check if the power-up initialization failure is permanent or can be recovered. A repeated occurrence of a power-up initialization error may indicate a permanent type of failure and should be checked/tested.

7.1.2 Write Enable Latch (WEL) – Volatile Bit

The Write Enable Latch (WEL) is a volatile bit in the Status Register (S1) that is set to 1 after executing a Write Enable Command. Setting the WEL bit to '1' means the device is write enabled, and this is required before an internal program, erase, or volatile/non-volatile register write command initiation. If WEL bit is cleared to '0' (reset), the device becomes write disabled and will not execute any program, erase or non-volatile write register commands. The WEL status bit is cleared to 0 by Write Disable command or by the completion of an internal program, erase, or nonvolatile register write. A write disable state occurs upon power-up or after successful completion of the following commands: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write NVCR, Program/Erase Security Register, and Program/Erase DLP Register.

7.1.3 Block Protect Bits (BP3, BP2, BP1, BP0) – *Non-Volatile Writable*

The Block Protect Bits (BP3, BP2, BP1, BP0) are non-volatile read/write bits in the Status Register (S5, S4, S3, and S2). These Block Protect (BP) bits provide Write Protection control to the device. Depending on the state of the SRP bit, WEL bit, and /WP pin (see SRP bit section for details), BP bits can be set using the Write Status Register Command (see tW in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase commands (see protected memory settings and ranges in the Status Register Memory Protection Table). The factory default setting of the Block Protect Bits is '0' where none of the memory array is protected.

7.1.4 Top/Bottom Block Protect (TB) – *Non-Volatile Writable*

The non-volatile Top/Bottom bit (TB) controls the Block Protect Bits (BP3, BP2, BP1, BP0) memory protection either from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. TB bit can be set with the Write Status Register Command depending on the state of the SRP bit, WEL bit, and /WP pin (see SRP bit section for details).

7.1.5 Status Register Protect (SRP) – *Non-Volatile Writable*

The Status Register Protect bit (SRP) is a non-volatile read/write bit in the Status Register (S7) that enables or disables /WP pin control of protecting against writes to the Status Register. The SRP bit is only functional in SDR mode along with the /WP pin, and it is disabled during ODDR mode. When the SRP bit is set to '1', the /WP can be driven low to protect against writes to the Status Register. If /WP is high when SRP bit is '1', the Status Register is unprotected from writes. When the SRP bit is '0', the Status Register is also unprotected and writes to the Status Register are accepted. The factory default setting of the SRP bit is '0'.

SRP	/WP	Status Register Protection	Description
0	X	Writable	/WP pin has no control. The Status Register can be written to after a Write Enable command, WEL=1.
1	0	Hardware Protected	When /WP pin is low, the device is protected against writes to the Status Register.
	1	Writable	When /WP pin is high, the Status Register can be written to after a Write Enable command, WEL=1.

7.1.6 Status Register Memory Protection (CMP = 0, SPEN=0)

Memory protection is configured using TB, BP3, BP2, BP1, BP0 and CMP setting. The Complement Protect bit (CMP) is a Volatile Configuration Register Address 05h bit 5 (VCR-CMP) that reverses the array protection scheme from the TB, BP3, BP2, BP1 and BP0 setting. The default setting is CMP=0. Refer to the following tables on the available protection schemes.

STATUS REGISTER					W35T51NW (512M-BIT / 64M-BYTE) MEMORY PROTECTION(1)			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
0	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	1023	03FF0000h - 03FFFFFFh	64KB	Upper 1/1024
0	0	0	1	0	1022 thru 1023	03FE0000h - 03FFFFFFh	128KB	Upper 1/512
0	0	0	1	1	1020 thru 1023	03FC0000h - 03FFFFFFh	256KB	Upper 1/256
0	0	1	0	0	1016 thru 1023	03F80000h - 03FFFFFFh	512KB	Upper 1/128
0	0	1	0	1	1008 thru 1023	03F00000h - 03FFFFFFh	1MB	Upper 1/64
0	0	1	1	0	992 thru 1023	03E00000h - 03FFFFFFh	2MB	Upper 1/32
0	0	1	1	1	960 thru 1023	03C00000h - 03FFFFFFh	4MB	Upper 1/16
0	1	0	0	0	896 thru 1023	03800000h - 03FFFFFFh	8MB	Upper 1/8
0	1	0	0	1	768 thru 1023	03000000h - 03FFFFFFh	16MB	Upper 1/4
0	1	0	1	0	512 thru 1023	02000000h - 03FFFFFFh	32MB	Upper 1/2
0	1	0	1	1	0 thru 1023	00000000h - 03FFFFFFh	64MB	ALL
0	1	1	0	0	0 thru 1023	00000000h - 03FFFFFFh	64MB	ALL
0	1	1	0	1	0 thru 1023	00000000h - 03FFFFFFh	64MB	ALL
0	1	1	1	0	0 thru 1023	00000000h - 03FFFFFFh	64MB	ALL
0	1	1	1	1	0 thru 1023	00000000h - 03FFFFFFh	64MB	ALL
1	0	0	0	0	NONE	NONE	NONE	NONE
1	0	0	0	1	0	00000000h - 0000FFFFh	64KB	Lower 1/1024
1	0	0	1	0	0 thru 1	00000000h - 0001FFFFh	128KB	Lower 1/512
1	0	0	1	1	0 thru 3	00000000h - 0003FFFFh	256KB	Lower 1/256
1	0	1	0	0	0 thru 7	00000000h - 0007FFFFh	512KB	Lower 1/128
1	0	1	0	1	0 thru 15	00000000h - 000FFFFFh	1MB	Lower 1/64
1	0	1	1	0	0 thru 31	00000000h - 001FFFFFh	2MB	Lower 1/32
1	0	1	1	1	0 thru 63	00000000h - 003FFFFFh	4MB	Lower 1/16
1	1	0	0	0	0 thru 127	00000000h - 007FFFFFh	8MB	Lower 1/8
1	1	0	0	1	0 thru 255	00000000h - 00FFFFFFh	16MB	Lower 1/4
1	1	0	1	0	0 thru 511	00000000h - 01FFFFFFh	32MB	Lower 1/2
1	1	0	1	1	0 thru 1023	00000000h - 03FFFFFFh	64MB	ALL
1	1	1	0	0	0 thru 1023	00000000h - 03FFFFFFh	64MB	ALL
1	1	1	0	1	0 thru 1023	00000000h - 03FFFFFFh	64MB	ALL
1	1	1	1	0	0 thru 1023	00000000h - 03FFFFFFh	64MB	ALL
1	1	1	1	1	0 thru 1023	00000000h - 03FFFFFFh	64MB	ALL

Notes:
1. If any Erase or Program command specifies a memory region that contains a protected data portion, this command will be ignored.

7.1.7 Status Register Memory Protection (CMP = 1,SPEN=0)

STATUS REGISTER					W35T51NW (512M-BIT / 64M-BYTE) MEMORY PROTECTION(1)			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
0	0	0	0	0	0 thru 1023	00000000h - 03FFFFFFh	ALL	ALL
0	0	0	0	1	0 thru 1022	00000000h - 03FEFFFFh	65,472KB	Lower 1023/1024
0	0	0	1	0	0 thru 1021	03FE0000h - 03FDFFFFh	65,408KB	Lower 511/512
0	0	0	1	1	0 thru 1019	03FC0000h - 03FBFFFFh	65,280KB	Lower 255/256
0	0	1	0	0	0 thru 1015	03F80000h - 03F7FFFFh	65,024KB	Lower 127/128
0	0	1	0	1	0 thru 1007	00000000h – 03EFFFFFh	63MB	Lower 63/64
0	0	1	1	0	0 thru 991	00000000h – 03DFFFFFh	62MB	Lower 31/32
0	0	1	1	1	0 thru 959	00000000h - 03BFFFFFh	60MB	Lower 15/16
0	1	0	0	0	0 thru 895	00000000h - 037FFFFFh	56MB	Lower 7/8
0	1	0	0	1	0 thru 767	00000000h - 02FFFFFFh	48MB	Lower 3/4
0	1	0	1	0	0 thru 511	00000000h - 01FFFFFFh	32MB	Lower 1/2
0	1	0	1	1	NONE	NONE	NONE	NONE
0	1	1	0	0	NONE	NONE	NONE	NONE
0	1	1	0	1	NONE	NONE	NONE	NONE
0	1	1	1	0	NONE	NONE	NONE	NONE
0	1	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	0	0 thru 1023	00000000h - 03FFFFFFh	ALL	ALL
1	0	0	0	1	1 thru 1023	00010000h - 03FFFFFFh	65,472KB	Upper 1023/1024
1	0	0	1	0	2 thru 1023	00020000h - 03FFFFFFh	65,408KB	Upper 511/512
1	0	0	1	1	4 thru 1023	00040000h - 03FFFFFFh	65,280KB	Upper 255/256
1	0	1	0	0	8 thru 1023	00080000h - 03FFFFFFh	65,024KB	Upper 127/128
1	0	1	0	1	16 thru 1023	00100000h - 03FFFFFFh	63MB	Upper 63/64
1	0	1	1	0	32 thru 1023	00200000h - 03FFFFFFh	62MB	Upper 31/32
1	0	1	1	1	64 thru 1023	00400000h - 03FFFFFFh	60MB	Upper 15/16
1	1	0	0	0	128 thru 1023	00800000h - 03FFFFFFh	56MB	Upper 7/8
1	1	0	0	1	256 thru 1023	01000000h - 03FFFFFFh	48MB	Upper 3/4
1	1	0	1	0	512 thru 1023	02000000h - 03FFFFFFh	32MB	Upper 1/2
1	1	0	1	1	NONE	NONE	NONE	NONE
1	1	1	0	0	NONE	NONE	NONE	NONE
1	1	1	0	1	NONE	NONE	NONE	NONE
1	1	1	1	0	NONE	NONE	NONE	NONE
1	1	1	1	1	NONE	NONE	NONE	NONE

Notes:
1. If any Erase or Program command specifies a memory region that contains a protected data portion, this command will be ignored.

7.2 Flag Register

The Flag Register provides status flags of internal Program/Erase/CRC operation, Program/Erase Suspend operation, Protected/OTP access monitor, and Address Mode (3-Byte or 4-Byte). The Flag Register includes Ready Flag, Erase Suspend Flag, Erase Flag (error flag), Program Flag (error flag), CRC-In-Transit Flag, Program Suspend Flag, Protected Memory Access Flag (error flag), and Address Mode Flag. All Flag Register bits are reset to '0' during power-up. Status bits are set and reset automatically after completion of the device operation. Error bits (flag) are cleared by using the Clear Flag Register command.

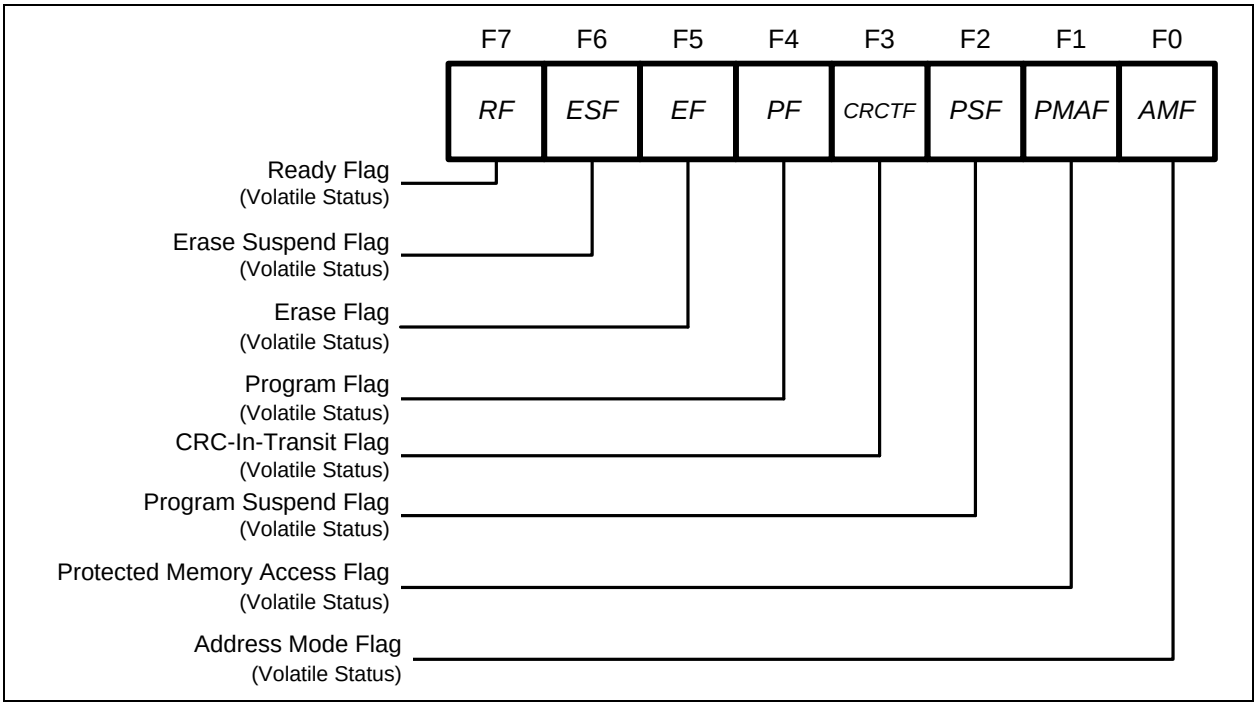


Figure 5-2. Flag Register

7.2.1 Address Mode Flag (AMF) – Volatile *Status Only*

In SDR mode, the device can operate in either 3-Byte or 4-Byte Address mode. From power-up, the Address mode is based on the value of the Non-Volatile Address Mode Configuration Register Address 05h (NVCR-AM) which is transferred to the Volatile Address Mode Configuration Register Address 05h (VCR-AM) and to the Internal Configuration Register.

In ODDR mode, the address mode setting is 4-Byte Address mode, and this is reflected by the AMF flag bit. Switching from SDR to ODDR mode or vice versa also affects the AMF flag status based either on the VCR-AM setting (3 or 4-Byte Address) or the ODDR mode (4-Byte Address).

A Non-Volatile/Volatile Address Mode Configuration Register (NVCR-AM / VCR-AM) value of FFh indicates 3-Byte Address Mode and a value of FEh indicates 4-Byte Address Mode.

The Address Mode Flag, which is a volatile read only bit in the Flag Register Bit 0 (F0), captures the Non-Volatile Address Mode from Volatile Address Mode Configuration setting and provides the current address mode the device is operating in. When AMF bit is '0', the device is in 3-Byte Address Mode, and when the AMF bit is '1', the device is operating in 4-Byte Address Mode. The Non-Volatile/Volatile Address Mode Configuration Register is configurable by the Write Non-Volatile Configuration Register which takes into effect after a reset or power-up and by the Write Volatile Configuration Register which takes into effect on the fly.

Enter 4-Byte Address Mode command and Exit 4-Byte Mode Address Mode command also affect the AMF flag bit and the VCR-AM setting in SDR mode.

7.2.2 Protected Memory Access Flag (PMAF) – Volatile Status Only

The Protected Memory Access Flag (PMAF) is a volatile error flag (F1) in the Flag Register that monitors illegal memory and registers access. The PMAF bit default is '0' and is set to '1' when an illegal program or erase accessed is attempted on protected/locked memory spaces or Security Registers. This bit is cleared to '0' by the Clear Flag Register command, reset, or power-up cycle.

7.2.3 Program Suspend Flag (PSF) – Volatile Status Only

The Program Suspend Flag (PSF) is a volatile read only (F2) in the Flag Register that provides internal program suspend operation status. PSF bit is set to '1' after executing a Program Suspend command. The device is considered in Program Suspend mode when the Ready Flag (F7) in the Flag Register is set to '1' after Erase/Program latency time plus Flag Register outputs at least one byte of data with RF bit outputting a '1'. In the Program Suspend mode, the device is readily available for valid commands.

When the Program Suspend command is initiated and if the Suspend operation time is less than the Suspend latency, the PSF bit will be cleared; whereas, the device also completes the ongoing internal program operation (See Program/Suspend section for detailed operation). Power-up cycle or reset will also clear the PSF bit state to '0'.

7.2.4 CRC-In-Transit Flag (CRCTF) – Volatile Status Only

The CRC-In-Transit Flag (CRCTF) is a volatile error flag (F3) in the Flag Register. It is set to '1' if there is an error during the input transmission in CRC-In-Transit mode. The CRCTF bit is '0' if there is no error during the input transmission in CRC-In-Transit mode. The Clear Flag register command, power-up cycle or reset will clear the CRCTF bit to '0'.

7.2.5 Program Flag (PF) – Volatile Status Only

The Program Flag (PF) is a volatile error flag (F4) in the Flag Register. It provides the status of either the internal program operation or CRC-At-Rest check. The PF is '0' after a successful internal program operation or a CRC-At-Rest check. The PF bit will be set to '1' when an internal program error, CRC-At-Rest check, or protection error occurred. The Clear Flag register command, power-up cycle or reset will clear the PF bit to '0'.

7.2.6 Erase Flag (EF) – Volatile Status Only

The Erase Flag (EF) is a volatile error flag (F5) in the Flag Register which provides internal erase operation status. The EF bit is '0' after a successful internal erase operation. EF will be set to '1' when an internal erase error or protection error occurred. The Clear Flag Register command, power-up cycle or reset will clear the EF bit to '0'.

7.2.7 Erase Suspend Flag (ESF) – Volatile Status Only

The Erase Suspend Flag (ESF) is a volatile read only bit (F6) in the Flag Register that provides internal erase suspend operation status. ESF is set to '1' after executing an Erase Suspend command. The device is considered in the Erase Suspend mode when the Ready Flag (F7) is set to '1' after an Erase/Program latency time plus the Flag Register outputs at least one byte of data with RF bit outputting a '1'. In the Erase Suspend mode, the device is readily available for valid and acceptable commands.

When the Erase Suspend command is initiated and if the Suspend operation time is less than the Suspend latency, the ESF bit will be cleared; whereas, the device also completes the ongoing internal erase operation (See Program/Suspend section for detailed operation). A Power-up cycle or reset will clear the ESF bit state to '0'.

7.2.8 Ready Flag (RF) – Volatile Status Only

Ready Flag (RF) is a volatile read only bit (F7) in the Flag Register that behaves like an inverse of the BUSY bit value. It also functions as a status monitor for ongoing embedded/CRC-At-Rest operations and a fail/safe power on reset status flag. If the device BUSY bit is '1', the RF bit is '0'. If the device BUSY bit is '0', the RF bit is '1'. Please refer to the BUSY bit section for detailed operation of the RF bit in conjunction with the BUSY and WEL bits.

7.3 Internal Configuration Register

Device operation and configuration is set and controlled by the Internal Configuration Register. It is not accessible externally. Changes to this register are either through the Non-Volatile Configuration Register, Volatile Configuration Register or specific Commands. The default configuration of the Internal Configuration Register from power up or reset is based from the transferred Non-Volatile Configuration Register values to the Volatile Configuration Register. During device operation, changes to the Volatile Configuration Register values transfer directly to the Internal Configuration Register and instantly change the device configuration.

7.4 Non-Volatile Configuration Register

The Non-Volatile Configuration Register contains 256 bytes and is the device configuration baseline from power-up or reset. Device configurations that includes Wrap Configuration, XIP Configuration, Address Mode Configuration, CRC-In-Transit Partition, Output Driver Strength, Security Register OTP Locks, Complement Protect, Dummy Clock Cycle, and Bus Interface Mode settings are stored in the Non-Volatile Configuration Register Address[07h:00h] range. Address[FFh:08h] are 'Reserved'. The supported device configurations are illustrated in the table below. This register can be read using the Read Non-Volatile Configuration Register command and written using the Write Non-Volatile Configuration Register command (see Command Set Table and Command Description for details). Configuration changes on 02h OTP Lock and CMP register bits take effect right after writing the Non-Volatile Configuration Register. All other configuration changes will take into effect after a power cycle or reset. Reserved values in the Non-Volatile Configuration Register are FFh. Write attempts to reserved addresses are ignored and will trigger the setting of Bit 1 (PMAF bit) in the Flag Register to '1', and clearing of WEL bit to '0'.

Address	Name	Description	Function Settings	Default[1]
08h:FFh[3]	Reserved	Reserved	Reserved	FFh
07h[3]	Wrap Around Mode Configuration (NVCR-Wrap)	Read sequence setting either in continuous incremental read or wrap around mode in 16, 32, or 64 byte boundaries.	FFh: Continuous FEh: 64 Bytes FDh: 32 Bytes FCh: 16 Bytes Others: Reserved	FFh
06h[3]	Execute-in-Place (XIP) Configuration (NVCR-XIP)	XIP mode setting after power on reset or reset	FFh: XIP Disabled FEh: 8IOFR XIP FDh: 8OFR XIP F8h: Fast Read XIP Others: Reserved	FFh
05h[3]	Address Mode Configuration Beyond 128Mb (NVCR-AM)	Address mode setting (3-bytes or 4-bytes) used during address input for commands	FFh: 3 Byte Address mode FEh: 4 Byte Address mode Others: Reserved	FFh
04h[3]	CRC-In-Transit Mode (NVCR-CRC)	CRC-In-Transit data partition setting	FFh: CRC-In-Transit Disable F8h: CRC-In-Transit 16-Byte data partition FAh: CRC-In-Transit 32-Byte data partition FCh: CRC-In-Transit 64-Byte data partition FEh: CRC-In-Transit 128-Byte data partition Others: Reserved	FFh

03h[3]	Output Driver Strength Configuration (NVCR-DS)	Output impedance setting at Vdd/2 output voltage during read operations.	FFh: 50Ω FEh: 35Ω FDh: 25Ω FCh: 18Ω 0Fh: 160Ω 0Eh: 150Ω 0Dh: 80Ω 0Ch: 75Ω Others: Reserved		FFh
02h[4]	SFDP OTP Lock	SFDP OTP Lock Bit	Bit 0	0: Default 1: SFDP Permanently Locked	90h
	Security Register OTP Lock Bits (NVCR-OLB)	Security Register-1 OTP Lock Bit	Bit 1	0: Default 1: Security Register-1 Permanently Locked	
		Security Register-2 OTP Lock Bit	Bit 2	0: Default 1: Security Register-2 Permanently Locked	
		Security Register-3 OTP Lock Bit	Bit 3	0: Default 1: Security Register-3 Permanently Locked	
	Reserved	Reserved	Bit 4	Reserved	
	Reserved[5]	Reserved	Bit [6:5]	0: Default (Disabled) 1: Reserved (must not use)	
	Reserved	Reserved	Bit 7	Reserved	
01h[3]	Dummy Clock Cycle Configuration (NVCR-DC)	Number of dummy clock cycle setting between the address input and the expected data output for all Fast Read commands. Refer to the Command Set Table for default number of dummy clock cycle values)	00h: Identical to 1Fh 01h: 1 Dummy Cycle 02h: 2 Dummy Cycles 03 to 1Dh: 3 to 29 Dummy Cycles 1Eh: 30 Dummy Cycles 1Fh: Default Others: Reserved		1Fh
00h[3]	Input/Output (I/O) Mode Configuration (NVCR-IOC)[2]	I/O mode configuration the device will operate from Standard SPI to Octal DDR mode along with or without data strobe (DS mode).	FFh: Default for Extended SPI (Device ID: Configuration=00h) [2] DFh: Extended SPI without DS E7h: Default for Octal DDR (Device ID: Configuration=04h)[2] C7h: Octal DDR without DS Others: Reserved		FFh or E7h[2]

Notes:

1. Default values from power-up or reset from factory. These values are configurable by the Write Non-Volatile Configuration Register command.
2. For 'W35T51NWxx**E**' devices that are factory preset with Extended SPI (Device ID: Configuration = 00h or IO Mode Boot up Configuration = 0b), address 00h of the Nonvolatile Configuration Register (NVCR) is fully configurable to any of the defined values. For 'W35T51NWxx**F**' devices that are factory preset with Octal DDR (Device ID: Configuration = 04h or IO Mode Boot up Configuration = 1b), NVCR address 00h value can only be configured by either 'E7h' Octal DDR with DS (default) or 'C7h' Octal DDR without DS values.
3. Update takes effect after power cycle or reset.
4. Update takes effect after Write Non-Volatile Configuration Register.
5. NVCR[6] is reserved and must not be used, NVCR[7:6,4] should always be written as 101b.

7.5 Volatile Configuration Register

The Volatile Configuration Register is a separate volatile register identical to the Non-Volatile Configuration Register in terms of size (256 bytes) and configurable content. The table below provides the configurable features and definition of the Volatile Configuration Register. After power up or reset, the Volatile Configuration Register gets its values transferred from the Non-Volatile Configuration Register values while the Non-Volatile Configuration Register values are also transferred directly to the Internal Configuration Register for initial configuration. After power up or reset, changes to the configuration of the Volatile Configuration Register via the Write Volatile Configuration Register command are transferred directly to the Internal Configuration Register which will instantly affect the device operation. Attempts to write to the reserved addresses are ignored which will trigger the setting of Flag Register Bit 1 (PMAF bit) to '1' and clearing of WEL bit to '0'.

Address	Name	Description	Function Settings		Default[1]
08h:FFh	Reserved	Reserved	Reserved		-
07h	Wrap Around Mode Configuration (VCR-Wrap)	Read sequence setting either in continuous incremental read or wrap around mode in 16, 32, or 64 byte boundaries.	FFh: Continuous FEh: 64 Bytes FDh: 32 Bytes FCh: 16 Bytes Others: Reserved		-
06h	Execute-in-Place (XIP) Configuration (VCR-XIP)	XIP mode setting	FFh: XIP Disabled FEh: XIP Enabled Others: Reserved		-
05h	Address Mode Configuration Beyond 128Mb (VCR-AM)	Address mode setting (3-bytes or 4-bytes) used during address input for commands	FFh: 3 Byte Address mode FEh: 4 Byte Address mode Others: Reserved		-
04h	CRC-In-Transit Mode (VCR-CRC)	CRC-In-Transit data partition setting	FFh: CRC-In-Transit Disable F8h: CRC-In-Transit 16-Byte data partition FAh: CRC-In-Transit 32-Byte data partition FCh: CRC-In-Transit 64-Byte data partition FEh: CRC-In-Transit 128-Byte data partition Others: Reserved		-
03h	Output Driver Strength Configuration (VCR-DS)	Output impedance setting at Vdd/2 output voltage during read operations.	FFh: 50Ω FEh: 35Ω FDh: 25Ω FCh: 18Ω 0Fh: 160Ω 0Eh: 150Ω 0Dh: 80Ω 0Ch: 75Ω Others: Reserved		-
02h[3]	SFDP Volatile Lock	SFDP Volatile Lock Bit:	Bit 0[3]	0: Default **(cannot be written to 0.)** 1: SFDP Temporary Locked	10h
	Security Register Volatile Lock Bits (VCR-VLB)	Security Register-1 Volatile Lock Bit	Bit 1	0: Default 1: Security Register-1 Protected	
		Security Register-2 Volatile Lock Bit	Bit 2	0: Default 1: Security Register-2 Protected	
		Security Register-3 Volatile Lock Bit	Bit 3	0: Default 1: Security Register-3 Protected	
	Reserved[3]	Reserved	Bit 4[3]	Reserved	
	Complement Protect (VCR-CMP)	Complement Protect Volatile Bit	Bit 5[4]	0: Default 1: Complement Protect	
	Reserved[3]	Reserved	Bit[7:6][3]	Reserved	

01h	Dummy Clock Cycle Configuration (VCR-DC)	Number of dummy clock cycle setting between the address input and the expected data output for all Fast Read commands. Refer to the Command Set Table for default number of dummy clock cycle values)	00h: Default 01h: 1 Dummy Cycle 02h: 2 Dummy Cycles 03 to 1Dh: 3 to 29 Dummy Cycles 1Eh: 30 Dummy Cycles 1Fh: Default Others: Reserved	-
00h	Input/Output (I/O) Mode Configuration (VCR-IOC)	I/O mode configuration the device will operate from Standard SPI to Octal DDR mode along with or without data strobe (DS mode).	FFh: Default for Extended SPI (Device ID: Configuration=00h) [2] DFh: Extended SPI without DS E7h: Default for Octal DDR (Device ID: Configuration=04h)[2] C7h: Octal DDR without DS Others: Reserved	FFh or E7h[2]

Notes:

1. Default values from power-up or reset are based on the Non-Volatile Configuration Register values.
2. FFh is the default value for factory default Extended SPI (SDR). E7h is default for Factory default Octal DDR.
3. Reserved bits[7,4], and bit0, SFDP Volatile Lock, can only be written to 1. If a Write VCR command tries to write a 0 to any of these bits, the command will be ignored.
4. The CMP bit will return to its default value (0) after each power-up and will not be reset by HW/SW Reset.

7.5.1 Clock Frequency with Required Dummy Clock Cycles

7.5.1.1 4-Byte Aligned Start Address (A[1:0]=00b)[1]

NUMBER OF DUMMY CLOCK CYCLES	FAST READ	FAST READ OCTAL I/O		OCTAL DDR (ODDR)
	SDR	SDR	DDR	
8	**166[2]**	50	50	50
16	166	**166[2]**	**166[2]**	**166[2]**
22 and above	166	200	200	200

Notes:

1. Values are guaranteed by characterization with TFBGA-24 package and not 100% tested in production.
2. Highlighted values are clock speeds for default dummy clock cycles.

7.5.1.2 32-Byte Aligned Start Address (A[4:0]=00000b)[1]

NUMBER OF DUMMY CLOCK CYCLES	FAST READ	FAST READ OCTAL I/O		OCTAL DDR (ODDR)
	SDR	SDR	DDR	
8	**166[2]**	104	104	104
16 and above	166	**200[2]**	**200[2]**	**200[2]**

Notes:

3. Values are guaranteed by characterization with TFBGA-24 package and not 100% tested in production.
1. Highlighted values are clock speeds for default dummy clock cycles.

7.5.1.3 4-Byte Aligned Start Address for XIP(A[1:0]=00b)[1]

NUMBER OF DUMMY CLOCK CYCLES	FAST READ	FAST READ OCTAL I/O		OCTAL DDR (ODDR)
	SDR	SDR	DDR	
8	**133[2]**	33	33	33
16	133	**133[2]**	**133[2]**	**133[2]**
22 and above	133	166	166	166

Notes:

4. Values are guaranteed by characterization with TFBGA-24 package and not 100% tested in production.
1. Highlighted values are clock speeds for default dummy clock cycles.

7.5.1.4 32-Byte Aligned Start Address for XIP (A[4:0]=00000b)[1]

NUMBER OF DUMMY CLOCK CYCLES	FAST READ	FAST READ OCTAL I/O		OCTAL DDR (ODDR)
	SDR	SDR	DDR	
8	**133[2]**	80	80	80
16 and above	133	**166[2]**	**166[2]**	**166[2]**

Notes:

5. Values are guaranteed by characterization with TFBGA-24 package and not 100% tested in production.
1. Highlighted values are clock speeds for default dummy clock cycles.

7.5.2 Wrap-Around Size with Address Input Sequence and Interval

The NVCR-Wrap-Around Configuration (NVCR-Wrap) and Volatile Wrap-Around Configuration (VCR-Wrap) Address 06h defines the length of read burst data in either continuous (default), 64-byte wrap, 32-byte wrap or 16-byte wrap range. There are some applications that can benefit from this feature to improve the overall system performance.

From power up or reset, the NVCR-Wrap settings are transferred to the VCR-Wrap. Depending on the settings, the device will boot up in FFh (continuous/default), FEh (64-Byte Wrap), FDh (32-Byte Wrap), or FCh (16-Byte Wrap) configuration.

WRAP AROUND SIZE	ADDRESS RANGES/BOUNDARIES[1]
16 Bytes	00h-0Fh, 10h-1Fh, 20h-2Fh, 30h-3Fh… 01FFFFE0h - 01FFFFEFh, 01FFFFF0h - 01FFFFFFh
32 Bytes	00h-1Fh, 20h-3Fh, 40h-5Fh, 60h-7Fh…01FFFFC0h - 01FFFFDFh, 01FFFFE0h - 01FFFFFFh
64 Bytes	00h-3Fh, 40h-7Fh, 80h-BFh, C0h-FFh…01FFFF80h - 01FFFFBFh, 01FFFFC0h - 01FFFFFFh

Notes:

1. The starting address can be anywhere within the address range and read sequences wrap around address boundaries. When the incremental data output reaches the highest address boundary, the next data output wraps around to the beginning of the address boundary.

7.6 Device ID

The W35T51NW Device ID show in the table can be read by Read JEDEC Device ID (9Fh) or Read ID (9Eh) commands and in either Extended SPI (SDR) or Octal DDR (ODDR) mode.

7.6.1 Manufacturer and Device Identification

JEDEC MANUFACTURER ID	(MF7 - MF0)	NUMBER OF BYTES	ADDRESS
Winbond Octal DDR Flash	EFh	1 Byte	00h
JEDEC Device ID		Total 2 Bytes	
Memory Type	5Bh = 1.8V	1 Byte	01h
Memory Capacity	1Ah = 512Mb	1 Byte	02h
Device ID Extension		Total 3 Bytes	
Size of Device ID Extension	02h	1 Byte	03h
Device ID: Revision/Type	00h: Uniform 64KB Blocks 01h: Uniform 128KB Blocks	1 Byte	04h
Device ID: Configuration	00h: Extended SPI (SDR) 04h: Octal DDR (ODDR)	1 Byte	05h

7.6.2 Device ID: Revision/Type (Address 04h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	**Device Generation**: 0 = 1st Generation 1 = 2nd Generation	Reserved	Reserved	Reserved	Reserved	**Block Size**: 00 = Uniform 64KB Blocks (Default) 01 = Uniform 128KB blocks	

7.6.3 Device ID: Configuration (Address 05h)

The Device ID: Configuration determines the factory default IO Mode Configuration of the device which is also indicated by the full marketing part number suffix ('-E' or '-F'). The table below shows the bit location/setting of the IO Mode Boot up Configuration. This Device ID: Configuration is also used during power loss and interface recovery in case the device powers up in an indeterminate state due to corruption of the Non-Volatile Configuration Register setting.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	**IO Mode Boot up Configuration**: 0 = Extended SPI (SDR) for W35T51NWxx**E** 1 = Octal DDR (ODDR) for W35T51NWxx**F**	Reserved	Reserved

7.7 Serial Flash Discovery Parameter (SFDP) Register

The W35T51NW has a 1K-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, supported read commands, and supported features like: Supported IO mode, Read Command codes, Memory Block sizes, Suspend/Resume, Power-down mode, Program/Erase times, others. The SFDP parameters are stored in an area separate from the memory array.

The SFDP Register is accessed through the Read SFDP (5Ah) command which is compatible with SFDP standard established in 2010 for PC and other applications, as well as several JEDEC standard revisions JESD216/216A-F.

Description		Address (Byte)	DW Address (Bit)	Data
SFDP signature		00H	A7:A0	53h
		01H	A15:A8	46h
		02H	A23:A16	44h
		03H	A31:A24	50h
SFDP Minor Revision		04H	A7:A0	0Ah
SFDP Major Revision		05H	A15:A8	01h
Number of Parameter Headers (NPH)		06H	A23:A16	02h
SFDP Access Protocol	**W35T51NWxxxE**	07H	A31:A24	FFh
	W35T51NWxxxF	07H	A31:A24	FEh
Parameter ID LSB		08H	A7:A0	00h
Parameter Table Minor Revision		09H	A15:A8	08h
Parameter Table Major Revision		0AH	A23:A16	01h
Parameter Table Length		0BH	A31:A24	17h
Parameter Table Pointer		0CH	A7:A0	80h
		0DH	A15:A8	00h
		0EH	A23:A16	00h
Parameter ID MSB		0FH	A31:A24	FFh
Parameter ID LSB		10H	A7:A0	84h
Parameter Table Minor Revision		11H	A15:A8	01h
Parameter Table Major Revision		12H	A23:A16	01h
Parameter Table Length		13H	A31:A24	02h
Parameter Table Pointer (PTP)		14H	A7:A0	E0h
		15H	A15:A8	00h
		16H	A23:A16	00h
Parameter ID MSB		17H	A31:A24	FFh
Parameter ID LSB		18H	A7:A0	05h
Parameter Table Minor Revision		19H	A15:A8	01h
Parameter Table Major Revision		1AH	A23:A16	01h
Parameter Table Length		1BH	A31:A24	06h
Parameter Table Pointer (PTP)		1CH	A7:A0	E8h
		1DH	A15:A8	00h
		1EH	A23:A16	00h
Parameter ID MSB		1FH	A31:A24	FFh
Block/Sector Erase Sizes		80H	A1:A0	01b
Write Granularity		80H	A2	1
Volatile Status Register Block Protect bits		80H	A3	0
Write Enable Command Select for Writing to Volatile Status Register		80H	A4	0
Unused		80H	A7:A5	111b
4 Kilobyte Erase Command		81H	A15:A8	20h
Supports (1S-1S-2S) Fast Read		82H	A16	0
Address Bytes		82H	A18:A17	01b
Supports Double Transfer Rate (DTR) Clocking		82H	A19	1
Supports (1S-2S-2S) Fast Read		82H	A20	0
Supports (1S-4S-4S) Fast Read		82H	A21	0
Supports (1S-1S-4S) Fast Read		82H	A22	0
Unused		82H	A23	1

Unused	83H	A31:A24	FFh
Flash Memory Density	84H	A7:A0	FFh
	85H	A15:A8	FFh
	86H	A23:A16	FFh
	87H	A31:A24	1Fh
(1S-4S-4S) Fast Read Number of Wait states (dummy clocks) needed before valid output	88H	A4:A0	00000b
Quad Input Address Quad Output (1S-4S-4S) Fast Read Number of Mode Clocks	88H	A7:A5	000b
(1S-4S-4S) Fast Read Command	89H	A15:A8	00h
(1S-1S-4S) Fast Read Number of Wait states (dummy clocks) needed before valid output	8AH	A20:A16	00000b
(1S-1S-4S) Fast Read Number of Mode Clocks	8AH	A23:A21	000b
(1S-1S-4S) Fast Read Command	8BH	A31:A24	00h
(1S-1S-2S) Fast Read Number of Wait states (dummy clocks) needed before valid output	8CH	A4:A0	00000b
(1S-1S-2S) Fast Read Number of Mode Clocks	8CH	A4:A0	000b
(1S-1S-2S) Fast Read Command	8DH	A15:A8	00h
(1S-2S-2S) Fast Read Number of Wait states (dummy clocks) needed before valid output	8EH	A20:A16	00000b
(1S-2S-2S) Fast Read Number of Mode Clocks	8EH	A23:A21	000b
(1S-2S-2S) Fast Read Command	8FH	A31:A24	00h
Supports (2S-2S-2S) Fast Read	90H	A0	0
Reserved	90H	A3:A1	111b
Supports (4S-4S-4S) Fast Read	90H	A4	0
Reserved	90H	A7:A5	111b
Reserved	91H	A15:A8	FFh
Reserved	92H	A23:A16	FFh
Reserved	93H	A31:A24	FFh
Reserved	94H	A7:A0	FFh
Reserved	95H	A15:A8	FFh
(2S-2S-2S) Fast Read Number of Wait states (dummy clocks) needed before valid output	96H	A20:A16	00000b
(2S-2S-2S) Fast Read Number of Mode Clocks	96H	A23:A21	000b
(2S-2S-2S) Fast Read Command	97H	A31:A24	00h
Reserved	98H	A7:A0	FFh
Reserved	99H	A15:A8	FFh
(4S-4S-4S) Fast Read Number of Wait states (dummy clocks) needed before valid output	9AH	A20:A16	00000b
(4S-4S-4S) Fast Read Number of Mode Clocks	9AH	A23:A21	000b
(4S-4S-4S) Fast Read Command	9BH	A31:A24	00h
Sector Type 1 Size	9CH	A7:A0	0Ch
Sector Type 1 Command	9DH	A15:A8	20h
Sector Type 2 Size	9EH	A23:A16	0Fh
Sector Type 2 Command	9FH	A31:A24	52h
Sector Type 3 Size	A0H	A7:A0	10h
Sector Type 3 Command	A1H	A15:A8	D8h
Sector Type 4 Size	A2H	A23:A16	00h
Sector Type 4 Command	A3H	A31:A24	00h
Multiplier from typical erase time to maximum erase time	A4H:A7H	A3:A0	0100b
Sector Type 1 Erase, Typical Time		A10:A4	0100011b
Sector Type 2 Erase, Typical time		A17:A11	0101010b
Sector Type 3 Erase, Typical time		A24:A18	0101101b
Sector Type 4 Erase, Typical time		A31:A25	0000000b
Multiplier from typical time to max time for Page or byte program	A8H:ABH	A3:A0	0010b
Page Size		A7:A4	1000b
Page Program Typical Time		A13:A8	100011b
Byte Program Typical time, first byte		A18:A14	10011b
Byte Program Typical time, additional byte		A19:A23	00010b
Chip Erase, Typical time		A30:A24	1011000b

Reserved		A31	0
Prohibited Operations During Program Suspend	ACH:AFH	A3:A0	1001b
Prohibited Operations During Erase Suspend		A7:A4	1110b
Reserved		A8	1
Program Resume to Suspend Interval		A12:A9	0001b
Suspend in-progress program max latency		A19:A13	0110011b
Erase Resume to Suspend Interval		A23:A20	0111b
Suspend in-progress erase max latency		A30:A24	0110011b
Suspend / Resume supported		A31	0
Program Resume Command	B0H	A7:A0	7Ah
Program Suspend Command	B1H	A15:A8	75h
Resume Command	B2H	A23:A16	7Ah
Suspend Command	B3H	A31:A24	75h
Reserved	B4H:B7H	A1:A0	11b
Status Register Polling Device Busy		A7:A2	111111b
Exit Deep Powerdown to next operation delay		A14:A8	1000011b
Exit Deep Powerdown Command		A22:A15	10101011b
Enter Deep Powerdown Command		A30:A23	10111001b
Deep Powerdown Supported		A31	0
4S-4S-4S mode disable sequences	B8H:BBH	A3:A0	0000b
4S-4S-4S mode enable sequences		A8:A4	00000b
0-4-4 mode supported		A9	0
0-4-4 Mode Exit Method		A15:A10	100000b
0-4-4 Mode Entry Method		A19:A16	0000b
Quad Enable Requirements (QER):		A22:A20	111b
HOLD or RESET Disable		A23	0
Reserved		A31:A24	FFh
Volatile or Non-Volatile Register and Write Enable Command for Status Register 1	BCH:BFH	A6:A0	1101001b
Reserved		A7	1
Soft Reset and Rescue Sequence Support		A13:A8	010000b
Exit 4-Byte Addressing		A14:A23	1111100001b
Enter 4-Byte Addressing		A24:A31	10100001b
(1S-8S-8S) Fast Read Number of Wait states (dummy clocks) needed before valid output	C0H:C3H	A4:A0	10000b
(1S-8S-8S) Fast Read Number of Mode Clocks		A:7:A5	000b
(1S-8S-8S) Fast Read Command		A15:A8	CBh
(1S-1S-8S) Fast Read Number of Wait states (dummy clocks) needed before valid output		A20:A16	01000b
(1S-1S-8S) Fast Read Number of Mode Clocks		A23:A21	000b
(1S-1S-8S) Fast Read Command		A31:A24	8Bh
Reserved. Leave as "0".	C4H:C7H	A17:A0	00b,00h,00h
Variable Output Driver Strength		A22:A18	01011b
JEDEC SPI Protocol Reset (In-Band Reset)		A23	1
Data Strobe Waveforms in STR Mode		A25:A24	00b
Data Strobe support for QPI STR mode (4S-4S-4S)		A26	0
Data Strobe support for QPI DTR mode (4S-4D-4D)		A27	0
Reserved. Leave as "0".		A28	0
Octal DTR (8D-8D-8D) Command and Command Extension		A30:A29	00b
Byte Order in 8D-8D-8D mode		A31	0
8s-8s-8s mode disable sequences	C8H:CBH	A3:A0	0000b
8s-8s-8s mode enable sequences		A8:A4	00000b
0-8-8 mode supported		A9	0
0-8-8 Mode Exit Method		A15:A10	000000b
0-8-8 Mode Entry Method:		A19:A16	0000b
Octal Enable Requirements:		A22:A20	000b
Reserved. Leave as "0".		A31:A23	00h,0b
Maximum operation speed of device in 4S-4S-4S mode when not utilizing Data Strobe	CCH:CFH	A3:A0	1111b

Maximum operation speed of device in 4S-4S-4S mode when utilizing Data Strobe		A7:A4	1111b
Maximum operation speed of device in 4S-4D-4D mode when not utilizing Data Strobe		A11:A8	1111b
Maximum operation speed of device in 4S-4D-4D mode when utilizing Data Strobe		A15:A12	1111b
Maximum operation speed of device in 8S-8S-8S mode when not utilizing Data Strobe		A19:A16	1111b
Maximum operation speed of device in 8S-8S-8S mode when utilizing Data Strobe		A23:A20	1111b
Maximum operation speed of device in 8D-8D-8D mode when not utilizing Data Strobe		A27:A24	0110b
Maximum operation speed of device in 8D-8D-8D mode when utilizing Data Strobe		A31:A28	1000b
Supports (1S-1D-1D) Fast Read	D0H:D3H	A0	0
Supports (1S-2D-2D) Fast Read		A1	0
Supports (1S-4D-4D) Fast Read		A2	0
Supports (4S-4D-4D) Fast Read		A3	0
Reserved. These bits default to all 0's		A31:A4	00h,00h,00h,0000b
(1S-1D-1D) Fast Read Number of Wait states (dummy clocks) needed before valid output	D4H:D7H	A4:A0	00000b
(1S-1D-1D) Fast Read Number of Mode Clocks		A7:A5	000b
(1S-1D-1D) Fast Read Command		A15:A8	00h
(1S-2D-2D) Fast Read Number of Wait states (dummy clocks) needed before valid output		A20:A16	00000b
(1S-2D-2D) Fast Read Number of Mode Clocks		A23:A21	000b
(1S-2D-2D) Fast Read Command DTR		A31:A24	00h
(1S-4D-4D) Fast Read Number of Wait states (dummy clocks) needed before valid output	D8H:DBH	A4:A0	00000b
(1S-4D-4D) Fast Read Number of Mode Clocks		A7:A5	000b
(1S-4D-4D) Fast Read Command DTR		A15:A18	00h
(4S-4D-4D) Fast Read Number of Wait states (dummy clocks) needed before valid output		A20:A16	00000b
(4S-4D-4D) Fast Read Number of Mode Clocks		A23:A21	000b
(4S-4D-4D) Fast Read Command		A31:A24	00h
Support for (1S-1S-1S) READ Command, Command=13h	E0h:E3h	A0	1
Support for (1S-1S-1S) FAST_READ Command, Command=0Ch		A1	1
Support for (1S-1S-2)S FAST_READ Command, Command=3Ch		A2	0
Support for (1S-2S-2S) FAST_READ Command, Command=BCh		A3	0
Support for (1S-1S-4S) FAST_READ Command, Command=6Ch		A4	0
Support for (1S-4S-4)S FAST_READ Command, Command=ECh		A5	0
Support for (1S-1S-1S) Page Program Command, Command=12h		A6	1
Support for (1S-1S-4S) Page Program Command, Command=34h		A7	0
Support for (1S-4S-4S) Page Program Command, Command=3Eh		A8	0
Support for Erase Command – Type 1 size,		A9	1
Support for Erase Command – Type 2 size,		A10	1
Support for Erase Command – Type 3 size,		A11	1
Support for Erase Command – Type 4 size,		A12	0
Support for (1S-1D-1D) DTR_Read Command, Command=0Eh		A13	0
Support for (1S-2D-2D) DTR_Read Command, Command=BEh		A14	0
Support for (1S-4D-4D) DTR_Read Command, Command=EEh		A15	0

Support for volatile individual sector lock Read command, Command=E0h		A16	0
Support for volatile individual sector lock Write command, Command=E1h		A17	0
Support for non-volatile individual sector lock read command, Command=E2h		A18	0
Support for non-volatile individual sector lock write command, Command=E3h		A19	0
Support for (1S-1S-8S) FAST_READ Command, Command=7Ch		A20	1
Support for (1S-8S-8S) FAST_READ Command, Command=CCh		A21	1
Support for (1S-8D-8D) DTR_READ Command, Command=FDh		A22	1
Support for (1S-1S-8S) Page Program Command, Command=84h		A23	1
Support for (1S-8S-8S) Page Program Command, Command=8Eh		A24	1
Reserved		A31:A25	1111111b
Command for Erase Type 1	E4h	A7:A0	21h
Command for Erase Type 2	E5h	A15:A8	5Ch
Command for Erase Type 3	E6h	A23:A16	DCh
Command for Erase Type 4	E7h	A31:A24	FFh
Read Fast Wrapped command	E8h:EBh	A7:A0	00h
Read Fast command		A15:A8	0Bh
Reserved. Leave as "0".		A21:A16	000000b
Number of Data Bytes Used for Write Register command		A22	0
Number of Additional Modifier Bytes Used for Write Register command		A23	0
Number of Additional Modifier Bytes Used for Write Status-Cfg Register command		A24	0
Initial Latency (CK cycles) for Read Non-Volatile Register command		A25	1
Initial Latency (CK cycles) for Read Volatile Register command		A26	1
Number of Additional Modifier Bytes Used for Read Register command		A27	0
Initial Latency (CK cycles) for Read Status Register command		A28	1
Number of Additional Modifier Bytes Used for Read Status Register command		A29	0
SFDP Command in 8D-8D-8D mode – Dummy Cycles		A30	0
SFDP Command in 8D-8D-8D mode – Address Bytes		A31	0
Write NV Register command	ECh:EFh	A7:A0	B1h
Write Volatile Register command		A15:A8	81h
Read NV Register command		A23:A16	B5h
Read Volatile Register command		A34:A24	85h
Reserved. Leave as "0".	F0h:F3h	A9:A0	00b,00h
Enter default protocol mode		A10	0
Soft Reset and Enter default protocol mode.		A11	1
Reset Enable		A12	1
Soft Reset		A13	0
Exit Deep Power Down		A14	1
Enter Deep Power Down		A15	1
Write NV Register		A16	1
Write Volatile Register		A17	1
Write Register		A18	0
Clear Flag Status Reg		A19	1
Write Status-Configuration Register		A20	1

Read NV Register		A21	1
Read Volatile Register		A22	1
Read Register		A23	0
Read Flag Status Register		A24	1
Read Configuration Register		A25	0
Erase Chip		A26	1
Erase 32Kbytes		A27	1
Erase 4Kbytes		A28	1
Setup Read Wrap		A29	0
Read Fast Wrapped		A30	0
Read SFDP 8D-8D-8D		A31	1
Reserved. Leave as "0".	F4h:F7h	A1:A0	00b
200 MHz operation: configuration bit pattern to set this number of dummy cycles		A6:A2	10110b
200 MHz operation: number of dummy cycles required		A11:A7	10110b
Reserved. Leave as "0".		A31:A12	00h,00h,0000b
Reserved. Leave as "0".	F8h:FBh	A1:A0	00b
100 MHz operation: configuration bit pattern to set this number of dummy cycles		A6:A2	01100b
100 MHz operation: number of dummy cycles required		A11:A7	01100b
133 MHz operation: configuration bit pattern to set this number of dummy cycles		A16:A12	01111b
133 MHz operation: number of dummy cycles required		A21:A17	01111b
166 MHz operation: configuration bit pattern to set this number of dummy cycles		A26:A22	10011b
166 MHz operation: number of dummy cycles required		A31:27	10011b
(8D-8D-8D) Default Dummy Cycles after POR	FCh:FFh	A4:A0	10000b
(8S-8S-8S) Default Dummy Cycles after POR		A9:A5	00000b
Reserved. Leave as "0".		A31:A10	00h,00h,000000b

7.8 Unique ID

The W35T51NW Unique ID is a 16-Byte segment that is factory-programmed. Each device's Unique ID is programmed with a unique number and cannot be changed. This Unique ID number is used in conjunction with user software to help prevent system copying or cloning.

Address	Name	Size	Default Value
N/A	Unique ID	16-Byte	Factory Programmed

7.9 Security Registers

The W35T51NW supports three 1K-Byte Security Registers on separate segment register address. The Security Registers are readable, programmable, and erasable individually. The Read Security Register (48h) command is used to read the Security Registers. The Program Security Register (42h) is used to program the Security Registers, and the Erase Security Register (44h) is used to erase individual 1K-Byte Security Register segments.

Each Security Register has separate OTP Lock Bits and Volatile Lock Bits for write protection. The OTP Lock Bits are in NVCR-Security Register OTP Address 04h Bits[3:1] (NVCR-OLB), while the Volatile Lock Bits are in VCR-Security Register OTP Address 04h Bits[3:1] (VCR-VLB).

The Security Register OTP Lock bits on the NVCR-OLB are One Time Programmable (OTP). They can be set to '1' individually; once set to '1', the corresponding 1-KByte Security Register is permanently locked and read-only. The default state of Security Register OTP Lock Bits is '0'.

The Security Register Volatile Lock bits in the VCR-VLB are configurable and the lock('1') / unlock('0') status is activated on the fly after the write to register operation. These bits are reset to their default unlock value of '0' after a power cycle, hardware reset or software reset sequence.

SECURITY REGISTERS	ADDRESS RANGE A[31:24] / A[23:16] [1]	SIZE
Security Register-1	00/001000h – 00/0013FFh	1K-Byte
Security Register-2	00/002000h – 00/0023FFh	1K-Byte
Security Register-3	00/003000h – 00/0033FFh	1K-Byte

Notes:

1. In Extended SPI 3-Byte Address Mode, the Security Registers are 3-Byte Address accessible, while in Extended SPI 4-Byte Address Mode and ODDR mode, access to the Security Registers requires 4-Byte Address input.

7.10 8-Byte CRC Register

The W35T51NW supports an 8-Byte CRC code that is stored in the CRC Register. The CRC code is calculated by executing the CRC-At-Rest Memory (9Bh) command and is stored in the CRC Register. The CRC Register is read by using the Read 8-Byte CRC Code (1Bh) command.

Address[1]	Name	Data 8	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1
24-bit Address or 32-bit Address	CRC Register[2]	00h	00h	00h	00h	00h	00h	00h	00h

Notes:

1. 000000h 24-bit Address input must be used in 3-Byte Address mode and 00000000h 32-bit Address input must be used in 4-Byte Address mode to read the CRC Register.
2. Default value is 00h.

7.11 256-Byte DLP Register

The W35T51NW supports a 256-Byte DLP Register that stores fine tuning data for enhancing high speed communication with the host. The DLP Register is read accessible by Read DLP (23h, 8Ch, 9Ch) commands. It is programmable by Program DLP Register (40h, 78h) commands and erasable by Erase DLP Register (B8h) command. The DLP Register is pre-programmed with the same pattern as the *e*·MMC HS200 standard twice.

Name	Address (A[23:8] / A[31:8])	Address (A[7:0])
DLP Register	xxxxh / xxxxxxh	00h – FFh

7.12 Error Code Correction (ECC) Registers

7.12.1 ECC Status Register – Volatile Writable and Readable

The W35T51NW provides a volatile ECC Status Register which consists of configuration and status bits for error correction and flash memory cell abnormality detection. Upon power up or after the execution of a Software/Hardware Reset, the ECC Status Register bits will be reset to their default value – SEC, DED, INT and ECCO bits default value is 0 and ECC bit default value is 1.

The Write ECC Status Register command (56h) is used to write to the writable bits of the ECC Status Register, namely ECC Enable bit (ER2) and Interrupt Enable bit (ER1).

The remaining ECC Register bits namely Single Error Correction bit (ER7), Double Error Detection bit (ER6), and ECC On/Off bit (ER0) are read status only bits. The Read ECC Status Register command (25h) is used to read the ECC Status Register.

It is important to note that when using 9Ch, 9Dh, FDh commands and any read commands with ODDR mode, the SEC, DED, and ECCO status bits will contain the (N+1) 16-byte aligned ECC information.

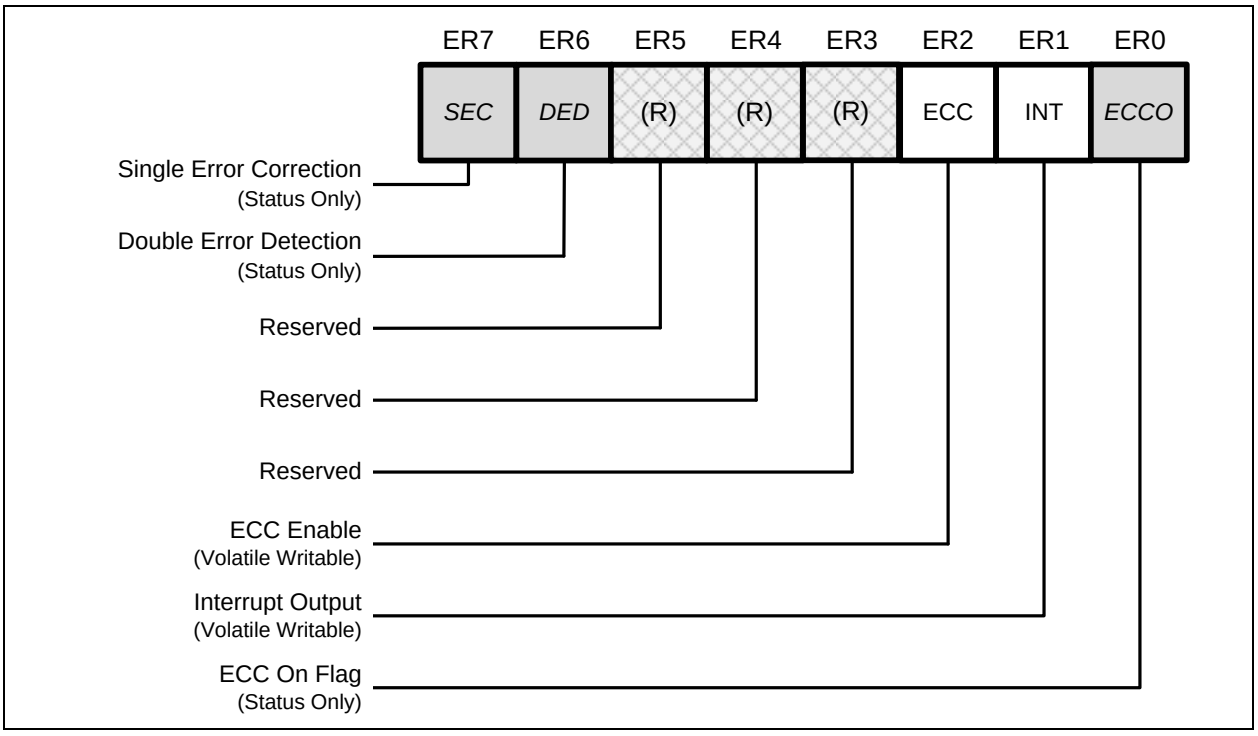


Figure 5-3. ECC Status Regsiter

7.12.1.1 ECC Status Bits (SEC, DED) – *Status Only*

SEC (Single Error Correction) and DED (Double Error Detection) Status Bits are used to show the ECC results for the last Read operation. SEC and DED bits will be cleared to 0 once the device accepts a new Read command.

SEC, DED	Definitions
0, 0	No ECC events in all aligned 16-Byte granularities.
1, 0	SEC events in single or multiple 16-Byte granularities, data is OK to use (unless it's odd bits error in 16-Byte granularity).
0, 1	DED events in single or multiple 16-Byte granularities, data contains 2 or more bits errors.
1, 1	SEC and DED events happened in separate single or multiple 16-Byte granularities, data contain 2 or more errors.

7.12.1.2 ECC Enable (ECC) – Volatile Writable by 56h

The on chip ECC engine can be enabled or disabled by the ECC Enable bit. When ECC bit is '1' (default), the ECC function is enabled to ensure data integrity and reliability. Each aligned 16-byte memory across the full memory range has an independent automatic ECC On/Off status bit in the ECC Status Register and an ECC On/Off Flag in the Advanced ECC Register as status detectors. When ECC is enabled, if more than one program operation per aligned 16-byte memory is performed, the ECC function for those aligned 16-byte memories will be automatically disabled during the read operation. During this read, the memory array content is transmitted without ECC calculation. When the ECC bit is '0', the ECC function is disabled during read memory but the number of programming attempts per aligned 16-byte memories is still tracked and recorded. Once ECC is enabled, aligned 16-byte memories that were programmed more than once when ECC was disabled, will automatically set ECC Off status for those particular aligned 16-byte.

7.12.1.3 Interrupt Pin Configuration (INT) – *Volatile Writable by 56h*

The hardware Interrupt Pin is used by the system to detect ECC events during Read operations when the ECC is enabled (ECC=1). When INT=0, the Interrupt Output Pin will be pulled low during the aligned 16-Byte data output period if there is a SEC (Single Error Correction) event within the 16-Byte ECC granularity. When INT=1, the Interrupt Output Pin will be pulled low for DED (Double Error Detection) events. When ECC is disabled (ECC=0), the INT bit value is ignored and Interrupt Output Pin is disabled.

7.12.1.4 ECC On/Off (ECCO) – Status Only

The ECC On/Off bit is a status indicator of whether the ECC function is active or inactive (disabled) on any of the 16-byte aligned memory from the last memory read operation. When ECC On/Off bit is '0' (default), the ECC function is active in all the 16-byte aligned memory from the last memory read operation. When ECC On/Off bit is '1', the ECC function has been turned off in one or more of the 16-byte aligned memory from the last memory read operation. The ECC On/Off bit is automatically turned off if any of the aligned 16-byte memory address ranges are programmed more than once before an erase operation.

7.12.2 Advanced ECC Register

The Advanced ECC Register is an 8-byte register that can be used as a supplemental tool to trace error code correction status of any aligned 16-byte memory (single error correction, double error detection, and ECC On/Off flag) from the target starting address. During a memory read operation, the corresponding address, counters, and valid captured address flags at the first ECC event are captured and stored in this register until a reset occurs.

The ECC (ER2) bit of ECC Status Register controls the ECC functionality of the device. When the ECC bit is a '1' (default), the Advanced ECC Register is enabled. When ECC is '0', the ECC functionality is disabled and the data in the Advanced ECC Register is invalid. The 8-byte Advanced ECC Register's default values from power up or reset are '0s'.

The Advanced ECC Register is partitioned into eight ECC Registers and are byte accessible using the Read Advanced ECC Register commands (7Dh) followed by a 24-bit or 32-bit ECC Register Address input based on the address mode setting. The ECC Register Address input targets the starting address of the Advanced ECC Register output. It is also a variable starting memory address to determine the ECC status of the target 16-byte aligned memory. Here are the details of the 8-byte Advanced ECC Register:

ECC Register 0 is accessible using the least significant ECC Register Address bits ERA[2:0]=000b and MSBs ERA[23:3] or ERA[31:3] (3-Byte Address or 4-Byte Address mode) as the target starting address. It contains the SACVF bit (EB7), the ECC flag status bits ECCOF (EB6), the DEDF (EB5), the SECF (EB4), and the Single Error Correction Register Address bits SRA25 and SR24 (EB1 and EB0).

The ECC flag status register bits, which are ECC On/Off Flag (ECCOF), Double Error Detection (DEDF), and Single Error Correction Flag (SECF) bits on ECC Register 0, provide the ECC status of the 16-byte aligned target address along with the ECC status of the next series of 16-byte aligned memory. These bits provide the error code correction status from the starting address in 16-byte alignment across the full memory array.

ECC Register 1 is accessible using the least significant ECC Register Address bits ERA[2:0]=001b and MSBs ERA[23:3] or ERA[31:3] (3-Byte Address or 4-Byte Address mode) as don't cares (x). It contains the Single Error Correction Address SRA[23:16] (EB [7:0]).

ECC Register 2 is accessible through the least significant ECC Register Address bits ERA[2:0]=010b with the MSBs ERA[23:3] for 3-Byte Address or ERA[31:3] for 4-Byte Address as don't cares (x). It contains the Single Error Correction Address SRA[15:8] (EB[7:0]).

ECC Register 3 is accessible through the least significant ECC Register Address bits ERA[2:0]=011b with the MSBs ERA[23:3] for 3-Byte Address or ERA[31:3] for 4-Byte Address as don't cares (x). It contains the Single Error Correction Address SRA[7:4] (EB[7:4]) and the Single Error Correction Counter SC[3:0] (EB[3:0]).

ECC Register 4 is accessible through the least significant ECC Register Address bits ERA[2:0]=100b with the MSBs ERA[23:3] for 3-Byte Address or ERA[31:3] for 4-Byte Address as the target starting address. It contains the DACVF bit (EB7), the ECC flag status bits ECCOF (EB6), the DEDF (EB5), the SECF (EB4), and the Single Error Correction Register Address bits DRA25 and DRA24 (EB1 and EB0).

The ECC flag status register bits, which are ECC On/Off Flag (ECCOF), Double Error Detection (DEDF), and Single Error Correction Flag (SECF) bits on ECC Register 0, provide the ECC status of the 16-byte aligned target address along with ECC status of the next series of 16-byte aligned memory. These bits provide the error code correction status from the starting address in 16-byte alignment across the full memory array.

ECC Register 5 is accessible through the least significant ECC Register Address bits ERA[2:0]=101b with the MSBs ERA[23:3] for 3-Byte Address or ERA[31:3] for 4-Byte Address as don't cares (x) . It contains the Double Error Detection Register Address DRA[23:16] (EB[7:0]).

ECC Register 6 is accessible through the least significant ECC Register Address bits ERA[2:0]=110b with the MSBs ERA[23:3] for 3-Byte Address or ERA[31:3] for 4-Byte Address as don't cares (x). It contains the Double Error Detection Register Address DRA[15:8] (EB[7:0]).

ECC Register 7 is accessible through the least significant ECC Register Address bits ERA[2:0]=111b with the MSBs ERA[23:3] for 3-Byte Address or ERA[31:3] for 4-Byte Address as don't cares (x). It contains the Double Error Detection Register Address DRA[7:4] (EB[7:4]) and the Double Error Detection Counter DC[3:0] (EB[3:0]).

The Read Advanced ECC Register command (7Dh) is used to read the 8-byte Advanced ECC Register in the single input SPI or in the ODDR mode. After an ECC read command, followed by a 24-bit or 32-bit address and the required dummy cycles, the 8-byte ECC Register output will then be shifted out.

The data output sequence of the Read Advanced ECC Register commands (7Dh) is as follows:

- The data output sequence is similar to the standard read memory command sequence as it sequentially read through the ECC Registers 0 to 7 and the linked target memory address within the 16-byte alignment as output.
- The data output sequence represents the linked 16-byte aligned memory ECC across the memory, from the ECC Register Address ERA[2:0] = 000b and MSBs ERA[23:3] or ERA[31:3] as the target address of the aligned 16-byte memory.
    - The first 16-byte output composes of two contiguous 8-byte Advanced ECC Register sequence that provides the ECC Flag Status (ECCOF, DEDF, and SECF) of the target ECC Register Address linked to the aligned 16-byte ECC memory and the captured addresses, counters, and flags to validate the captured addresses/counters (SRA[25:4], SC[3:0], DRA[25:4], DC[3:00], SACVF, and DACVF) with ECC error from the previous memory read operations. The captured addresses, counters, and captured addresses/counters valid flags are the same throughout the Advanced ECC Register read sequence.
    - The next 16-byte output sequence provides the ECC Flag Status (ECCOF, DEDF, and SECF) of the next 16-byte aligned memory after the target ECC Register Address. The remaining register output are the captured addresses, counters, and captured addresses/counters valid flags (SRA[25:4], SC[3:0], DRA[25:4], DC[3:00], SACVF and DACVF) are recurrence of previous captured ECC addresses and counters (from the previous 16-byte ECC addresses/counters). The next series of 16-byte output are similar data from successive 16-byte ECC memory alignment across the memory.

For detailed command sequence and timing diagram, refer to Section 9.12.4 Read Advanced ECC Register.

Register Name	24 or 32-Bit ECC Register Address[1]		8-Byte ECC Register Data								Description
	ERA[23/31:4]	ERA[3:0]	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0	
ECC[2,3] Register 0	ERA[23:4] or ERA[31:4]	x000b	SACVF[2,3]	ECCOF[2]	DEDF[2]	SECF[2]	(R)[4]	(R)[4]	SRA25[2,3]	SRA24[2,3]	ECC Flags and Single Error Correction Register Address SRA[25:24]
ECC[3] Register 1	ERA[23:4] or ERA[31:4]	x001b	SRA23	SRA22	SRA21	SRA20	SRA19	SRA18	SRA17	SRA16	Single Error Correction Register Address SRA[23:16]
ECC[3] Register 2	ERA[23:4] or ERA[31:4]	x010b	SRA15	SRA14	SRA13	SRA12	SRA11	SRA10	SRA9	SRA8	Single Error Correction Register Address SRA[15:8]
ECC[3] Register 3	ERA[23:4] or ERA[31:4]	x011b	SRA7	SRA6	SRA5	SRA4	SC3	SC2	SC1	SC0	SRA[7:4] & Single Error Correction Counter SC[3:0]
ECC[2,3] Register 4	ERA[23:4] or ERA[31:4]	x100b	DACVF[2,3]	ECCOF[2]	DEDF[2]	SECF[2]	(R)[4]	(R)[4]	DRA25[2,3]	DRA24[2,3]	ECC Flags and Double Error Detection Register Address DRA[25:24]
ECC[3] Register 5	ERA[23:4] or ERA[31:4]	x101b	DRA23	DRA22	DRA21	DRA20	DRA19	DRA18	DRA17	DRA16	Double Error Detection Register Address DRA[23:16]
ECC[3] Register 6	ERA[23:4] or ERA[31:4]	x110b	DRA15	DRA14	DRA13	DRA12	DRA11	DRA10	DRA9	DRA8	Double Error Detection Register Address DRA[15:8]
ECC[3] Register 7	ERA[23:4] or ERA[31:4]	x111b	DRA7	DRA6	DRA5	DRA4	DC3	DC2	DC1	DC0	DRA[7:4] & Double Error Detection Counter DC[3:0]

Notes:

1. The ECC Register Address input is also the linked start memory address targeting the 16-byte aligned memory for ECC Status. It is a variable input address that can start on any of the 8-ECC Registers or linked memory address.
2. The ECC Register Address input used to access ECC Register 0 is ERA[23:3] or ERA[31:3] & ERA[2:0] = 000b. The ECC Register Address input used to access ECC Register 4 is ERA[23:3] or ERA[31:3] & ERA[2:0] = 100b. When ERA[2:0] input is 000b or 100b, the corresponding output ECC flag status bits ECCOF, DEDF, and SECF will display the ECC status of the target 16-byte memory alignment. The remaining ECC Register 0 SACVF, SRA25 and SRA24 are recurring captured SEC address and valid flag bits; their values do not change with the change on ERA[23:3] or [ERA31:3] input(don't care) or continuous read. The remaining ECC Register 4 DACVF, DRA25, and DRA24 are also recurring captured DED address and valid flag bits; their values do not change with the change on ERA[23:3] or [ERA31:3] input(don't care) or during continuous Read Advanced ECC Status Register output sequence.
3. The remaining ECC Register bit values (SACVF, DACVF ECC addresses and counters) are recurring ECC address and counter values captured from previous memory reads with ECC event and will remain the same. The ECC Register Address input ERA[23:3] or ERA[31:3] are Don't Care (x) on ECC Register bits referring to captured SACVF, DACVF, ECC addresses and counters.
4. '(R)' is for Reserved.
5. When using the 9Ch, 9Dh, FDh and any ODDR read commands, the SACVF, SRA[25:4], SC[3:0], DACVF, DRA[25:4], and DC[3:0] bits will contain (N+1) 16-byte aligned ECC information.

Figure 5-4. Advanced ECC Register

7.12.2.1 SEC Address Captured Valid Flag (SACVF) – SEC Address Valid Flag

The SEC Address Captured Valid Flag (SACVF), bit 7 of the ECC Register 0, provides the status of the captured address from a Single ECC error event stored in the SRA[25:4] register from previous memory reads. When the SACVF bit is '1', the captured/stored address in SRA[25:4] is valid. When SACVF bit is '0' (default), the stored data in SRA[25:4] is invalid. The Reset ECC Counters (72h) command along with power on reset, software reset or hardware reset will clear this bit to '0'.

7.12.2.2 ECC Flag (ECCOF) – ECC On/Off Flag

The ECC On/Off Flag (ECCOF), bit 6 of the ECC Register 0 and ECC Register 4, indicates whether the ECC functionality of the target address within the current 16-byte aligned memory is enabled or disabled due to having 2 or more programming operations within this 16-byte aligned area. It is possible to obtain the ECCOF bit status of each of the 16-byte aligned memory across the full memory by targeting individual 16-byte aligned address or by performing continuous Advanced ECC Register read. When the ECCOF bit is '0' (default), the ECC functionality is enabled. When the ECCOF bit is '1', the ECC function is disabled.

7.12.2.3 Double Error Detection Flag (DEDF) – DED Status

The Double Bit Error Detection Flag (DEDF), bit 5 of the ECC Register 0 and ECC Register 4, is a double error detection indicator. When set to '1', a 2-bit error event had occurred at the target address within the current 16-byte aligned memory. It is possible to receive a DEDF status on each of the 16-byte aligned memory across the full array by targeting each individual 16-byte aligned address or by performing continuous Advanced ECC Register read. When DEDF bit is '0' (default), there is no 2-bit error event at the 16-byte aligned memory.

7.12.2.4 Single Error Correction Flag (SECF) – SEC Status

The Single Error Correction Flag (SECF), bit 4 of the ECC Register 0 and ECC Register 4, is a single bit error correction event indicator at the current 16-byte aligned area. It is possible to receive a SECF status of each of the 16-byte aligned memory across the full memory by targeting each individual 16-byte aligned address or by performing continuous Advanced ECC Register read. When SECF bit is '0' (default), there is no single bit error correction event at the 16-byte aligned memory. When this bit is '1', a single bit error correction had occurred at the 16-byte aligned memory.

7.12.2.5 Single Error Correction Register Address (SRA[25:4]) – Single ECC Address Location

The Single Error Correction Register Address (SRA[25:4]) stores the captured address of the first single error correction event that had occurred at previous read memory operations. The SRA[25:24] bits are at Bit 1 and Bit 0 of the ECC Register 0; the SRA[23:16] bits are from ECC Register 1; the SRA[15:8] bits are from ECC Register 2; the SRA[7:4] are EB[7:4] of the ECC Register 3.

7.12.2.6 Single Error Correction Counter (SC[3:0]) – Single ECC Counter

The Single Error Correction Counter (SC[3:0]) keeps track of the number of single error correction events from previous read memory operations. The default value of SC[3:0] bits from power up is 0000b. The SC[3:0] can count up to 15 SEC events. A count value greater than zero along with the SACVF bit being set to '1' indicate that the captured SRA[25:4] address and SC[3:0] values are valid. This is an active running counter that will not be reset after every read operation. If utilized, it is important to reset this counter after every read access. The SC[3:0] counter value is reset by Reset ECC Counters (72h) command, power on reset, or software/hardware reset.

7.12.2.7 DED Address Capture Valid Flag (DACVF) – DED Address Valid Flag

The DED Address Capture Valid Flag (DACVF) is a bit indicator that validates a captured address due a DED ECC error event stored in the DRA[25:4] register from previous memory reads. When the DACVF is '1', the address captured/stored in the DRA[25:4] register is valid. When DACVF is '0' (default), the stored address in the SRA[25:4] register is invalid. A Reset ECC Counters (72h) command, power on reset, software reset or hardware reset will clear this bit to '0'.

7.12.2.8 Double Error Detection Register Address (DRA[25:4]) – Double ECC Address Location

The Double Error Detection Register Address (DRA[25:4]) stores the address of the first double error correction event that occurred on previous read memory operations. The DRA[25:24] bits are at Bit 1 and Bit 0 of the ECC Register 4; the DRA[23:16] bits are at ECC Register 5; the DRA[15:8] bits are at ECC Register 6; the DRA[7:4] are at EB[7:4] of ECC Register 7.

7.12.2.9 Double Error Detection Counter (DC[3:0]) – Double ECC Detection Counter

The Double Error Detection Counter (DC[3:0]) keeps track of the number of double error detection events from a previous read memory operation. The default value of the DC[3:0] bits from power up is 0000b. The DC[3:0] can count up to 15 DED events. A count value greater than zero along with the DACVF bit being set to '1' indicate that the captured DRA[25:4] address and DC[3:0] values are valid. This is an active running counter that will not be reset after every read operation. If utilized, it is important to reset this counter after every read access. The DC[3:0] counter value is reset by Reset ECC Counters (72h) command, power on reset or hardware/software reset.

8. COMMANDS

The command set of W35T51NW consists of 56 basic commands (See Command Set Table) that are all supported in Extended SPI (SDR) mode. All commands are also supported in Octal DDR (ODDR) mode except for the two legacy SPI read commands 03h and 13h. The command sequences use Command, Address, or Data sequence with DDR option either driven by specific command in SDR or by register setting in ODDR during write and read protocols.

Commands vary in length from an 8-bit command code to several bytes and maybe followed by address input either in 24-bit (3-byte address mode) or 32-bit (4-byte address mode), data input/output, dummy cycles, or a combination of address, dummy cycles and data output. The data portion of the input varies in length, from 1 up to 256 bytes, depending on the target register/memory and command. For some register and memory reads, a preset number of dummy cycles are required before the data output. The number of dummy cycles for read memory commands are programmable using the Non-Volatile Configuration Register Address 05h or Volatile Configuration Register Address 05h.

Furthermore, command sequences are represented by the (C-A-D) or (Cd-Ad-Dd) command mode nomenclature format. This format indicates the number of active IO pins used for the Command (C), Address (A), and Data (D) while DDR is represented by (d).

Write sequences use the following input protocols:

- Command (C) Input only (1-0-0 in SDR or 8d-0-0 in ODDR)
- Command and Data (C-0-D) Input (1-0-1 in SDR or 8d-0-8d ODDR)
- Command, Address and Data (C-A-D) Input (1-1-1, 1-1-8, 1-8-8 in SDR or 8d-8d-8d in ODDR)

Read sequences use command, address, dummy cycles and data output protocols (dummy cycles are not included in the command nomenclature):

- Command and Data Output (C-D) for register reads (1-0-1 in SDR or 8d-0-8d in ODDR)
- Command, Address, and Data Output (C-A-D) for memory reads (1-1-1, 1-1-8, 1-8-8, 1-1d-8d, 1-8d-8d in SDR or 8d-8d-8d in ODDR); Dummy Cycle is required after address input

Commands are entered with the high to low transition of the Chip Select (/CS) pin, followed by the command opcode, address input/output, or data input/output if needed. Write commands are initiated when /CS pin is de-asserted. Register Writes are instantaneous while writes involving internal program or erase time require a wait time before new read memory or write commands are accepted. During an internal program or erase operation, only Read Status, Read Flag Register, and Suspend commands are accepted while other commands will be ignored until the internal program or erase is completed or suspended and device is ready for the next command.

Valid read commands are shifted in followed by address and dummy cycles if required. The transition from input to shifting data output either after the command, address or after a combination of command/address with dummy cycles. A low to high transition of the /CS pin during the read sequence brings the device to standby mode and ready to accept the next valid commands.

In SDR input mode, the command input sequence (C-A-D) is latched in either through the single bit IO0 or byte-wide IO[7:0] (depending on the I/O mode configuration – SPI or Octal SPI) on the rising edge of clock starting with the most significant bit (MSB). Command input sequences will always be in single bit SPI on IO0 using 8 CLKs. All of the commands are in single bit SPI mode except for the 1-1-8 / 1-8-8 Read commands (also the 1-1d-8d and 1-8d-8d DDR reads) and the 1-1-8 / 1-8-8 Page Program commands that transitions from single bit SPI to Octal SPI either during the address input or data input/output. Address input can either be set in 3-byte or 4-byte address mode.

In ODDR mode, the command, address, and data input sequences are latched using the byte-wide IO[7:0] on both rising and falling edges of clock; the byte-wide data output is also ready on both edges of clock. The byte command code is required to be latched in on both the rising and falling edge of the clock in ODDR. If a byte data is the size of the data input, it is also required to have the data input byte in the IO[7:0] bus on both the rising and falling edge of clock. ODDR mode only operates in 4-Byte Address mode, and it is latched on both the rising and falling edges of clock shifted-in byte increments (requiring 2 clocks).

The complete list of commands supported by the W35T51NW is shown in the Command Set Table. Detailed timing diagrams and implementation of each command in both SDR and ODDR mode (if supported) are shown in the Command Cycles section.

All read commands can be completed after any clocked bit. However, all commands that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked), otherwise, the command will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all commands except for Read Status Register are ignored until the program or erase cycle has completed.

8.1 Command Set Table

Command	Synchronous Bus Interface		Command Cycle Opcode	Address Cycle[2]	Dummy Cycle[3]	Data Cycle
	SDR (SPI / OSPI) (C-Ad-Dd)[1]	ODDR (Cd-Ad-Dd)[1]				
Software Reset Commands						
Enable Reset	1-0-0	8d-0-0	**66h**	-	-	-
Reset Device	1-0-0	8d-0-0	**99h**	-	-	-
Read ID Commands						
Read ID	1-0-1	8d-0-8d	**9Eh**	-	0(8)	1 to 6
Read JEDEC ID	1-1-1	8d-0-8d	**9Fh**	-	0(8)	1 to 6
Read Serial Flash Discovery Parameter (SFDP)	1-1-1	8d-8d-8d	**5Ah**	3[4]	8(8)	1 to 1024
Flag Register Commands						
Flag Register	1-0-1	8d-0-8d	**70h**	-	0(8)	1 to ∞
Clear Flag Register	1-0-0	8d-0-0	**50h**	-	-	-
Configuration Commands						
Read Status Register	1-0-1	8d-0-8d	**05h**	-	0(8)	1 to ∞
Write Status Register	1-0-0	8d-0-8d	**01h**	-	-	1
Read Non-Volatile Configuration Register	1-1-1	8d-8d-8d	**B5h**	3(4)	8	1 to ∞
Write Non-Volatile Configuration Register	1-1-1	8d-8d-8d	**B1h**	3(4)	-	1
Read Volatile Configuration Register	1-1-1	8d-8d-8d	**85h**	3(4)	8	1 to ∞
Write Volatile Configuration Register	1-1-1	8d-8d-8d	**81h**	3(4)	-	1
Pre-Write Setup Commands						
Write Enable	1-0-0	8d-0-0	**06h**	-	-	-
Write Disable	1-0-0	8d-0-0	**04h**	-	-	-
Write Enable for Volatile Status Register	1-0-0	8d-0-0	**08h**	-	-	-
Address Mode Commands						
Enter 4-Byte Address Mode	1-0-0	8d-0-0	**B7h**	-	-	-
Exit 4-Byte Address Mode	1-0-0	8d-0-0	**E9h**	-	-	-
SPI (1-1-1) Read Memory Only Commands						
Read Data	1-1-1	-	**03h**	3(4)	-	1 to ∞
Read Data with 4-Byte Address	1-1-1	-	**13h**	4	-	1 to ∞
Read Commands with 3-Byte or 4-Byte Address						
Fast Read	1-1-1	8d-8d-8d	**0Bh**	3(4)	8(16)	1 to ∞
Fast Read Octal-Output	1-1-8	8d-8d-8d	**8Bh**	3(4)	8(16)	1 to ∞
Fast Read Octal-I/O	1-8-8	8d-8d-8d	**CBh**	3(4)	16	1 to ∞
Fast Read DDR Single-Address-Input and Octal-Output	1-1d-8d	8d-8d-8d	**9Dh**	3(4)	8(16)	1 to ∞
Read Commands with 4-Byte Address						
Fast Read with 4-Byte Address	1-1-1	8d-8d-8d	**0Ch**	4	8(16)	1 to ∞
Fast Read Octal-Output with 4-Byte Address	1-1-8	8d-8d-8d	**7Ch**	4	8(16)	1 to ∞
Fast Read Octal-I/O with 4-Byte Address	1-8-8	8d-8d-8d	**CCh**	4	16	1 to ∞
Fast Read DDR Octal I/O with 4-Byte Address	1-8d-8d	8d-8d-8d	**FDh**	4	16	1 to ∞

Command Set Table 1 (Continuation)

Command	Serial Interface Mode		Command Cycle Opcode	Address Cycle[2]	Dummy Cycle[3]	Data Cycle
	SDR (SPI/ OSPI) (C-Ad-Dd)[1]	ODDR (Cd-Ad-Dd)[1]				
Program Memory Commands						
Page Program	1-1-1	8d-8d-8d	**02h**	3(4)	-	1 to 256
Page Program Octal Data	1-1-8	8d-8d-8d	**82h**	3(4)	-	1 to 256
Page Program Octal Address/Data	1-8-8	8d-8d-8d	**C2h**	3(4)	-	1 to 256
Page Program with 4-Byte Address	1-1-1	8d-8d-8d	**12h**	4	-	1 to 256
Page Program Octal Data with 4-Byte Address	1-1-8	8d-8d-8d	**84h**	4	-	1 to 256
Page Program Octal Address/Data with 4-Byte Address	1-8-8	8d-8d-8d	**8Eh**	4	-	1 to 256
Erase Memory Commands						
Sector Erase	1-1-0	8d-8d-0	**20h**	3(4)	-	-
32KB Block Erase	1-1-0	8d-8d-0	**52h**	3(4)	-	-
64KB Block Erase	1-1-0	8d-8d-0	**D8h**	3(4)	-	-
Sector Erase with 4-Byte Address	1-1-0	8d-8d-0	**21h**	4	-	-
32KB Block Erase with 4-Byte Address	1-1-0	8d-8d-0	**5Ch**	4	-	-
64KB Block Erase with 4-Byte Address	1-1-0	8d-8d-0	**DCh**	4	-	-
Chip Erase	1-0-0	8d-0-0	**C7h/60h**	-	-	-
Suspend/Resume Commands						
Erase / Program Suspend	1-0-0	8d-0-0	**75h**	-	-	-
Erase / Program Resume	1-0-0	8d-0-0	**7Ah**	-	-	-
Unique ID and Security Register						
Read Unique ID	1-1-1	8d-8d-8d	**4Bh**	3(4)	8(16)	1 to 16
Program Security Registers	1-1-1	8d-8d-8d	**42h**	3(4)	-	1 to 256
Erase Security Registers	1-1-0	8d-8d-0	**44h**	3(4)	-	-
Read Security Registers	1-1-1	8d-8d-8d	**48h**	3(4)	8(16)	1 to ∞
Deep Power-down Commands						
Power-down	1-0-0	8d-0-0	**B9h**	-	-	-
Exit Power-down	1-0-0	8d-0-0	**ABh**	-	-	-
Read Data Learning Pattern						
(1-1-1) Read DLP	1-1-1	-	**23h**	-	-	1 to ∞
(1-1-8) Read DLP	1-1-8	-	**8Ch**	-	8	1 to ∞
(1-1d-8d) or (8d-8d-8d) Read DLP	1-1d-8d	8d-8d-8d	**9Ch**	-	8(16)	1 to ∞
Program Data Learning Pattern						
(1-1-1) Program DLP Register	1-1-1	-	**40h**	3(4)	-	256
(1-1-8) or (8d-8d-8d) Program DLP Register	1-1-8	8d-8d-8d	**78h**	3(4)	-	256
Erase Data Learning Pattern						
(1-1-0) or (8d-8d-0) Erase DLP Register	1-1-0	8d-8d-0	**B8h**	3(4)	-	-
ECC Registers Commands						
Read ECC Status Register	1-0-1	8d-0-8d	**25h**		0(8)	1 to ∞
Write ECC Status Register	1-0-1	8d-0-8d	**56h**			1
Reset ECC Counters	1-0-0	8d-0-0	**72h**			
Read Advanced ECC Register	1-1-1	8d-8d-8d	**7Dh**	3(4)	8(16)	1 to ∞

Notes:

1. C**d**-A**d**-D**d format**: C stands for Command input; A stands for Address input; D stands for either Data input or Output; **d** stands for DDR. Extended SPI (SDR) can operate in (1-0-0), (1-1-0), (1-1-1), (1-1-8), (1-8-8), (1-1d-8d), or (1-8d-8d) IO interfaces, while Octal DDR (ODDR) can only operate in (8d-0-0), (8d-8d-0), or (8d-8d-8d) IO interfaces.
2. The x(y) format is used to define the Dual Address Byte Mode setting the device can operate in. 'x' is for 3-Byte Address Mode while 'y' is for 4-Byte Address Mode. ODDR mode operates in 4-Byte Address Mode only.

3. The x(y) format is used to define the Dummy Cycles used for SDR and ODDR modes. ‘x’ is the number of dummy cycles for SDR commands, while ‘y’ is for the number of dummy cycles in ODDR commands.
4. The Read SFDP command has a restriction where it can only accept 3-byte address, regardless of whether the device is configured to use 4-byte addressing mode. In Octal DDR mode, the address cycle will always be a fixed 4 bytes. Additionally, READ SFDP command requires exactly 8 dummy cycles and cannot be changed through the device's configuration registers. To determine the maximum clock frequency that can be used, please consult the Supported Clock Frequencies tables for 8 dummy cycles.

9. COMMAND CYCLES

9.1 Enable Reset (66h) and Reset Device (99h) Software Reset Commands

The W35T51NW supports a software Reset command in addition to the /RESET pin. Once the Reset command is accepted, any on-going internal operations are terminated, and the device will return to its default power-on state. All current volatile states will be lost and will return to their default power-up settings such as Status Register WEL and BUSY bits, Flag Register, Volatile Configuration Register, Volatile Block Lock bits.

The “Enable Reset (66h)” and “Reset Device (99h)” commands can be issued in either SPI or ODDR mode. In SDR mode, the software reset sequence is entered by driving the /CS pin low, followed by shifting in the Enable Reset command code ‘66h’ into IO0 on the rising edge of clock and driving the /CS pin high for tSHSL2 time. This is followed by the Reset Device command by driving the /CS pin low, followed by shifting in the Reset Device command code ‘99h’ into IO0 on the rising edge of clock. When /CS pin is driven high, software reset is accepted and the internal reset is executed internally. Figure 6-1a illustrates the SDR Software Reset sequence. The Software reset sequence initiation in ODDR mode is similar to SDR mode except the command code input sequence uses all 8-pins IO[7:0] and shifts in on both the rising and falling edge of clock. Figure 6-1b illustrates the ODDR Software Reset sequence.

To avoid accidental reset, both commands must be issued in sequence. Any commands other than “Reset Device (99h)” after “Enable Reset (66h)” will disable the “Reset Enable” state, and a new sequence of “Enable Reset (66h)” and “Reset (99h)” is needed to reset the device. Once the Reset command is accepted by the device, the /RSTO pin is driven low, no command will be accepted, and the device will take approximately tRST=30us to reset. Once the internal reset is completed, the /RSTO pin will transition from low to high impedance, the Flag Register Bit 7 (Ready Flag) outputs ‘1’ in a cycle of at least one full byte output, and the device becomes readily accessible.

Note that “Enable Reset (66h)” is not accepted when internal Write Status Register or Write Non-Volatile Configuration Register commands are being processed. Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when the Reset command sequence is accepted by the device. It is recommended to check the Status Register BUSY bit and the Flag Register SUS bit before issuing a Reset command sequence.

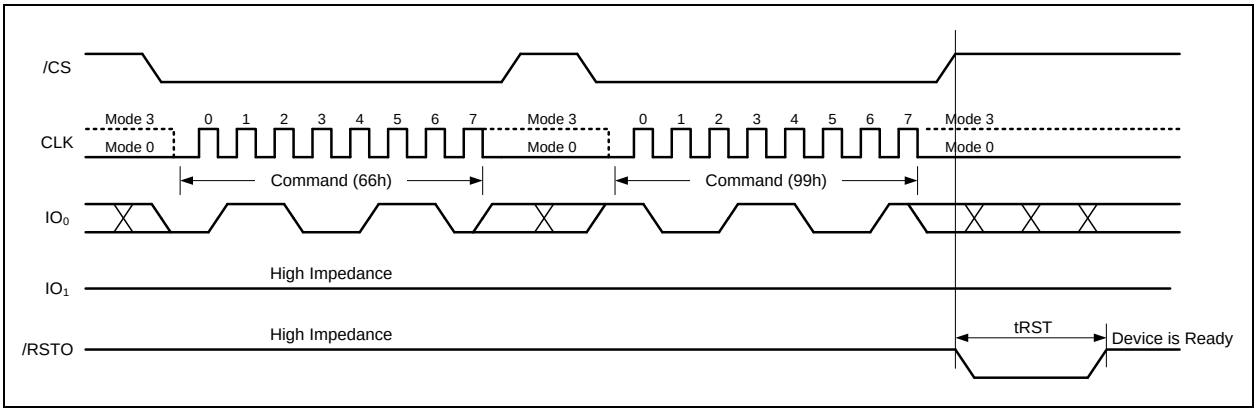


Figure 6-1a. Enable Reset and Reset Command Sequence (SDR Mode)

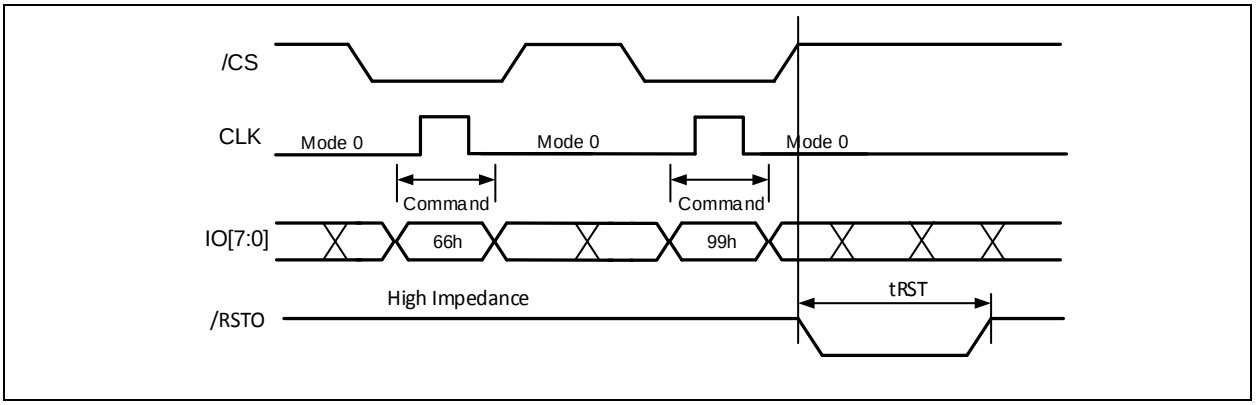


Figure 6-1b. Enable Reset and Reset Command Sequence (ODDR Mode)

9.2 Read ID Commands

The W35T51NW supports Read JEDEC ID and Read SFDP Register commands for device identification. Both commands are supported in SDR and ODDR mode.

9.2.1 Read JEDEC ID (9Fh) or Read ID (9Eh)

The W35T51NW supports Read JEDEC ID and Read ID command with command codes 9Fh and 9Eh to identify the device. The Read JEDEC ID command is backward compatible with the JEDEC standard for SPI compatible serial memories. The first 3-bytes include Manufacturer ID, Memory Type and Memory Density in SDR mode. An expanded ID with 3-Byte Device Information consisting of Expanded ID Size, Device Block Size Partition, and Device Configuration is also supported.

In SDR mode, the command is initiated by driving the /CS pin low and shifting the command code '9Fh' or '9Eh' using the IO0 pin. The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes, Memory Type and Capacity are shifted out, followed by the Expanded ID Size, Device Block Size Partition, and Device Configuration on IO1 pin at the falling edge of CLK with most significant bit (MSB) first. The JEDEC Read ID command is ended by a low to high transition of the /CS pin.

The Read JEDEC ID (Read ID) sequence in ODDR mode is similar to SDR mode except for the IO configuration and dummy cycles used. ODDR Read JEDEC ID is entered using the following sequence: drive the /CS pin low; shift command code '9Fh' or '9Eh' using IO[7:0] pins on the rising and falling edge of clock; follow with 8-dummy cycles. The JEDEC ID data outputs on both edges of clock. The ODDR JEDEC Read ID operation ends by the low to high transition of the /CS pin. Read JEDEC ID (Read ID) sequences in SDR and ODDR mode are illustrated in Figure 7-1a and 7-1b.

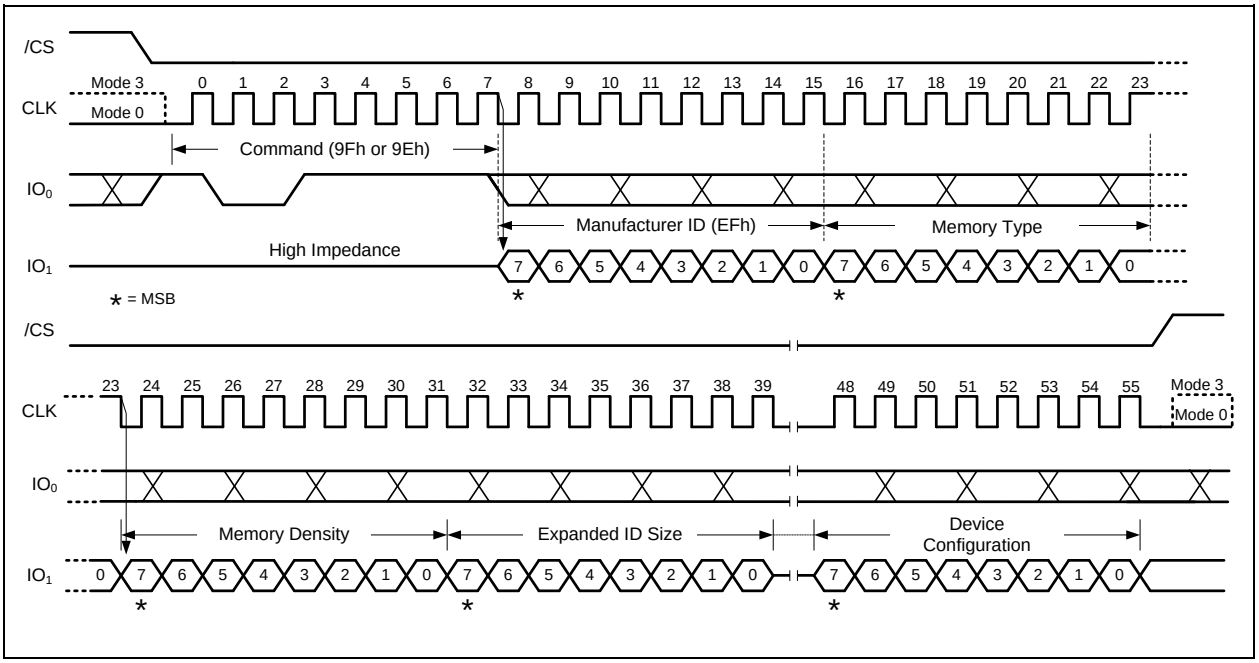


Figure 7-1a. Read JEDEC ID 9Fh (Read ID 9Eh) Command (SDR Mode)

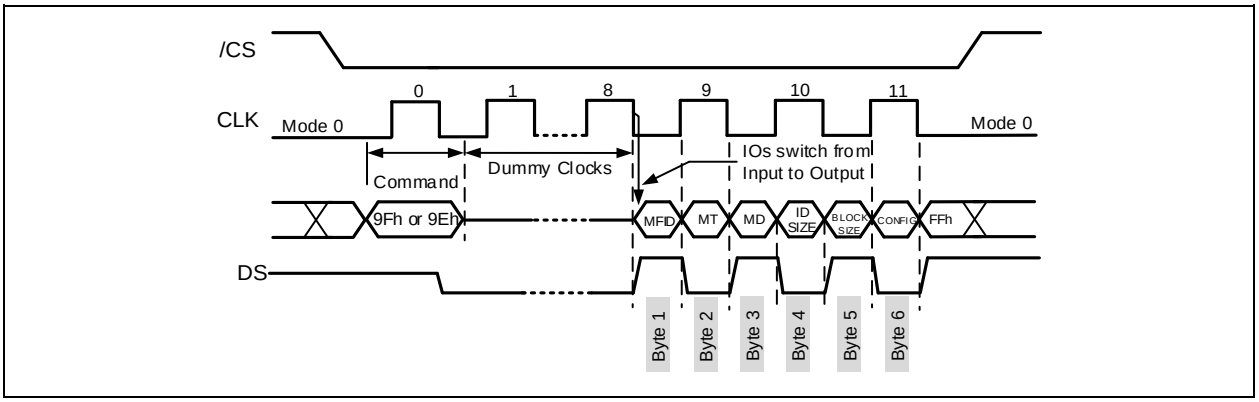


Figure 7-1b. Read JEDEC ID 9Fh (Read ID 9Eh) Command (ODDR Mode)

9.2.2 Read SFDP Register (5Ah)

The W35T51NW features a 1-KByte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, features, and available commands. The SFDP parameters are stored in a separate area from the memory array.

The Read SFDP Register command is compatible with the SFDP standard established in 2010, as well as subsequent JEDEC standard revisions JESD216/216A-F.

In SDR mode, the Read SFDP command is initiated by driving the /CS pin low and shifting the command code “5Ah” using IO0 followed by the 24-bit address input. Eight “dummy” clocks are required before the SFDP register contents starts shifting output data on IO1 from the target address on the falling edge of clock with most significant bit (MSB) first as illustrated in Figure 7-2a.

In ODDR mode, the Read SFDP command is performed with this sequence: /CS pin driven low; Read SFDP command code ‘5Ah’ shifted using IO[7:0] on both the rising and falling edge of clock; followed by a 32-bit address on both clock edges; 8-clock dummy cycles; then output SFDP data from the target starting address through IO[7:0] on both clock edges. The command is ended by a low to high transition on the /CS pin.

The Read SFDP command does not support the wrap around sequence. Once data output reaches the highest address, 1024, the data output will be FFh. The Address Mode and Wrap-Around Mode Configuration settings in the Non-Volatile Configuration and Volatile Configuration Register do not apply to the Read SFDP Register command. Figure 7-2b illustrates the Read SFDP Register in ODDR mode.

Since the Read SFDP command supports a non-programmable 8 dummy cycles after the address input, the maximum clock speed is the same as the frequencies listed under 8 dummy cycles in Section 7.5.1.2 and 7.5.1.3 Clock Frequency tables.

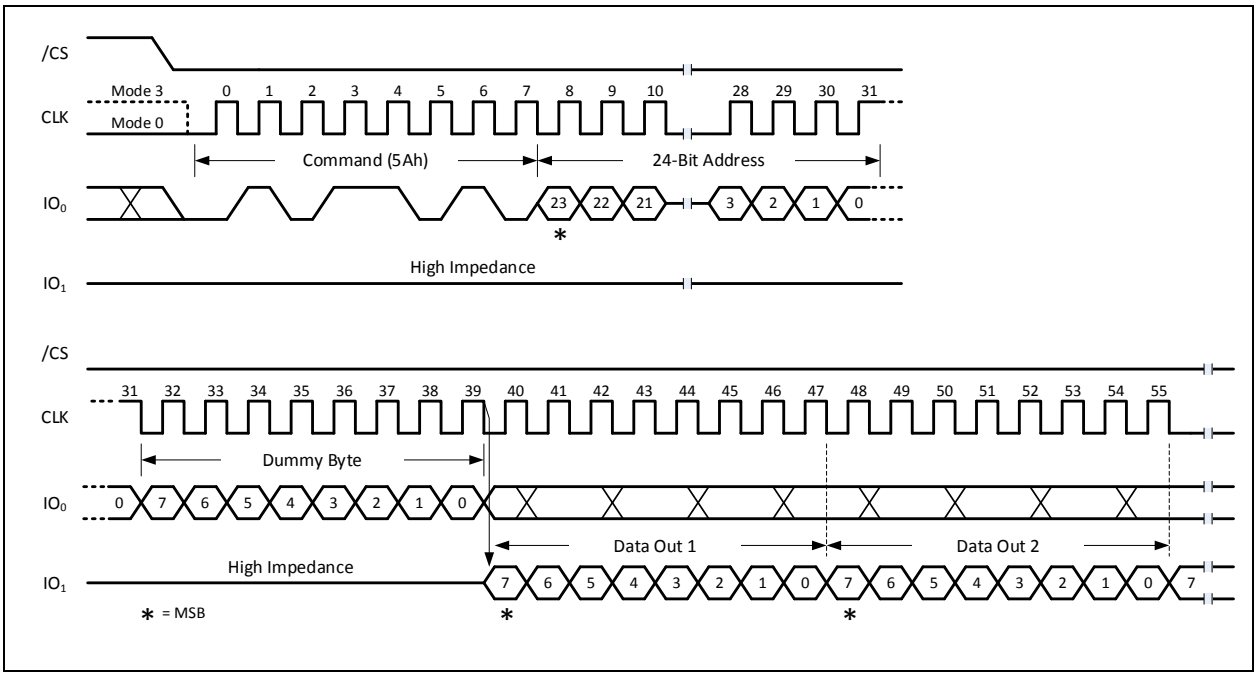


Figure 7-2a. Read SFDP Register Command Sequence (SDR Mode)

24-Bit Address input only even when device is operating in 4-Byte Address Mode

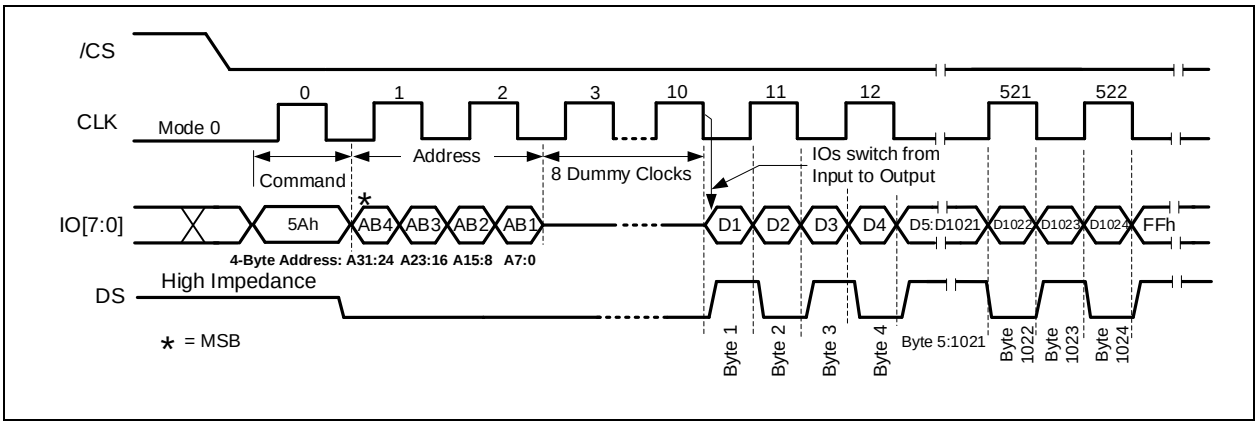


Figure 7-2b. Read SFDP Register Command Sequence (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR Mode

9.3 Flag Register, Status Register and Configuration Registers Commands

There are 4 registers associated with device configuration and operating status. These registers are accessed and controlled by read and write commands. The Flag Register is accessible by the Read Flag Register and Clear Flag Register commands. The Status Register is accessible by the Status Register and Write Status Register commands. The Non-Volatile Configuration Register is accessible by Read Non-Volatile Configuration Register and Write Non-Volatile Configuration Registers. The Volatile Configuration Register is accessible by Read Volatile Configuration Register and Write Volatile Configuration Register commands. These commands are all supported in either SDR or ODDR mode. Detailed information is in Section 7 Registers.

9.3.1 Read Flag Register (70h)

The Flag Read Register command reads and provides the current state of the 8-bit Flag Register. The command is entered by driving /CS low. In SDR mode, the Read-Flag Register command code '70h' is shifted into the IO0 pin on the rising edge of CLK. The flag register bits are then shifted out on the IO1 pin at the falling edge of CLK with the most significant bit (MSB) first as illustrated in Figure 8-1a. In ODDR mode, the command code '70h' is shifted using the IO[7:0] pins on both the rising and falling edge of CLK along with the required 8 dummy clock cycles before the Flag Register bits are shifted out from the IO[7:0] pins. Figure 8-1b illustrates the Read-Flag Register sequence in ODDR mode.

The Read-Flag Register command can be used even while internal Program, Erase or Writes to Registers are in progress. This allows error and Flag Register bits to be checked to determine whether a cycle has completed and that the device can accept new commands. The Flag Register can be read continuously as illustrated in Figure 8-1a and 8-1b. The command is completed by driving the /CS pin high.

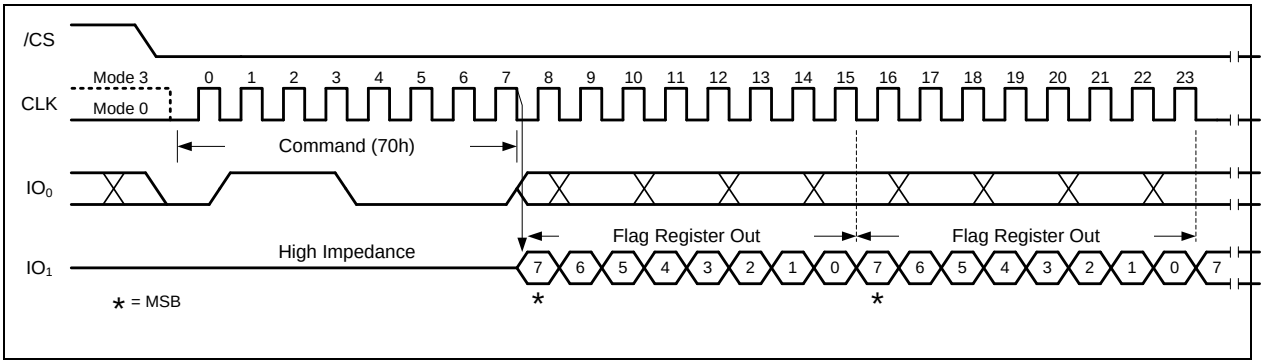


Figure 8-1a. Read Flag Register Command (SDR Mode)

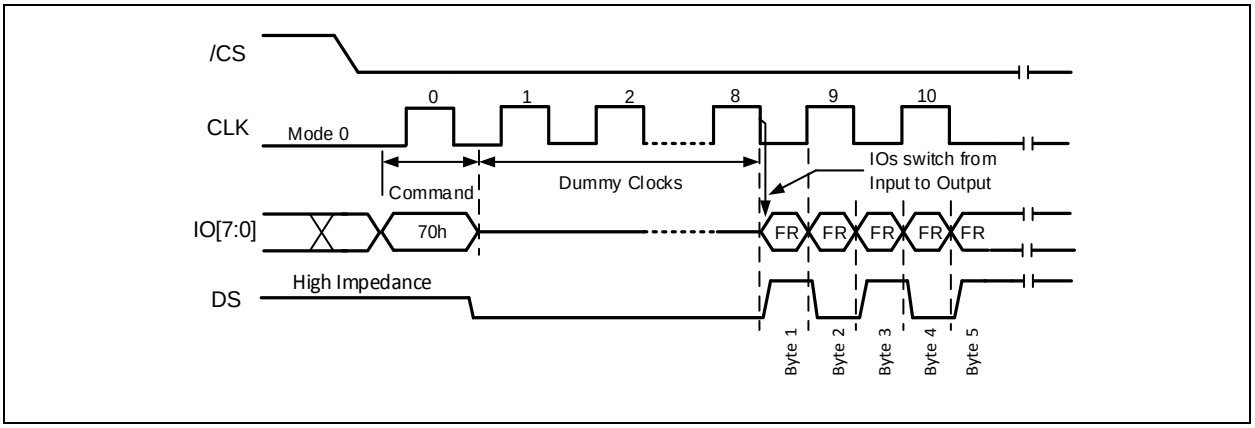


Figure 8-1b. Read Flag Register Command (ODDR Mode)

9.3.2 Clear Flag Register (50h)

The Clear Flag Register command clears or resets the Flag Register's error flag bits 5, 4, 3 and 1 (Erase Flag, Program Flag, CRC-In-Transit Flag, and Protected Memory Access Flag). Note that there are other device operations that indirectly set and clear the Flag Register bits that include Program Suspend, Erase Suspend, internal Program/Erase/Non-Volatile Write/CRC cycle status, and Address Mode settings.

In SDR mode, the Clear Flag Register command (Figure 8-2 Left) is entered by driving the /CS pin low, shifting the command opcode "50h" using the IO0 pin on the rising edge of CLK, and subsequently driving the /CS pin high to execute the command.

In ODDR mode, the Clear Flag Register command is entered by driving the /CS pin low, followed by shifting the command opcode '50h' using the IO[7:0] pins on both the rising and falling edge of CLK, and then driving the /CS pin high to execute the command. Refer to Figure 8-2 Right.

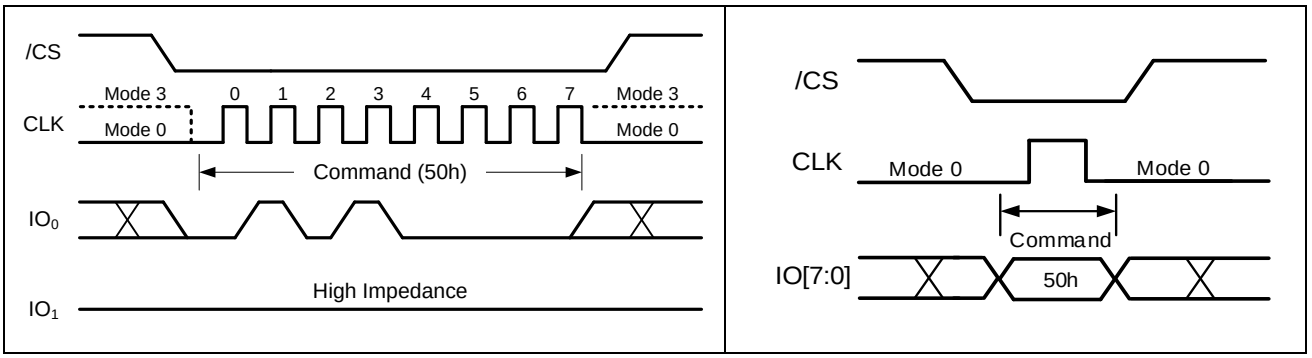


Figure 8-2. Clear-Flag Register Command for SDR Mode (left) or ODDR Mode (right)

9.3.3 Read Status Register (05h)

The Read Status Register command allows the 8-bit Status Register to be read. The command is entered by driving /CS pin low. In SDR mode, command code “05h” for Status Register is shifted using the IO0 pin on the rising edge of CLK. The status register bits are then shifted out on the IO1 pin on the falling edge of CLK with most significant bit (MSB) first as illustrated in Figure 8-3a. In DDR mode, command code “05h” for Read Status Register is shifted using the IO[7:0] pins on both the rising and falling edge of CLK. The Status Register bits state are then shifted out on the IO[7:0] pins on every rising and falling edge of CLK after 8-dummy clock cycles as illustrated in Figure 8-3b. Refer to Section 7.1 for Status Register description.

The Read Status Register command may be used at any time, even while an internal program, erase or write on Non-Volatile Registers cycle is in progress. The BUSY bit of the Status Register provides the status when an internal program, erase or write operation is ongoing or completed. When the internal write is completed, the device is ready to accept another command. The Status Register can be read continuously, as illustrated in Figure 8-3a and 8-3b. The command is completed by driving the /CS pin high.

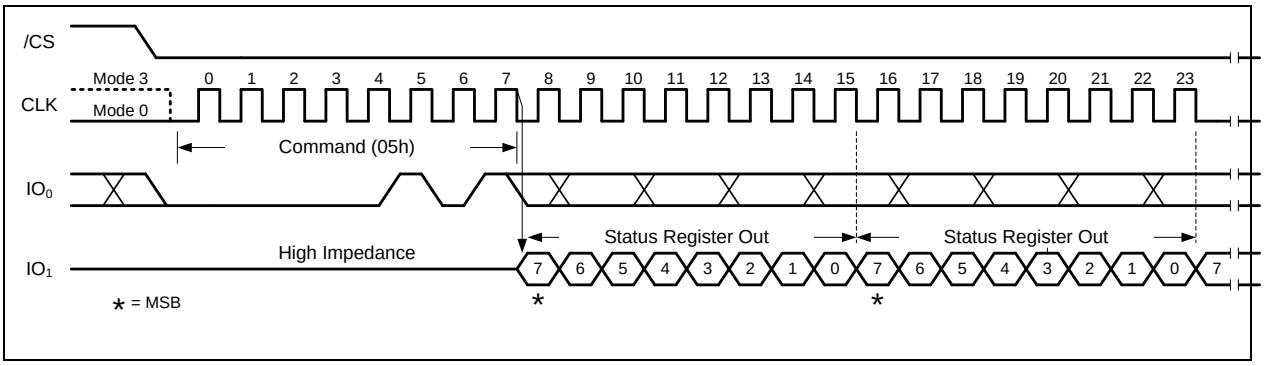


Figure 8-3a. Read Status Register Command (SDR Mode)

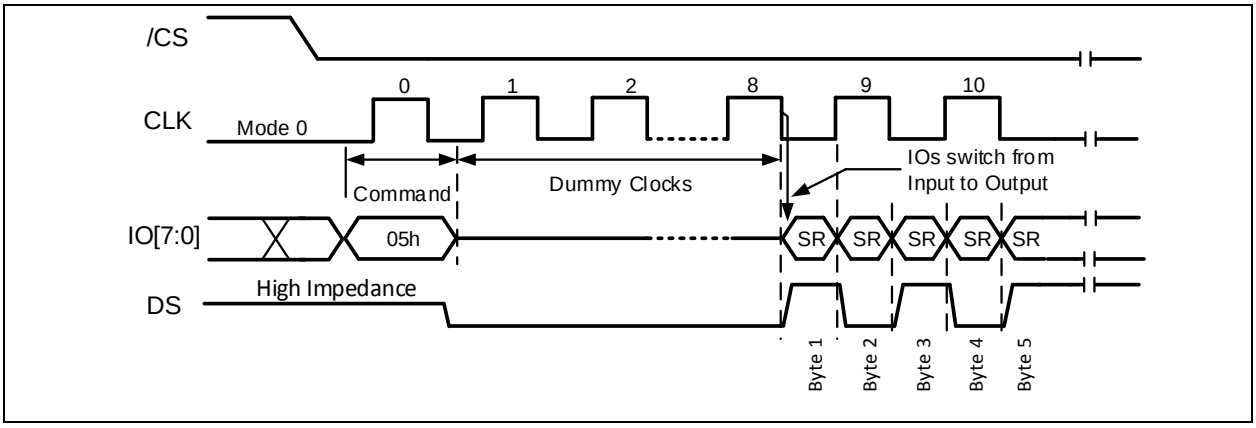


Figure 8-3b. Read Status Register Command (ODDR Mode)

9.3.4 Write Status Register (01h)

The Write Status Register command writes to the Status Register non-volatile bits. The writable Status Register bits include: SRP, TB, and BP[3:0].

To write the non-volatile Status Register bits, a Write Enable (06h) command must be first executed for the device to accept the Write Status Register command (Status Register WEL bit must equal '1'). In SDR mode and once the device is write enabled, the command is entered by driving the /CS pin low, shifting in the command code '01h' followed by the byte (setting) to be written to the Status Register into the IO0 pin on rising edge of the CLK. The Write Status Register command is executed when the /CS pin is driven high as illustrated in Figure 8-4a.

In ODDR mode, the Write Status Register sequence is similar to its SDR mode sequence except for the IO configuration and latch in sequence. The Write Status Register command sequence is entered by driving the /CS pin low, followed by the command code '01h' using IO[7:0] pins on both the rising and falling edge of CLK and by the byte (setting) to be written to the Status Register into the IO[7:0] pins also on both the rising and falling edge of CLK. The Write Status Register command is executed when /CS pin is driven high as illustrated in Figure 8-4b.

During the non-volatile Status Register write operation (06h followed by 01h) and after the /CS pin is driven high, the self-timed Write Status Register cycle will commence for a time duration of tw (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register command may still access the Status Register and check the BUSY bit status. When the BUSY bit is '1' during the Write Status Register command cycle, the device is busy with the internal write operation. When the BUSY bit transitions from '1' to '0', the write cycle is completed and the device is ready to accept other commands. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0. Refer to Section 7.1 for Status Register description.

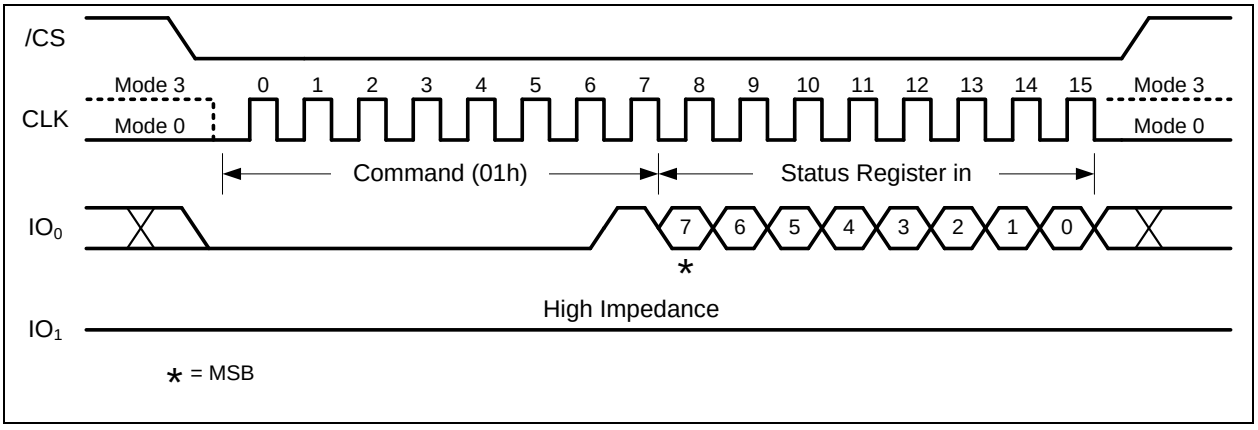


Figure 8-4a. Write Status Register Command (SDR Mode)

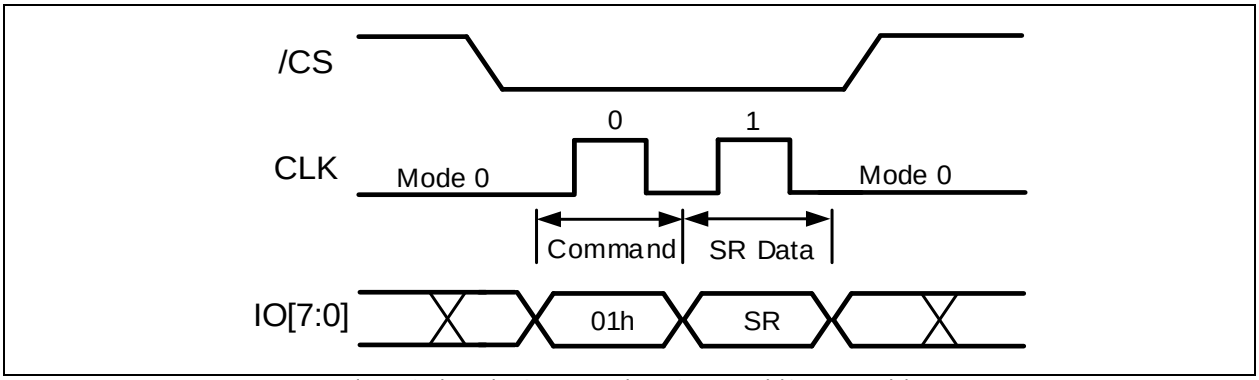


Figure 8-4b. Write Status Register Command (ODDR Mode)

9.3.5 Read Non-Volatile Configuration Register (B5h)

The Read Non-Volatile Configuration Register (Read-NVCR) reads the 256-byte Non-Volatile Configuration Register (NVCR) used to store the default settings of the device after power-up or reset. The read data size is only one byte from the target address and the same data byte will output continuously. The Read-NVCR is supported in both SDR and ODDR modes.

In SDR mode, the Read-NVCR command sequence is initiated by the following sequence: Drive the /CS pin low; shift-in the Read-NVCR command code “B5h” using the IO0 pin on the rising edge of CLK; shift into the IO0 pin on the rising edge of CLK either the 24-bit or 32-bit address (depending on the Address Mode Configuration setting) and the required 8-dummy CLK cycles. The NVCR data will start shifting out on the IO1 pin on the falling edge of CLK with the most significant bit (MSB) first from the target address as illustrated in Figure 8-5a.

In ODDR mode, the Read-NVCR command sequence is initiated by the following sequence: Drive the /CS pin low; shift-in the Read NVCR command code “B5h” into the IO[7:0] pins on both the rising and falling edge of CLK; shift the 32-bit Address on both the rising and falling edge of CLK; and shift in 8-dummy CLK cycles. The NVCR data will start shifting out on the IO[7:0] pins on both the falling and rising edge of CLK from the target address as illustrated in Figure 8-5b.

The Read NVCR will shift-out the same data byte continuously as illustrated in Figure 8-5a and 8-5b. The command is completed by driving the /CS pin high.

Refer to Section 7.4 for Non-Volatile Configuration Register description.

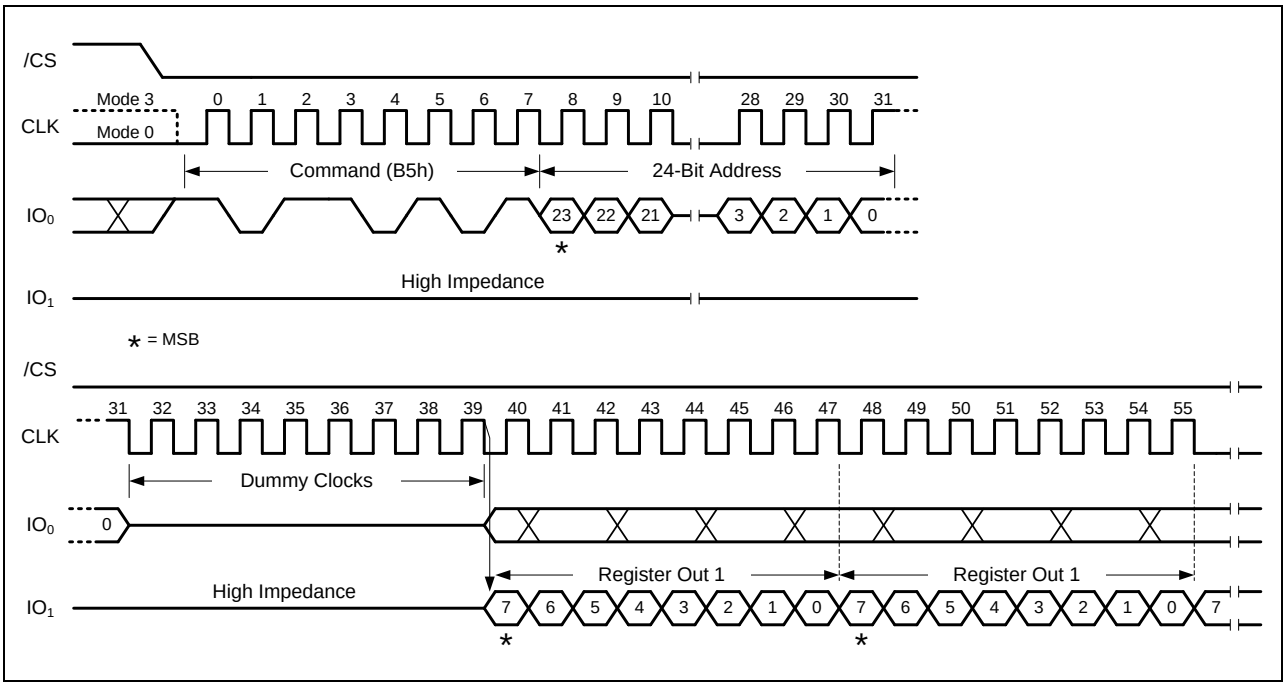


Figure 8-5a. Read Non-Volatile Configuration Register Command (SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

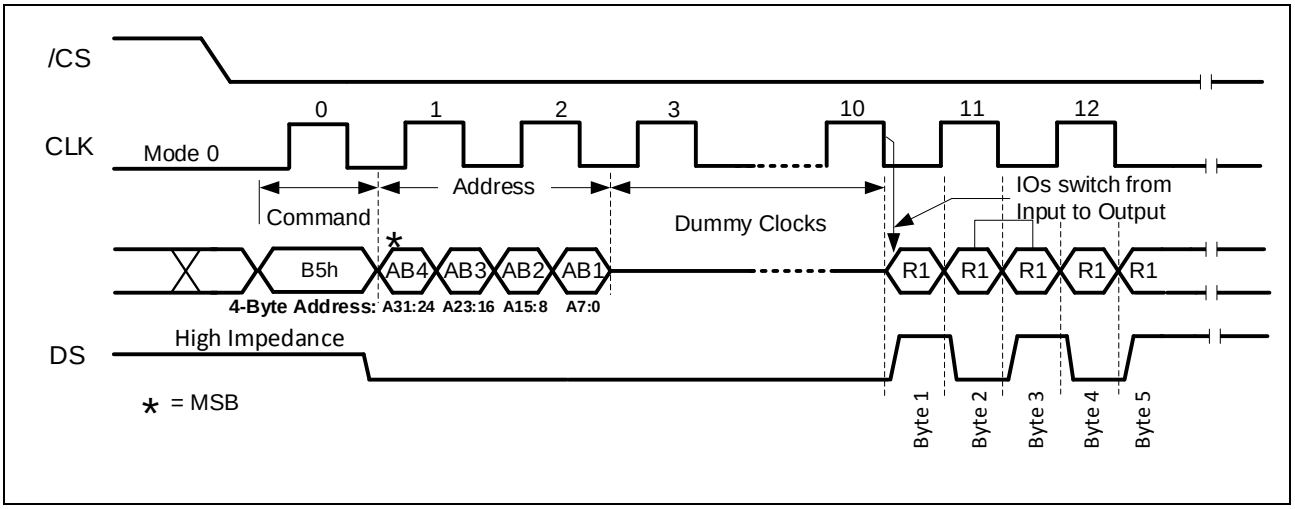


Figure 8-5b. Read Non-Volatile Configuration Register Command (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR mode

9.3.6 Write Non-Volatile Configuration Register (B1h)

The Write Non-Volatile Configuration Register (Write-NVCR) command individually writes a byte of data in a target address within the 256-byte Non-Volatile Configuration Register. The writable Non-Volatile Configuration Register addresses are as follows: Address 00h (IO mode), 01h (Dummy Clock Cycles), 03h (Drive Strength), 05h (Address Mode), 06h (XIP Configuration) and 07h (Wrap-Around Mode). Address[08h:FFh] are Reserved (FFh value) and not writable. To write the Non-Volatile Configuration Register, a standard Write Enable (06h) command must be first executed (Status Register WEL bit must equal '1').

In SDR mode and with the device write enabled (WEL bit = 1), the command is entered by the following sequence: drive the /CS pin low; shift-in on IO0 on the rising edge of CLK the command 'B1h', a 24-bit or 32-bit address (depending on Address Mode Configuration), a data byte, and subsequently drive /CS pin high to initiate the internal Non-Volatile Configuration Register write cycle as illustrated in Figure 8-6a.

In ODDR mode, the Write-NVCR command is entered by the following sequence: drive the /CS pin low; shift-in command code 'B1h' on IO[7:0] on both the rising and falling edge of CLK; continue to shift-in a 32-bit address on IO[7:0] pins on both the rising and falling edge of CLK; shift-in a byte of data on both the rising and falling edge of CLK; and subsequently drive the /CS pin high to initiate the internal Non-Volatile Configuration Register write cycle as illustrated in Figure 8-6b.

During the Non-Volatile Configuration Register internal write operation, after the /CS pin is driven high, the self-timed Write Configuration Register cycle will commence for a duration of tw (See AC Characteristics). While the Write Non-Volatile Configuration Register cycle is in progress, the Read Status Register and Read Flag Register commands may still access the Status Register and Flag Register to check the BUSY status and Ready Flag status. When the BUSY bit is '1' during the Write Non-Volatile Configuration Register command cycle, the device is busy with the internal write operation. When the BUSY bit transitions from '1' to '0', the write cycle has completed, and the device is ready to accept other commands. Alternatively, the Ready Flag is '0' when busy, and '1' when write operation is complete. After the write cycle completion, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

Writes to the 'Reserved' Address settings of the Non-Volatile Configuration Register are ignored, the Flag Register Bit 1 (PMAF) is set to '1' and the Status Register Bit 1 (WEL bit) is cleared to '0'.

The Non-Volatile Configuration Register holds the device configuration setting from power up. When performing an update with the Non-Volatile Configuration Register settings, extra precaution is required to ensure the internal Write-NVCR cycle is not interrupted by a power loss or hardware reset (recommended

stable power). If the internal Write-NVCR cycle is interrupted, the device configuration settings could be corrupted. The device can power up in an unknown state resulting in the device not being accessible by set commands in SDR or ODDR mode.

Section 6.6 Interface Recovery due to Hardware Interruption provides a method to recover the device interface if the device powered up in an unknown state due to Non-Volatile Configuration Register corruption.

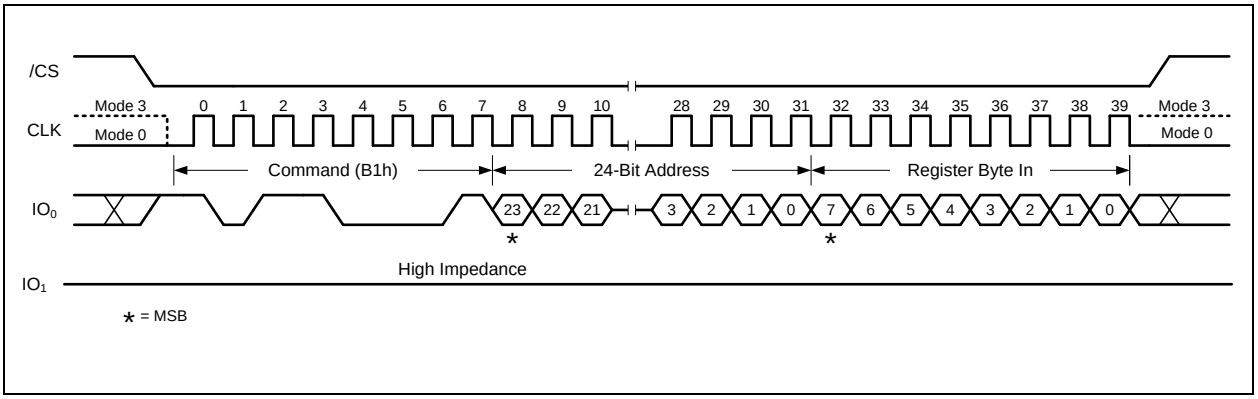


Figure 8-6a. Write Non-Volatile Configuration Register Command (SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

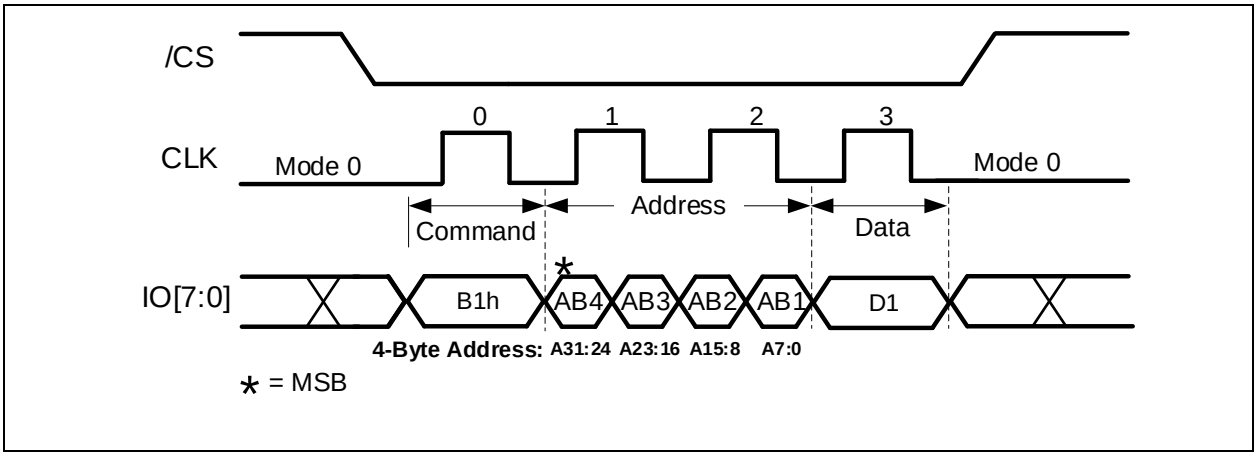


Figure 8-6b. Write Non-Volatile Configuration Command (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR mode

9.3.7 Read Volatile Configuration Register (85h)

The Read Volatile Configuration Register (Read-VCR) reads the 256-byte Volatile Configuration Register (VCR) used to configure or change device settings (IO Mode Configuration, Dummy Clock Cycle for memory read, Address Mode Configuration, XIP Configuration, Wrap-Around Mode) after power up. The read data size is only one byte from the target address and the same data byte will output continuously. The Read-VCR is supported in either SDR or ODDR mode.

In SDR mode, the Read-VCR command is initiated by the following sequence: Drive the /CS pin low; shift-in Read-VCR command code “85h” into the IO0 pin on the rising edge of CLK; shift into IO0 pin on rising edge of CLK either the 24-bit or 32-bit address (depending on Address Mode Configuration setting) input and the required 8-dummy CLK cycles. The VCR data will start shifting out on IO1 pin on the falling edge of CLK with the most significant bit (MSB) first from the target address as illustrated in Figure 8-7a.

In ODDR mode, the Read-VCR command is initiated by the following sequence: Drive the /CS pin low; shift-in the Read VCR command code “85h” into the IO[7:0] pins on both the rising and falling edge of CLK; shift the 32-bit Address on both the rising and falling edge of CLK, and the 8-dummy CLK cycles. The VCR output will start shifting out on IO[7:0] pins on both the falling and rising edge of CLK from the target address as illustrated in Figure 8-7b.

The Read VCR will shift-out the same data output continuously as illustrated in Figure 8-7a and 8-7b. The command is completed by driving the /CS pin high.

Refer to Section 7.5 for Volatile Configuration Register description.

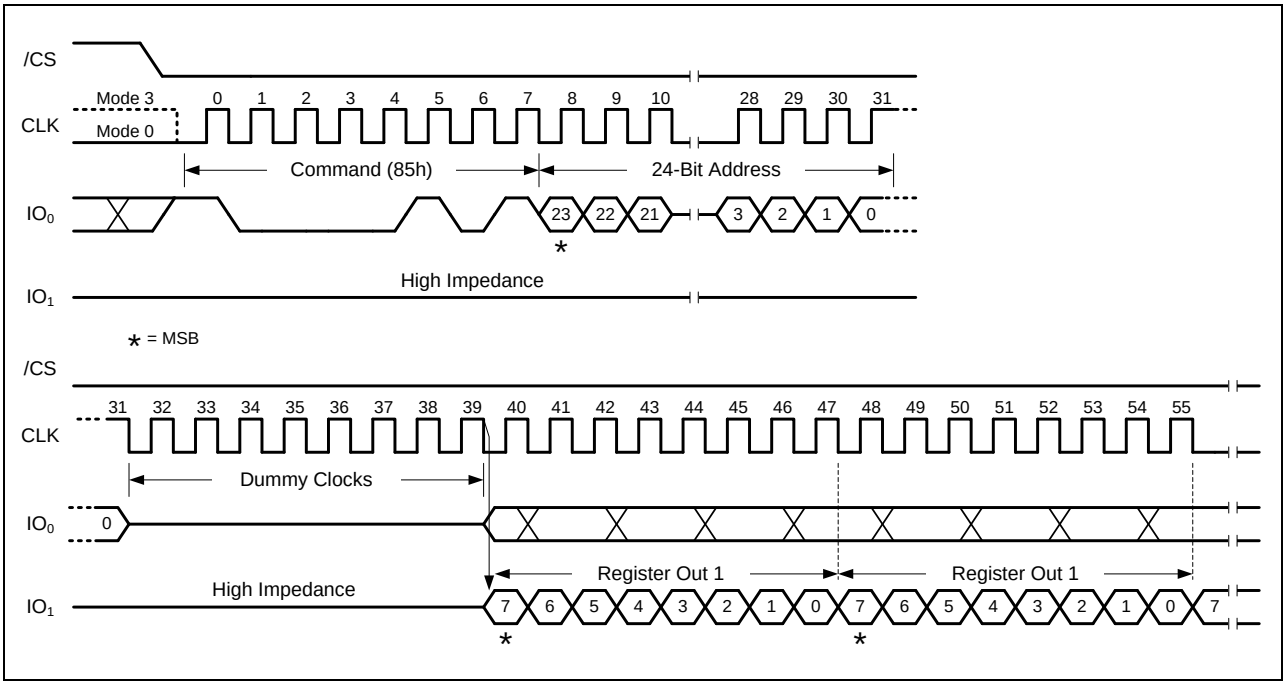


Figure 8-7a. Read Volatile Configuration Register Command (SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

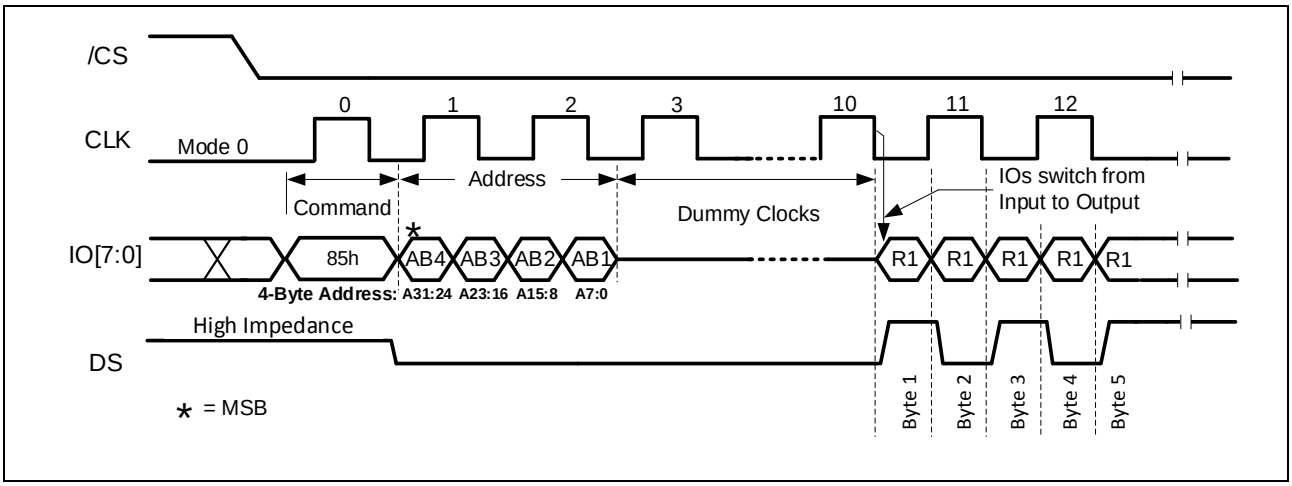


Figure 8-7b. Read Volatile Configuration Register Command (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR mode

9.3.8 Write Volatile Configuration Register (81h)

The Write Volatile Configuration Register (Write-VCR) command writes a byte of data to a targeted address within the 256-byte Volatile Configuration Register. The writable Volatile Configuration Register addresses are Address[00h:07h]. Address[08h:FFh] are Reserved (FFh value) and not writable. To write to the Volatile Configuration Register, a standard Write Enable (06h) command must be first executed (Status Register WEL bit must equal '1').

In SDR mode and with device write enabled (WEL bit = 1), the command is entered by the following sequence: drive the /CS pin low; shift-in on IO0 on the rising edge of CLK the command code '81h', shift a 24-bit or 32-bit address (depending on Address Mode Configuration), a data byte; and subsequently drive the /CS pin high to execute the Write Volatile Configuration Register command as illustrated in Figure 8-8a.

In ODDR mode, the ODDR Write-VCR command is entered by the following: drive the /CS pin low; shift-in command code '81h' using IO[7:0] on both the rising and falling edge of CLK; continue to shift-in a 32-bit address using IO[7:0] pins on both the rising and falling edge of CLK; followed by shifting-in a byte on both the rising and falling edge of CLK; and subsequently drive the /CS pin high to execute the Write Volatile Configuration Register command as illustrated in Figure 8-8b.

The Write Volatile Configuration Register command is a write to a volatile register address location. A minimum tSHSL2 time of 30 ns (see AC Characteristics) is needed to complete the write. After the write cycle completion, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

Writes to the 'Reserved' Addresses of the Non-Volatile Configuration Register are ignored, the Flag Register Bit 1 (PMAF) is set to '1', and Status Register Bit 1 (WEL bit) is cleared to '0'.

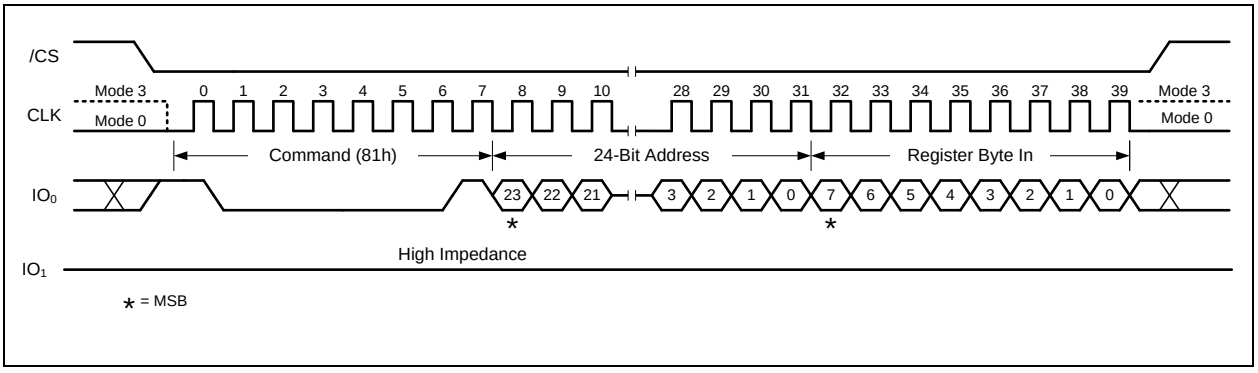


Figure 8-8a. Write Volatile Configuration Register Command (SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

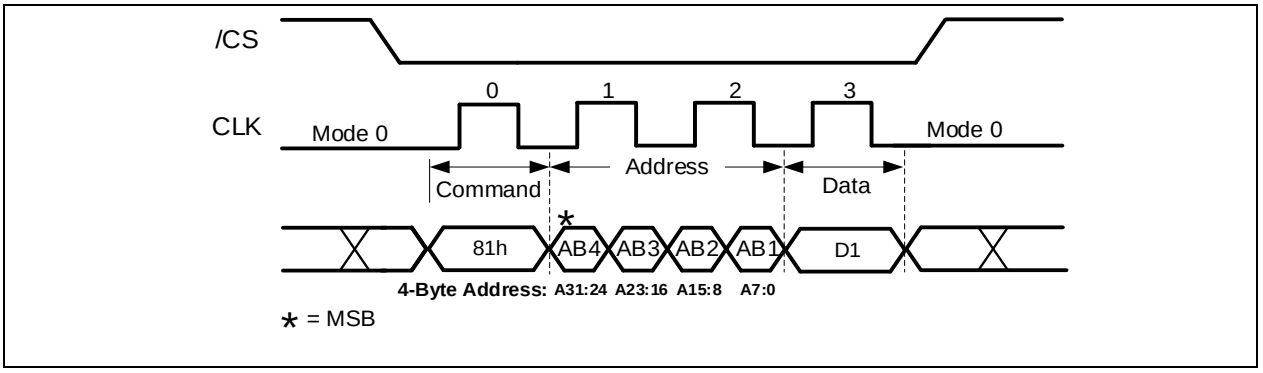


Figure 8-8b. Write Volatile Configuration Command (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR mode

9.4 Pre-Write Setup Commands

The Write Enable Latch (WEL) bit of the Status Register indicates if the device is write enabled or disabled. If the WEL bit is '0', it is write disabled and will not accept program, erase or write to register commands. If the WEL bit is set to '1', it is write enabled and device will acknowledge program, erase, or write to register commands. After program, erase or write to register completion, the WEL bit will automatically reset to '0'. Write Enable and Write Disable commands directly set and clear the WEL bit. Both commands are supported in both SDR and ODDR mode.

9.4.1 Write Enable (06h)

The Write Enable command sets the Write Enable Latch (WEL) bit in the Status Register to '1'. The WEL bit must be set prior to every program memory, erase memory, or write to register commands. In SDR mode, the Write Enable command is entered by driving the /CS pin low, shifting the command code "06h" using the IO0 pin on the rising edge of CLK, and subsequently driving the /CS pin high to execute the command. In ODDR mode, the Write Enable command is entered by driving /CS low, shifting the command code '06h' using the IO[7:0] pins on both the rising and falling edge of CLK, and subsequently driving the /CS pin high to execute the command. Figure 8-9 illustrates the Write Enable command in both SDR (left) and ODDR mode (right).

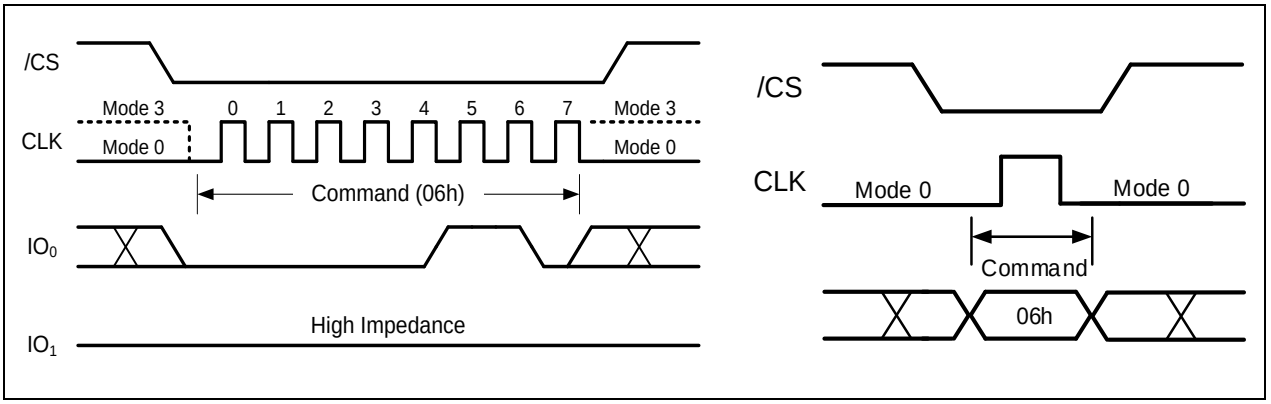


Figure 8-9. Write Enable Command for SDR Mode (left) or ODDR Mode (right)

9.4.2 Write Disable (04h)

The Write Disable command resets the Write Enable Latch (WEL) bit in the Status Register to '0'. In SDR mode, the Write Disable command is entered by driving the /CS pin low, shifting the command code '04h' into the IO0 pin, and subsequently driving the /CS pin high to execute the command. In ODDR mode, the Write Disable command is entered by driving the /CS low, shifting code '04h' into the IO[7:0] pins on both the rising and falling edge of CLK, and subsequently driving the /CS pin high to execute the command. Figure 8-10 illustrates the Write Disable command sequence in both the SDR (left) and ODDR mode (right).

The WEL bit is automatically reset after Power-up, Hardware or Software Reset sequence, and upon completion of internal program, erase, and write to register commands.

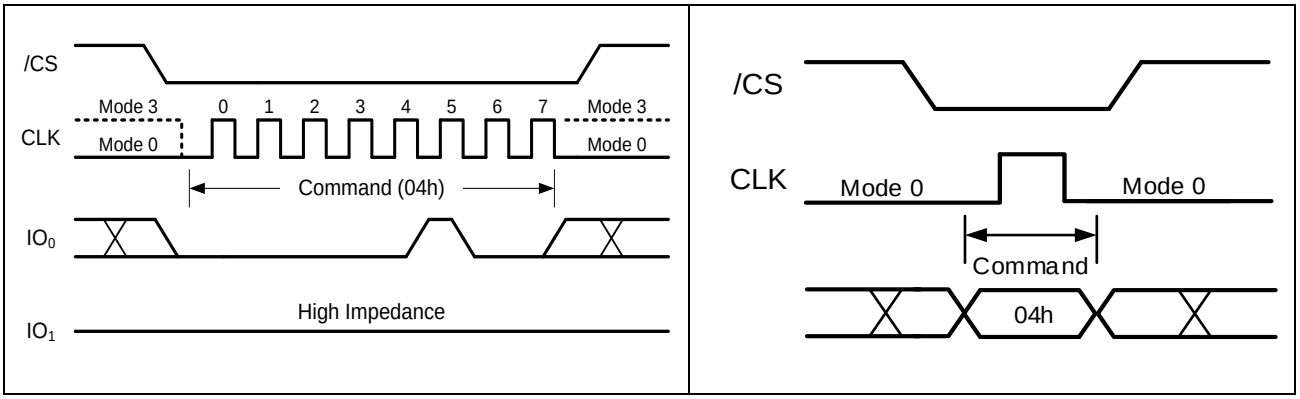


Figure 8-10. Write Disable Command for SDR Mode (left) or ODDR Mode (right)

9.4.3 Write Enable for Volatile Status Register (08h)

The non-volatile Status Register bits described in Section 7.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the non-volatile Status Register bits. To write the volatile values into the Status Register, the Write Enable for Volatile Status Register (08h) command must be issued prior to a Write Status Register (01h) command. The Write Enable for Volatile Status Register command (Figure 8-11) will not set the Write Enable Latch (WEL) bit. Only the Write Status Register command can change the volatile Status Register bit values.

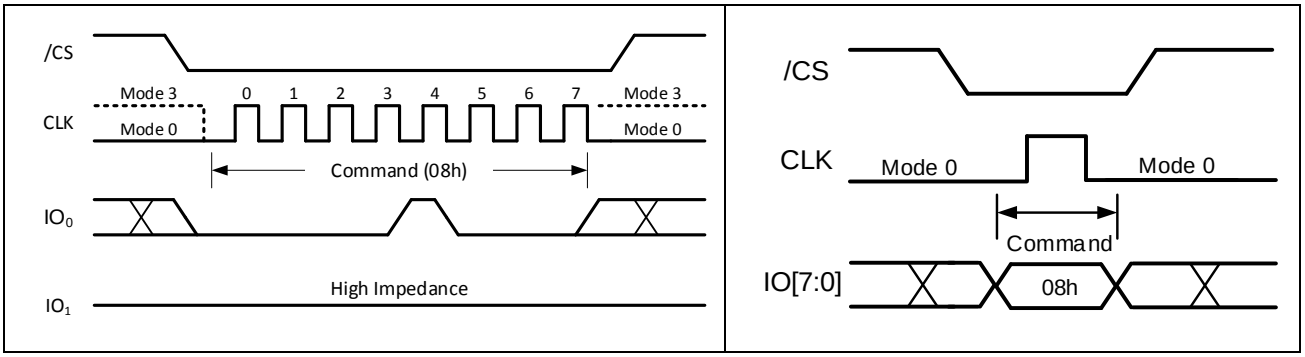


Figure 8-11. Write Enable for Volatile Status Register Command - SDR Mode (left) or ODDR Mode (right)

9.5 Address Mode Commands

Legacy Spiflash devices use 3-Byte Address Mode (24-bit address) only. For backward compatibility, 3-Byte Address Mode is supported to access the memory array up to 128Mb. To access beyond 128Mb, 4-Byte Address Mode has to be enabled. In SDR mode, the default Address mode setting after power up is based on the Non-Volatile Configuration Register Address 05h value that is transferred to the Volatile Configuration Register Address 05h. If the Non-Volatile/Volatile register value is FFh (factory default), 3-Byte Address mode is enabled. To switch between 3-Byte and 4-Byte Address Modes, “Enter 4-Byte Mode (B7h)” or “Exit 4-Byte Mode (E9h)” commands can be used. Both commands are supported in SDR and ODDR mode.

Another method to change the Address mode is by the Configuration Register setting. Changing the values of the Address Mode Configuration in the Volatile Configuration Register will instantly change the address mode. Using the Address Mode Configuration of the Non-Volatile Configuration Register to change the Address Mode requires a power cycle or reset to activate the mode change.

The current address mode is indicated by the Flag Register Address Mode Flag (AMF) Bit 0 (F0). When the AMF bit = ‘0’, the device is in 3-Byte Address Mode, and when the AMF bit = ‘1’, the device is operating in 4-Byte Address Mode.

9.5.1 Enter 4-Byte Address Mode (B7h)

The Enter 4-Byte Address Mode command enables 32-bit address (A31-A0) or the 4-Byte Address Mode. In SDR mode, the Enter 4-Byte Address Mode command is entered by driving the /CS low, shifting the command code “B7h” into the IO0 pin on the rising edge of CLK, and subsequently driving the /CS pin high to execute the command. In ODDR mode, the Enter 4-Byte Address Mode command is entered by driving /CS low, shifting the command code ‘B7h’ into IO[7:0] pins on both the rising and falling edge of CLK, and subsequently driving the /CS pin high to execute the command. Executing this command will set the AMF bit in the Flag Register to ‘1’. Figure 9-1 illustrates the Enter 4-Byte Address Mode command in SDR Mode (left) and ODDR Mode (right).

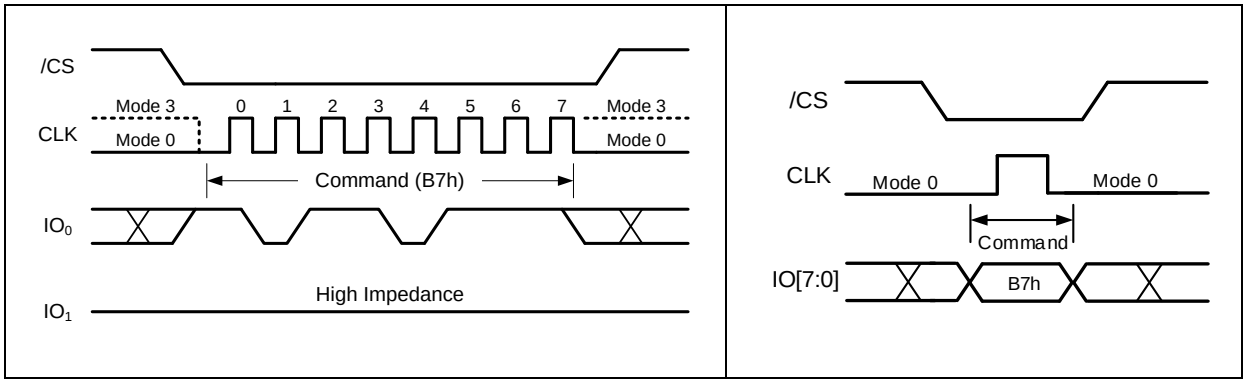


Figure 9-1. Enter 4-Byte Address Mode command for SDR Mode (left) or OODR Mode (right)

9.5.2 Exit 4-Byte Address Mode (E9h)

The Exit 4-Byte Address Mode command switches the Address Mode back to 24-bit address (A23-A0) or the 3-Byte Address Mode. In SDR mode, the Exit 4-Byte Address Mode command is entered by driving /CS low, shifting the command code “E9h” into the IO0 pin on the rising edge of CLK, and subsequently driving the /CS pin high to execute the command. In ODDR mode, the Exit 4-Byte Address Mode command is also entered by driving /CS low, shifting the command code ‘E9h’ into IO[7:0] pins on both the rising and falling edge of CLK, and subsequently driving the /CS pin high to execute the command. Executing this command will clear the AMF bit in the Flag Register to ‘0’. Figure 9-2 illustrates the Exit 4-Byte Address Mode command in SDR Mode (left) and ODDR Mode (right).

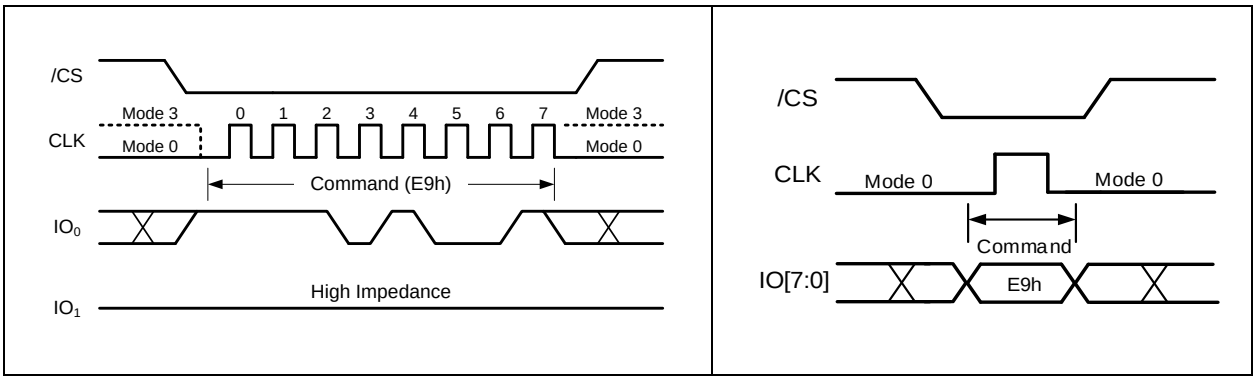


Figure 9-2. Exit 4-Byte Address Mode command for SDR Mode (left) or ODDR Mode (right)

9.6 Read Memory Commands

There is a total of 10 Read Memory commands supported in either SDR or ODDR mode. The Read commands 03h and 13h are supported in SDR mode only. The other Read commands 0Bh, 0Ch, 8Bh, 8Bh, 7Ch, CBh, CCh, 9Dh, and FDh are all supported in both SDR and ODDR mode. The read memory sequences include the command, address, dummy cycles and data output. Command, Address, and Data Output (C-A-D or Cd-Ad-Dd) for memory reads support 1-1-1, 1-1-8, 1-8-8, 1-1d-8d, 1-8d-8d in SDR and 8d-8d-8d in ODDR protocols. Dummy Cycles are required after address input (dummy cycle is not included in the command nomenclature).

9.6.1 Read Data (03h)

The Read Data command is initiated by driving the /CS pin low and then shifting the command code '03h' followed by either a 24-bit or 32-bit address (depending on the Address Mode Configuration) on the IO0 pin on the rising edge of CLK. After the command and address are received, a data byte of the address memory location will be shifted out on the IO1 pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the highest memory address, it will wrap-around back to address 000000h. The command is completed by driving the /CS pin high.

The Read Data command sequence is illustrated in Figure 10-1. If a Read Data command is issued while an Erase, Program or Write cycle is in progress (BUSY=1), the command is ignored and will not have any effect on the current cycle. The Read Data command allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

The Read Data (03h) command is only supported in SDR mode.

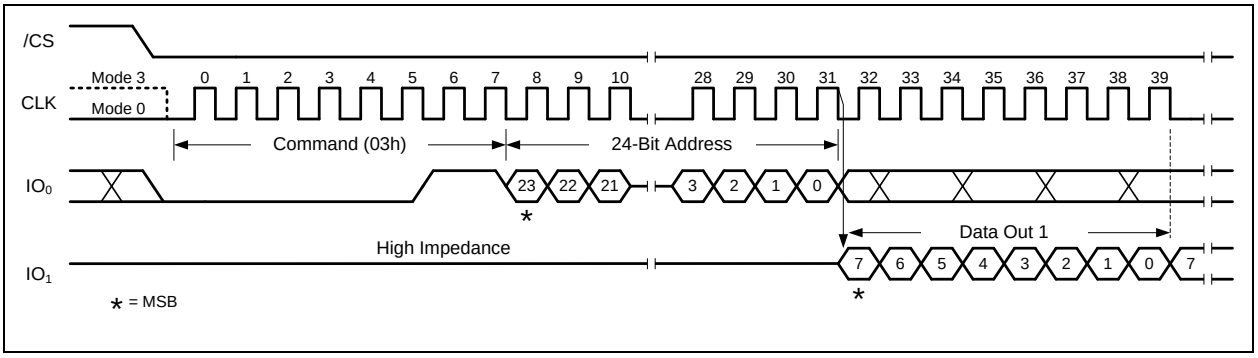


Figure 10-1. Read Data Command (SDR Mode only)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.6.2 Read Data with 4-Byte Address (13h)

The Read Data using a 4-Byte Address command is similar to the Read Data (03h) command except that it requires a 32-bit address instead of a 24-bit. The Address Mode configuration setting does not apply (even in 3-Byte Address Mode) and always requires a 32-bit address to access the entire 512Mb memory.

The Read Data command is initiated by driving the /CS pin low and then shifting the command code '13h' followed by a 32-bit address using the IO0 pin on the rising edge of CLK. After the command and address are received, the data byte of the address memory location will be shifted out on the IO1 pin at the falling edge of CLK with the most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the highest memory address, it will wrap-around back to address 000000h. The command is completed by driving the /CS pin high.

The Read Data using the 4-Byte Address command sequence is illustrated in Figure 10-2. If this command is issued while an Erase, Program or Write cycle is in progress (BUSY=1), the command is ignored and will not have any effect on the current cycle. The Read Data using the 4-Byte Address command allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

The Read Data with 4-Byte Address (13h) command is only supported in SDR mode.

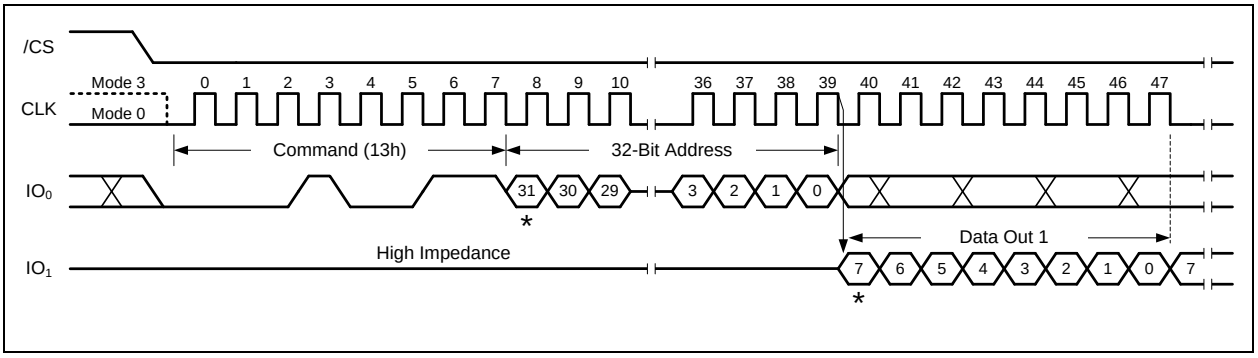


Figure 10-2. Read Data using the 4-Byte Address Command (SDR Mode only)

9.6.3 Fast Read (0Bh)

Fast Read command is similar to the Read Data command except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks (default/programmable) after the 24-bit or 32-bit address which allows the devices internal circuits additional time for setting up the initial address. During the dummy clocks, the data value on the DO pin is “don’t care”.

In SDR mode, the Fast Read command is initiated by driving the /CS pin low and then shifting the command code ‘0Bh’ followed by either a 24-bit or 32-bit address (depending on Address Mode Configuration) on the IO0 pin on the rising edge of CLK, and the required eight “dummy” clocks. After the command, address and dummy cycles are received, the data byte of the addressed memory location will be shifted out on the IO1 pin at the falling edge of CLK with the most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the highest memory address, it will wrap-around back to address 000000h. The command is completed by driving the /CS pin high.

Besides the default 8 dummy cycles, the device also supports programmable dummy clock cycles using the Non-Volatile/Volatile Configuration Register Address 01h (Dummy CLK Cycle Configuration). The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO pins should be high-impedance prior to the falling edge of the first data out clock. Section 7.5.1 Clock Frequency with Required Dummy Clock Cycles table provides details on the maximum clock support based on the dummy CLK Cycle Configuration.

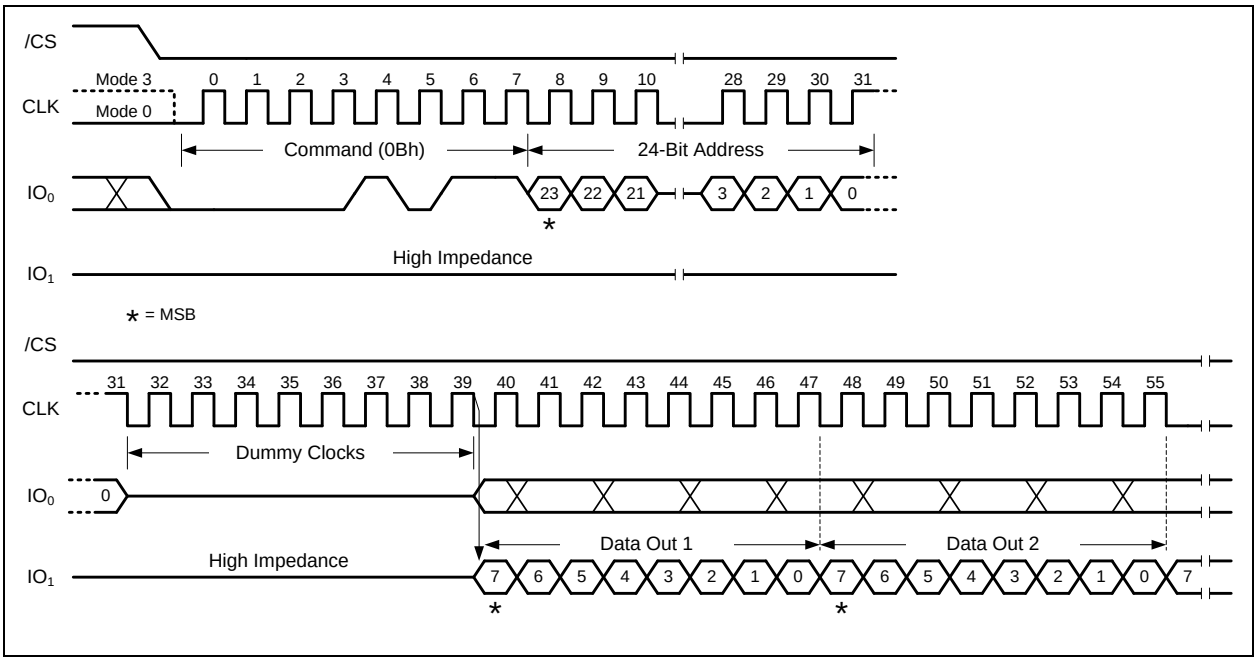


Figure 10-3. Fast Read Command (1-1-1 SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.6.4 Fast Read with 4-Byte Address (0Ch)

The Fast Read using the 4-Byte Address command is similar to the Fast Read (0Bh) command except that it requires a 32-bit address instead of a 24-bit address. The Address Mode configuration setting does not apply (even in 3-Byte Address Mode) and always requires 32-bit address to access the entire 512Mb memory.

In SDR mode, the Fast Read using the 4-Byte Address command is initiated by driving the /CS pin low and then shifting the command code '0Ch' followed by a 32-bit address on IO0 pin on the rising edge of CLK, and the required eight "dummy" clocks (default/programmable). After the command, address and dummy cycles are received, the data byte of the addressed memory location will be shifted out on the IO1 pin at the falling edge of CLK with the most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the highest memory address, it will wrap-around back to address 000000h. The command is completed by driving the /CS pin high.

Besides the default 8 dummy cycles, the device also supports programmable dummy clock cycles using the Non-Volatile/Volatile Configuration Register Address 01h (Dummy CLK Cycle Configuration). The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock. Section 7.5.1 Clock Frequency with Required Dummy Clock Cycles table provides details on the maximum clock support based on the dummy CLK Cycle Configuration.

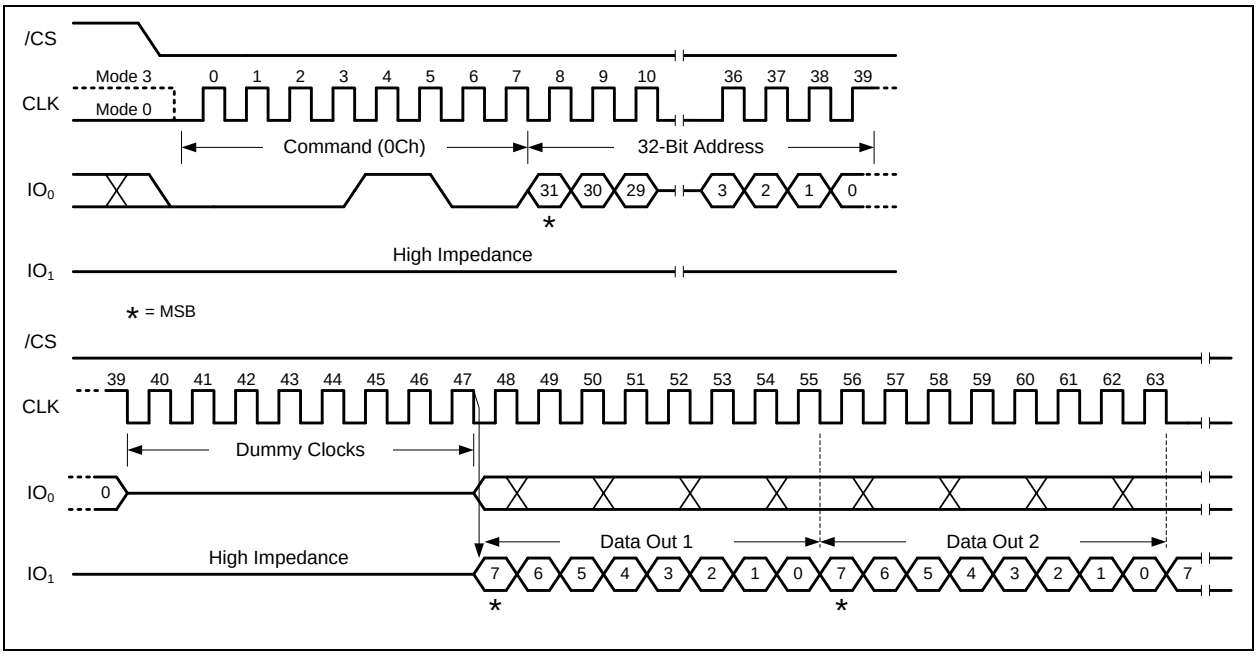


Figure 10-4. Fast Read using the 4-Byte Address Command (1-1-1 SDR Mode)

9.6.5 Fast Read Octal Output (8Bh)

The Fast Read Octal Output (8Bh) command is similar to the Fast Read (0Bh) command except that read data is shifted-out on eight IO[7:0] pins.

In SDR mode, the Fast Read Octal Output command is initiated by driving the /CS pin low and then shifting the command code '8Bh' followed by either a 24-bit or 32-bit address (depending on Address Mode Configuration) on the IO0 pin on the rising edge of CLK, and the required eight "dummy" clocks (default/programmable). After the command, address and dummy cycles are received, the single bit input transitions to an 8-bit output and the data byte of the address memory location will be shifted out on IO[7:0] pins on the falling of CLK. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the highest memory address, it will wrap-around back to address 000000h. The command is completed by driving the /CS pin high.

Besides the default 8 dummy cycles, the device also supports programmable dummy clock cycles using the Non-Volatile/Volatile Configuration Register Address 01h (Dummy CLK Cycle Configuration). The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock. Section 7.5.1 Clock Frequency with Required Dummy Clock Cycles table provides details on the maximum clock support based on the dummy CLK Cycle Configuration.

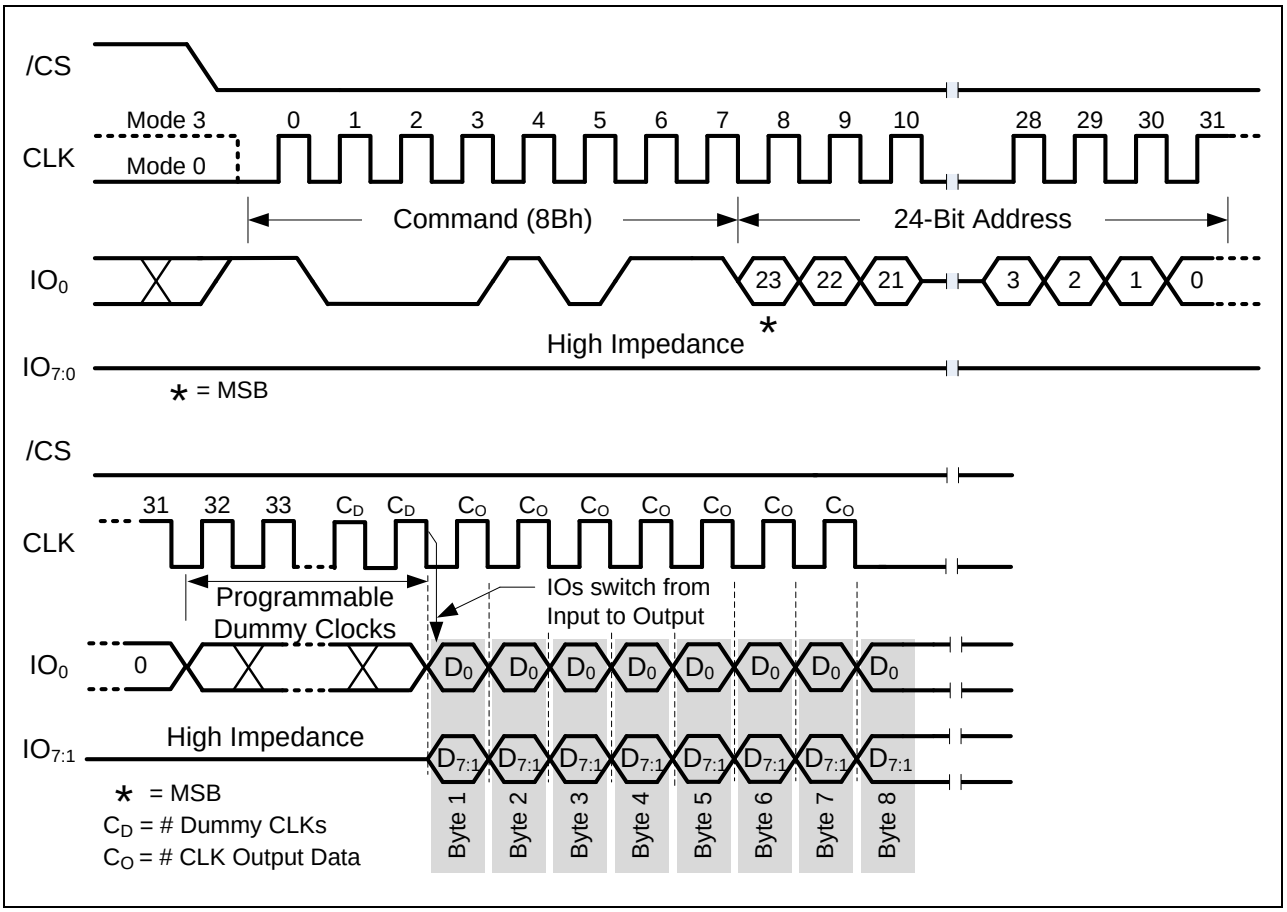


Figure 10-5. Fast Read Octal Output Command (1-1-8 SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.6.6 Fast Read Octal Output with 4-Byte Address (7Ch)

The Fast Read Octal Output using the 4-Byte Address command is similar to the Fast Read Octal Output (8Bh) command except that it requires a 32-bit address instead of a 24-bit address. The Address Mode configuration setting does not apply (even in 3-Byte Address Mode) and always requires a 32-bit address to access the entire 512Mb memory.

In SDR mode, the Fast Read Octal Output using the 4-Byte Address command is initiated by driving the /CS pin low and then shifting the command code '7Ch' followed by a 32-bit address on the IO0 pin on the rising edge of CLK, and the required eight "dummy" clocks (default/programmable). After the command, address and dummy cycles are received, the single bit input transitions to an 8-bit output and the data byte of the address memory location will be shifted out on IO[7:0] pins on the falling of CLK. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the highest memory address, it will wrap-around back to address 000000h. The command is completed by driving /CS pin high.

Besides the default 8 dummy cycles, the device also supports programmable dummy clock cycles using the Non-Volatile/Volatile Configuration Register Address 01h (Dummy CLK Cycle Configuration). The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock. Section 7.5.1 Clock Frequency with Required Dummy Clock Cycles table provides details on the maximum clock support based on the dummy CLK Cycle Configuration.

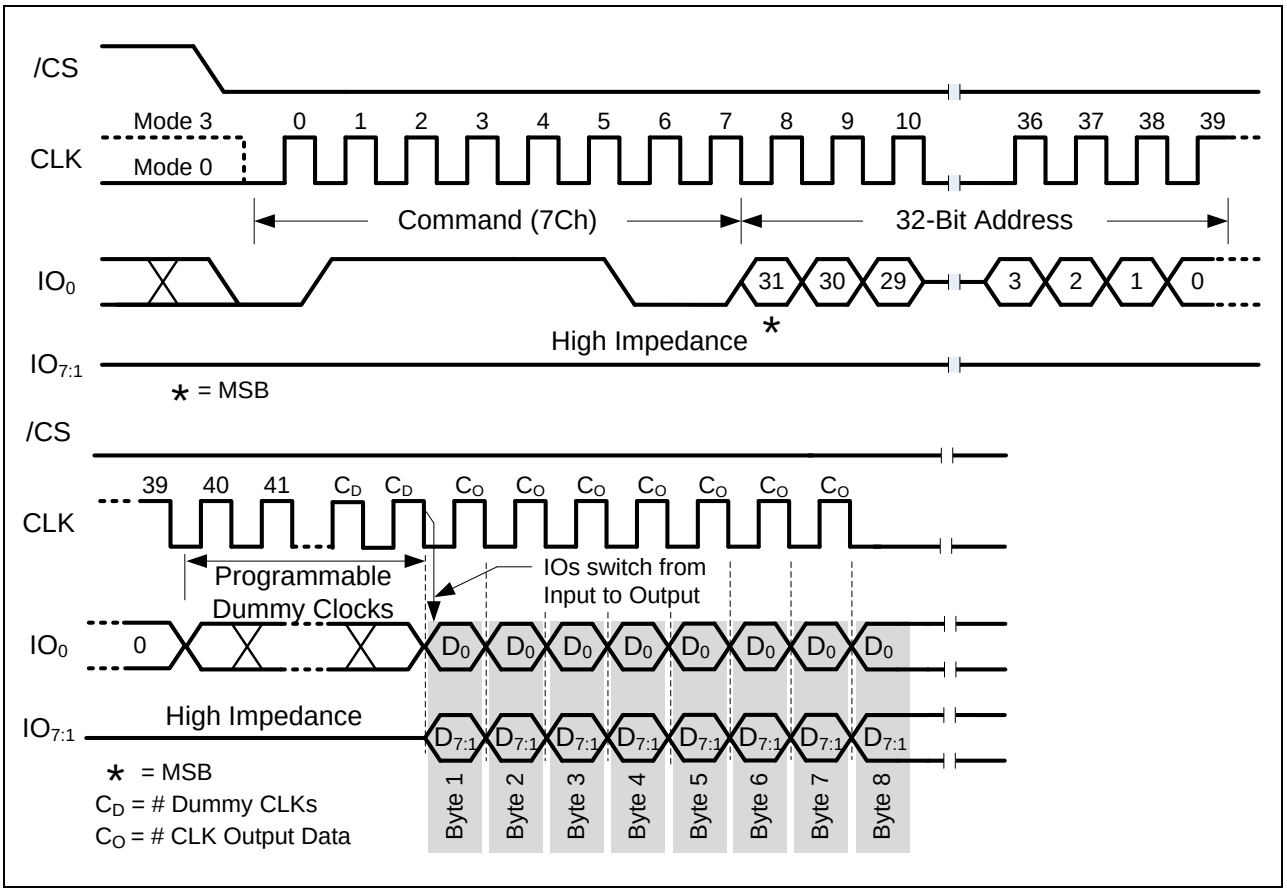


Figure 10-6. Fast Read Octal Output using the 4-Byte Address Command (1-1-8 SDR Mode)

9.6.7 Fast Read Octal I/O (CBh)

The Fast Read Octal I/O (CBh) command is similar to the SDR read command which inputs the command code with a single bit SPI and then transitions to eight IO[7:0] pins during the address input, dummy cycles, and data output.

In SDR mode, the Fast Read Octal I/O command is initiated by driving the /CS pin low and then shifting the command code ‘CBh’ on IO0 pin on the rising edge of CLK, followed by shifting either a 24-bit or 32-bit address (depending on Address Mode Configuration) using eight IO[7:0] pins on the rising edge of the CLK, and the required 16 “dummy” clocks ((default/programmable). After the command, address and dummy cycles are received, the data byte of the address memory location will be shifted out on the IO[7:0] pins on the falling of CLK. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the highest memory address, it will wrap-around back to address 000000h. The command is completed by driving the /CS pin high.

Besides the default 16 dummy cycles, the device also supports programmable dummy clock cycles using the Non-Volatile/Volatile Configuration Register Address 01h (Dummy CLK Cycle Configuration). The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO pins should be high-impedance prior to the falling edge of the first data out clock. Section 7.5.1 Clock Frequency with Required Dummy Clock Cycles table provides details on the maximum clock support based on the dummy CLK Cycle Configuration.

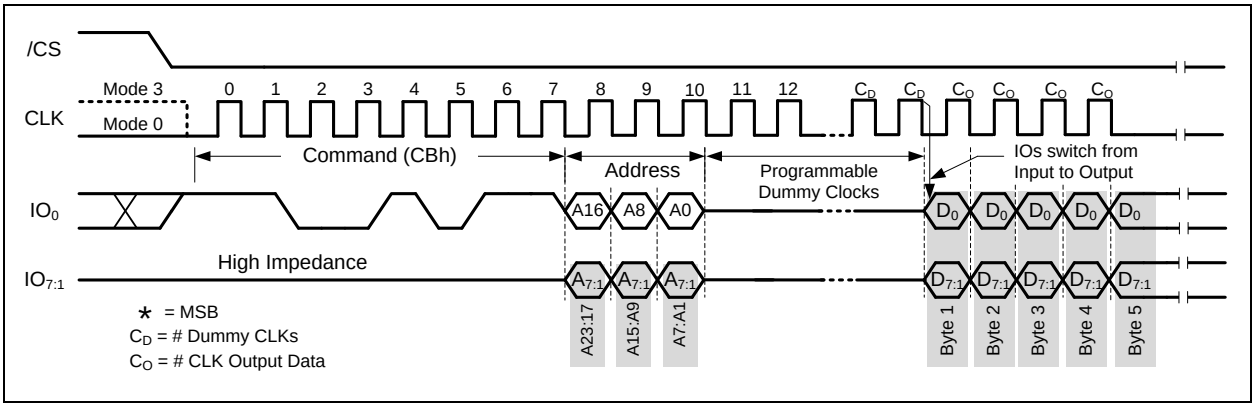


Figure 10-7. Fast Read Octal I/O (1-8-8 SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.6.8 Fast Read Octal I/O with 4-Byte Address (CCh)

The Fast Read Octal I/O using the 4-Byte Address command is similar to the Fast Read Octal I/O (CBh) command except that it requires a 32-bit address instead of a 24-bit address. The Address Mode configuration setting does not apply (even in 3-Byte Address Mode) and will always require a 32-bit address to access the entire 512Mb memory.

In SDR mode, the Fast Read Octal I/O using the 4-Byte Address command is initiated by driving the /CS pin low and then shifting the command code 'CCh' on IO0 pin on the rising edge of CLK, followed by shifting a 32-bit address on eight IO[7:0] pins also on the rising edge of the CLK, and the required 16 "dummy" clocks (default/programmable). Then the data byte of the address memory location will be shifted out on IO[7:0] pins on the falling edge of CLK. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the highest memory address, it will wrap-around back to address 000000h. The command completes by driving the /CS pin high.

Besides the default 16 dummy cycles, the device also supports programmable dummy clock cycles using the Non-Volatile/Volatile Configuration Register Address 01h (Dummy CLK Cycle Configuration). The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock. Section 7.5.1 Clock Frequency with Required Dummy Clock Cycles table provides details on the maximum clock support based on the dummy CLK Cycle Configuration.

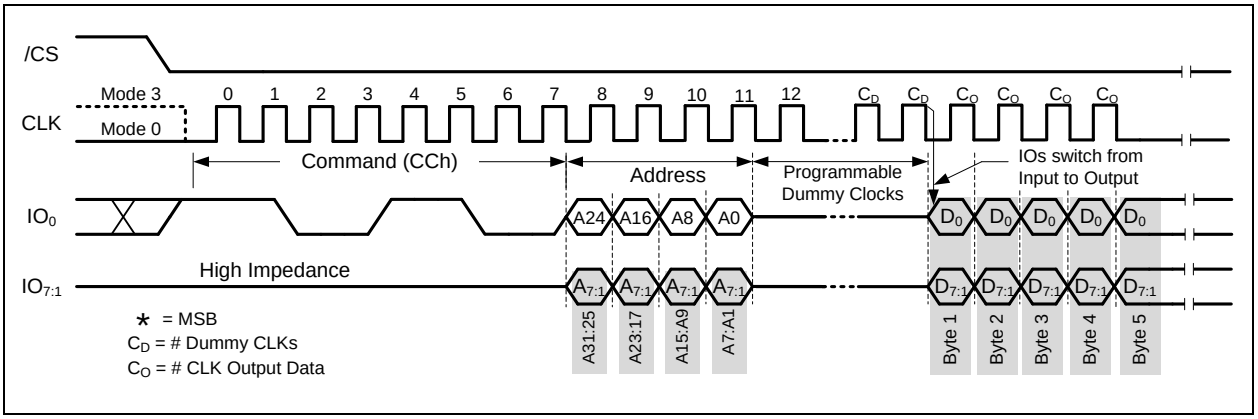


Figure 10-8. Fast Read Octal I/O Command using 4-Byte Address (1-8-8 SDR)

9.6.9 Fast Read DDR Single-Address-Input and Octal-Output (9Dh)

The Fast Read DDR Single-Address-Input and Octal-Output commands start similar to the SDR read command with single bit SPI and latching in the byte command on the rising edge of CLK. The CLK mode transitions to using the rising and falling edge of CLK during the address input and data output phase. From the data input to the data output phase, the IO mode transitions from single bit input to octal output.

In SDR mode, the Fast Read DDR Single-Address-Input and Octal-Output command is initiated by driving the /CS pin low and then shifting the command code '9Dh' on IO0 pin on the rising edge of CLK, followed by shifting in of either a 24-bit or a 32-bit address (depending on Address Mode Configuration) on the IO0 pin on both the rising and falling edge of CLK, and the required eight "dummy" clocks (default/programmable). Then the single bit input transitions to 8-bit output, and the data byte of the target address memory location will be shifted out on the IO[7:0] pins on the falling and rising edge of CLK. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the highest memory address, it will wrap-around back to address 000000h. The command is completed by driving the /CS pin high.

Note that A[0] must be 0 in Fast Read DDR 9Dh commands. If A0≠0, wrong data will be read from 9Dh commands. Besides the default 16 dummy cycles, the device also supports programmable dummy clock cycles using Non-Volatile/Volatile Configuration Register Address 01h (Dummy CLK Cycle

Configuration). The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO pins should be high-impedance prior to the falling edge of the first data out clock. Section 7.5.1 Clock Frequency with Required Dummy Clock Cycles table provides details on the maximum clock support based on the dummy CLK Cycle Configuration.

If the Data Strobe (DS) pin is enabled by the NVCR/VCR-IOC, the DS pin is a synchronization signal supporting high speed data output. Regardless of Mode0 or Mode3, when the /CS pin is driven low and after the first falling edge of clock, the device drives the DS pin low from a high impedance state. The device IO pins then transition from input sequence to output sequence; and at this point the DS pin toggles simultaneously as the data output is shifted out on each CLK edge. When /CS pin is driven high, the DS pin goes to high impedance. The DS pin is in high impedance when the DS pin functionality is disabled.

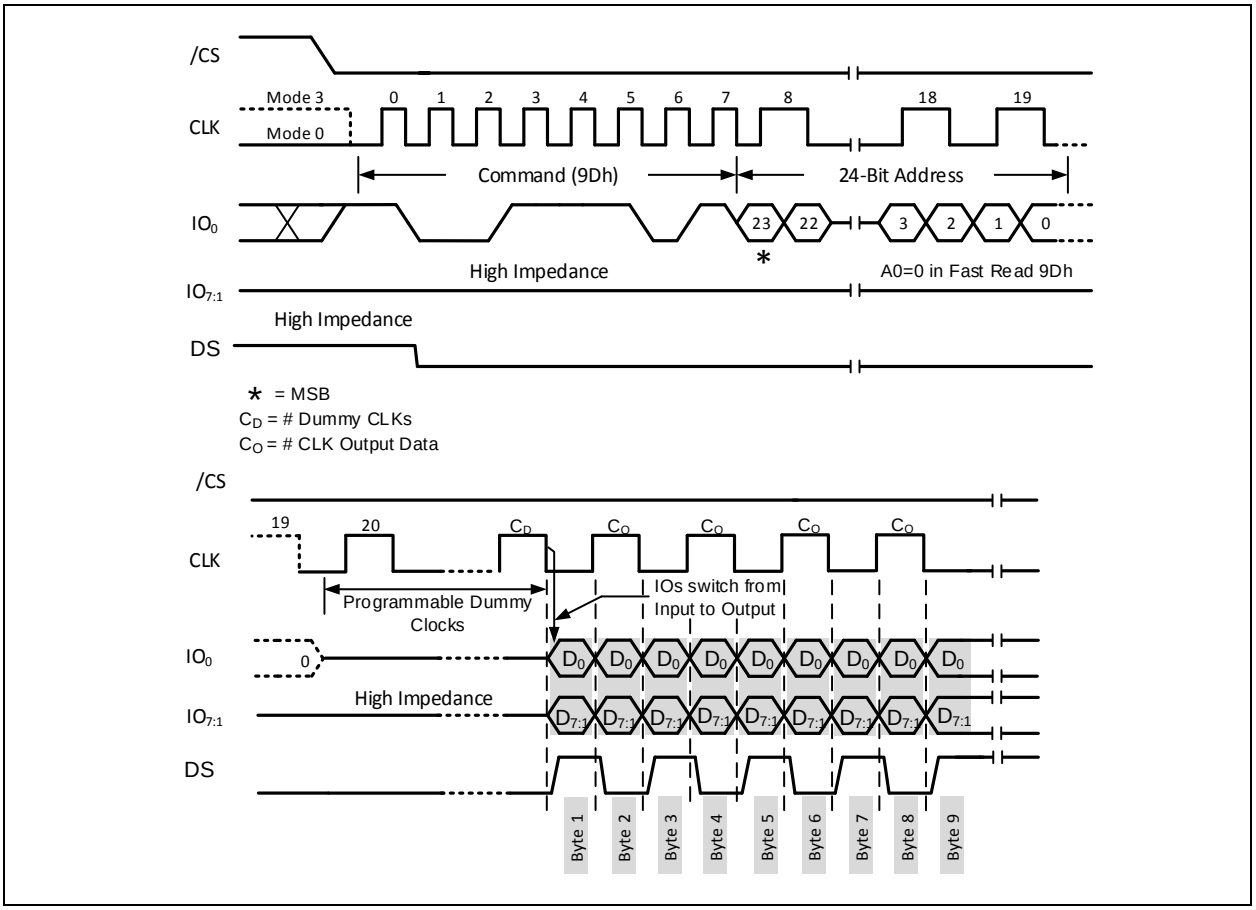


Figure 10-9. Fast Read DDR Single-Address-Input and Octal-Output (1-1d-8d SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.6.10 Fast Read DDR Octal I/O (FDh)

The Fast Read DDR Octal I/O (FDh) command starts similar to the SDR read command code input with single bit SPI and latching in the byte command on the rising edge of CLK. The CLK mode transitions to using both the rising and falling edge of CLK while the IO Mode Configuration transitions to Octal IO during the address input and data output phase.

In SDR mode (command code only), the Fast Read DDR Octal I/O command is initiated by driving the /CS pin low and then shifting the command code 'FDh' using the IO0 pin on the rising edge of CLK, followed by shifting in of a 32-bit address on IO[7:0] pins on both the rising and falling edge of CLK, and the required 16 "dummy" clocks (default/programmable). Then the data byte of the target address memory location will be shifted out on IO[7:0] pins on both the falling and rising edge of CLK. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the highest memory address, it will wrap-around back to address 000000h. The command is completed by driving the /CS pin high.

Note that A[0] must be 0 in Fast Read DDR FDh commands. If A0≠0, wrong data will be read from the FDh command. Besides the default 16 dummy cycles, the device also supports programmable dummy clock cycles using the Non-Volatile/Volatile Configuration Register Address 01h (Dummy CLK Cycle Configuration). The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock. Section 7.5.1 Clock Frequency with Required Dummy Clock Cycles table provides details on the maximum clock support based on the dummy CLK Cycle Configuration.

If the Data Strobe (DS) pin is enabled by the NVCR/VCR-IOC, the DS pin is a synchronization signal supporting high speed data output. Regardless of Mode0 or Mode3, when the /CS pin is driven low and after the first falling edge of clock, the device drives the DS pin low from a high impedance state. The device IO pins then transition from input sequence to output sequence; and at this point the DS pin toggles simultaneously as the data output is shifted out on each CLK edge. When the /CS pin is driven high, the DS pin goes to high impedance. The DS pin is in high impedance when the DS pin functionality is disabled.

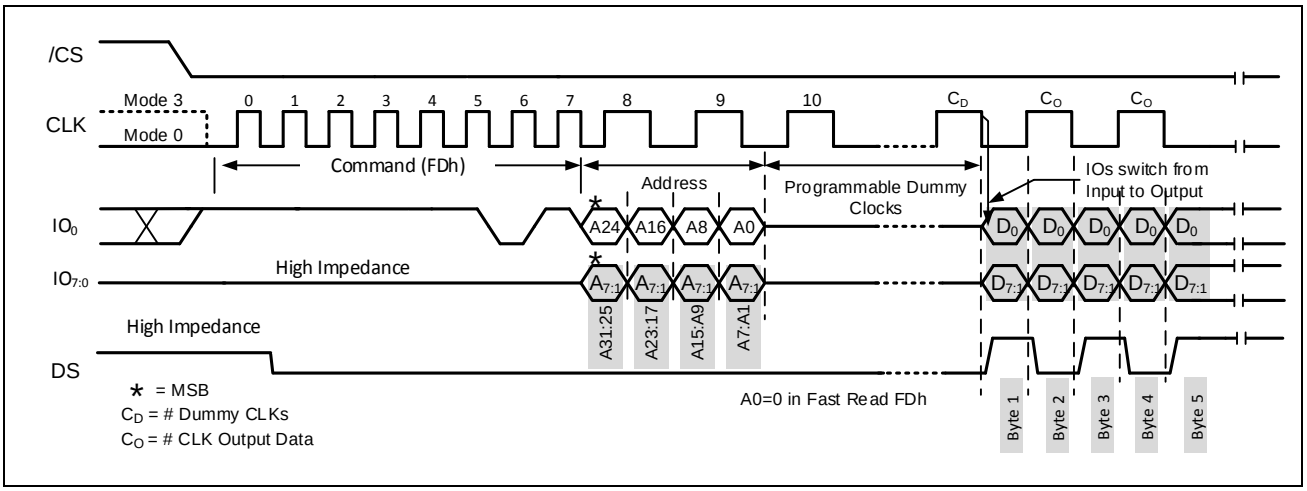


Figure 10-10. Fast Read DDR Octal I/O with 4-Byte Address (1-8d-8d SDR Mode)

9.6.11 ODDR Fast Read Commands

In ODDR mode, the command input, address input, and data output of all the ODDR Fast Read commands (0Bh, 0Ch, 8Bh, 7Ch CBh, CCh, 9Dh, and FDh) are latched-in using the IO[7:0] pins on both the rising and falling edges of the clock.

The ODDR Fast Read command is initiated by driving the /CS pin low and shifting the command code '0Bh, 0Ch, 8Bh, 7Ch, CBh, CCh, 9Dh, or FDh' using the IO[7:0] pins on both the rising and falling edge of CLK. A 32-bit address is shifted using the IO[7:0] pins on both the rising and falling edge of CLK after the command. **A[0] must be 0 in ODDR Fast Read commands. If A0≠0, wrong data will be read from ODDR commands.** The address is followed by 16 dummy CLK cycles (default/programmable), and IO[7:0] will transition from input to output on the falling edge of the last dummy clock cycle. Each data byte (output data) is shifted out using the IO[7:0] pins on both the falling and rising edge of CLK starting from the target address. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the highest memory address, it will wrap-around back to address 000000h. The command is completed by driving the /CS pin high. Figure 10-11 illustrates the ODDR Fast Read command.

Besides the default 16 dummy cycles, the device also supports programmable dummy clock cycles using the Non-Volatile/Volatile Configuration Register Address 01h (Dummy CLK Cycle Configuration). The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock. Section 7.5.1 Clock Frequency with the Required Dummy Clock Cycles table provides details on the maximum clock support based on the dummy CLK Cycle Configuration.

If the Data Strobe (DS) pin is enabled by the NVCR/VCR-IOC, the DS pin is a synchronization signal supporting high speed data output. When the /CS pin is driven low and after the falling edge of the first clock input, the device drives the DS pin low from a high impedance state. The device IO pins then transition from an input sequence to an output sequence; and at this point the DS pin toggles simultaneously as the data output is shifted out on each CLK edge. When the /CS pin is driven high, the DS pin goes to high impedance. The DS pin is in high impedance when the DS pin functionality is disabled.

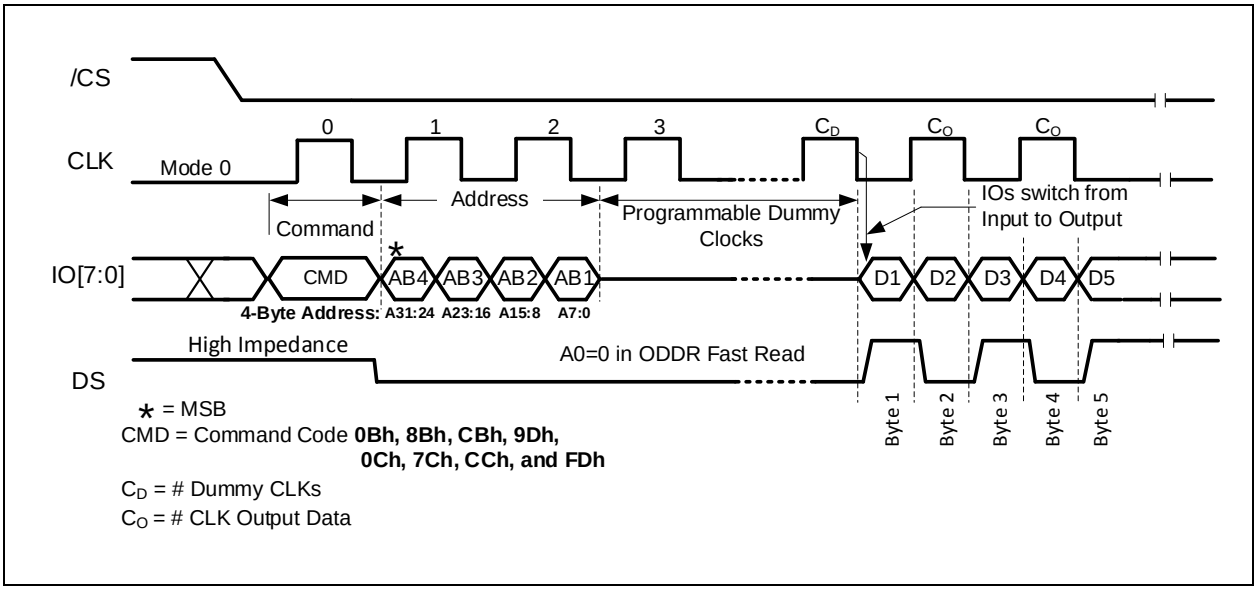


Figure 10-11. ODDR Fast Read Command (8d-8d-8d ODDR)

A 32-Bit Address is required when the device is operating in ODDR Mode

9.7 Program Memory Commands

Page Program commands program from one byte to 256 bytes (a page) of data on previously erased (FFh) target memory locations. A Write Enable command must be executed before the device accepts any Page Program Commands (Status Register bit WEL= 1).

If an entire 256-byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In cases where less than 256 bytes (a partial page) is programmed, the other bytes within the same page will not be affected. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously programmed data.

In SDR mode, as with the write and erase commands, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the Page Program command will not be executed, the WEL bit will remain '1', and no error flag bits will be set.

When the Page Program is initiated (after /CS pin is driven high), the self-timed Page Program command will commence for a time duration of t_{PP} (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register command may still access the Status Register's BUSY bit. The BUSY bit is "1" during internal programming cycle. After program completion, both the BUSY bit and the Write Enable Latch (WEL bit) of the Status Register are cleared to "0", and the device will be ready to accept new commands. The Page Program command will not be executed if the addressed page is protected by the Block Protect bits (CMP, TB, BP3, BP2, BP1, and BP0).

The ECC Enable (ECC) bit of the ECC Status Register can be enabled or disabled at any point during the device operation. Regardless of the ECC bit setting, the number of programming attempts and the ECC On/Off status monitor of every aligned 16-Byte memory are tracked and monitored internally. Every programming attempt will program the data input to the memory array. ECC calculation is also performed during the internal programming operation, and the results are stored in the redundancy or spare area of the memory array. Error correction codes are calculated and stored based on 16-byte aligned address boundaries across the memory (from A[3:0] = 0000b to 1111b).

Every aligned 16-byte memory should only be programmed once with one up to 16 bytes of data, so ECC functionality (ECC On status) will be maintained during memory reads. When the ECC Enable (ECC) bit is 1 (ECC enabled), read memory on aligned 16-byte memory with ECC On status will first check the ECC data stored in the spare area and apply the necessary error detection or correction on the memory array address range before read data output is shifted out.

If any of the aligned 16-byte memory is programmed more than once, the ECC functionality of those affected 16-byte aligned memories will automatically be turned off (ECC Off status). When the Enable (ECC) bit is 1 (ECC enabled), read memory on aligned 16-byte memory with ECC Off status (ECCO or ECCOF bits are off) will access the memory location without any internal ECC check for error detection or correction. An erase operation on 16-byte aligned memory with ECC Off status will turn on the ECC functionality (ECC On status) of those affected aligned 16-byte memory addresses.

When the ECC Enable (ECC) bit is 0 (ECC disabled), read memory will only access the target memory array location without any internal ECC check for error detection or correction.

The page program commands supported in SDR mode are Page Program, Page Program with 4-Byte Address, Page Program Octal Data, Page Program Octal Data with 4-Byte Address, Page Program Octal Address/Data, and Page Program Octal Address/Data with 4-Byte Address. The Octal DDR Page Program uses all the Page Program command codes using the ODDR command sequence. The Page Program command sequences are detailed in the following sections.

9.7.1 Page Program (02h)

In SDR mode and once the device is write enabled (WEL bit = 1), the Page Program ‘02h’ command is entered by the following sequence: drive the /CS pin low; shift-in the command code ‘02h’, a 24-bit or a 32-bit address (depending on Address Mode Configuration), and 1 to 256 bytes of data (to be programmed) using the IO0 pin on the rising edge of CLK; and drive the /CS pin high to initiate the internal program cycle. Figure 11-1 illustrates the Page Program ‘02h’ command in SDR mode.

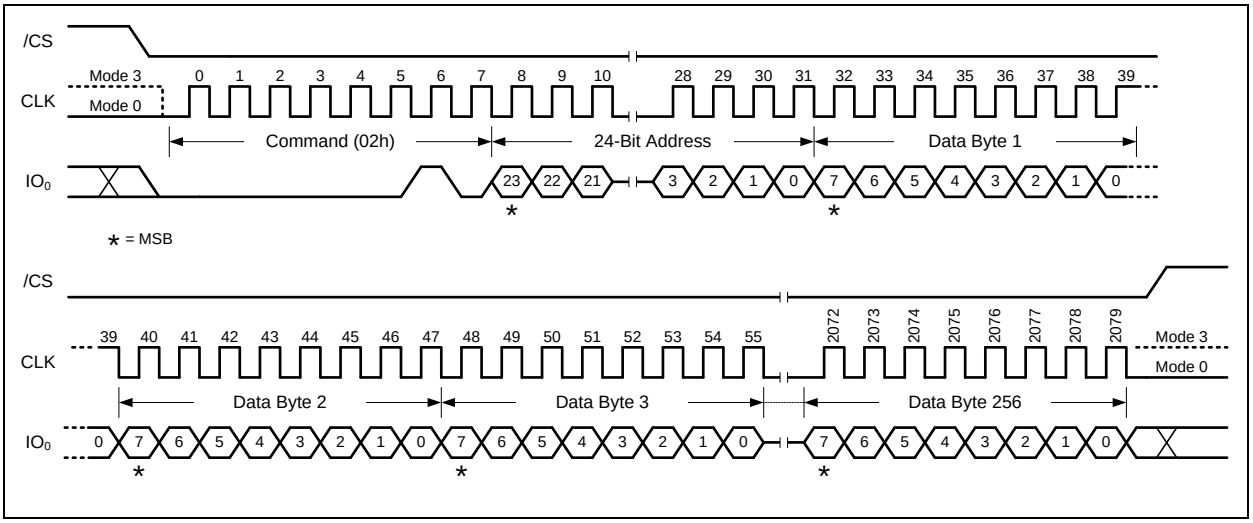


Figure 11-1. Page Program Command (SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.7.2 Page Program with 4-Byte Address (12h)

In SDR mode, the Page Program with 4-Byte Address command is similar to the Page Program command except that it requires a 32-bit address instead of a 24-bit address to access the entire 512Mb memory. The Address Mode configuration setting is not applicable (even in 3-Byte Address Mode).

Once the device is write enabled (WEL bit = 1), Page Program '12h' with 4-Byte Address command is entered by the following sequence: drive the /CS pin low; shift-in the command code '02h' – 32-bit Address – 1 to 256 bytes data (to be programmed) using the IO0 pin on the rising edge of CLK; and drive the /CS pin high to initiate the internal program cycle. Figure 11-2 illustrates the Page Program '12h' with 4-Byte Address command in SDR mode.

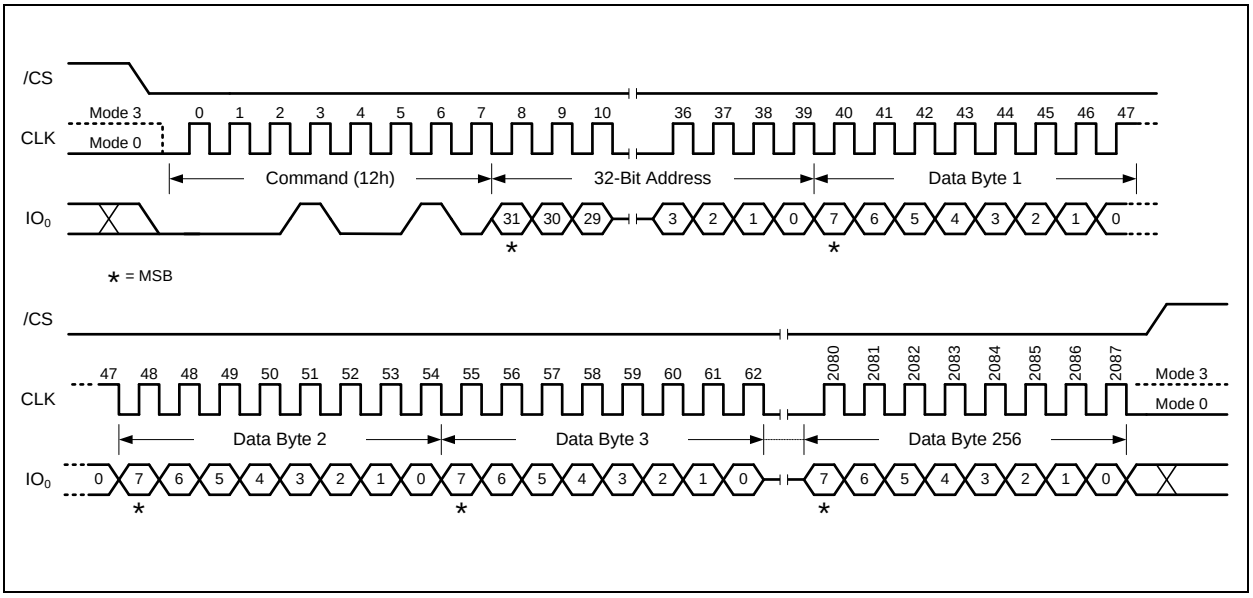


Figure 11-2. Page Program with 4-Byte Addr. (SDR Mode Only)

9.7.3 Page Program Octal Data (82h)

The Page Program Octal Data command allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using the IO0 pin during the command/address input sequence and transitioning to IO[7:0] pins during the data input step in SDR mode.

Once the device is write enabled (WEL bit =1), the command is initiated by the following sequence: drive the /CS pin low; shift-in the command code “82h” followed by a 24-bit or a 32-bit address (depending on Address Mode Configuration) using the IO0 pin on the rising edge of CLK; transition to IO[7:0] and shift-in 1 to 256 bytes of data on the rising edge of CLK; and subsequently drive the /CS pin high to initiate the internal program cycle. The Page Program Octal Data command sequence is illustrated in Figure 11-3.

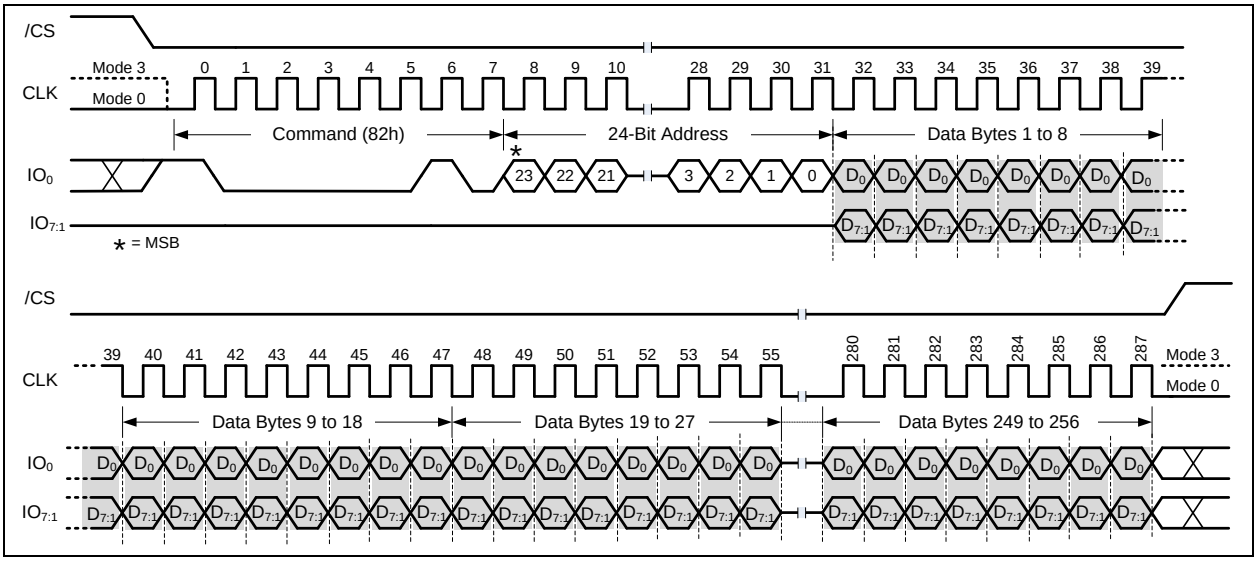


Figure 11-3. Page Program Octal Data Command (SDR Mode only)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.7.4 Page Program Octal Data with 4-Byte Address (84h)

In SDR mode, the Page Program Octal Data using the 4-Byte Address command is similar to the Page Program Octal Data command except that it requires a 32-bit address instead of a 24-bit address to access the entire 512Mb memory. The Address Mode configuration setting is not applicable (even in 3-Byte Address Mode).

Once the device is write enabled (WEL bit =1), the command is initiated by the following sequence: drive the /CS pin low; shift-in the command code “84h” followed by a 32-bit address using the IO0 pin on the rising edge of CLK; transition to IO[7:0] and shift-in 1 to 256 bytes of data on the rising edge of CLK; and subsequently drive the /CS pin high to initiate the internal program cycle. The Page Program Octal Data with 4-Byte Address command sequence is illustrated in Figure 11-4.

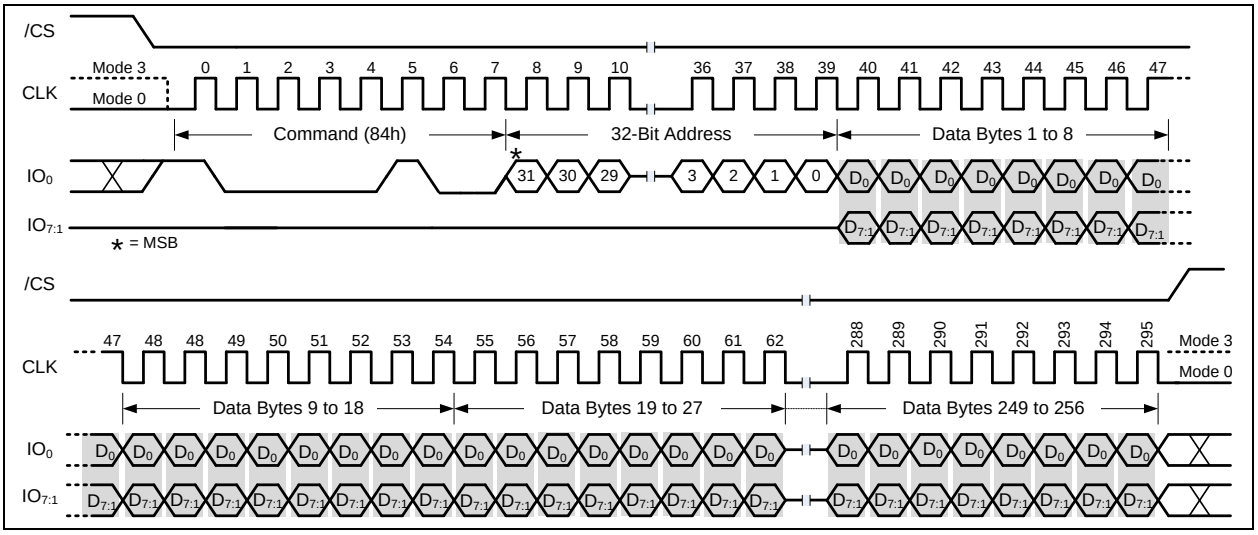


Figure 11-4. Page Program Octal Data using 4-Byte Addr. (SDR Mode)

9.7.5 Page Program Octal Address/Data (C2h)

The Page Program Octal Address/Data command allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using the IO0 pin during the command code input sequence and transitioning to the IO[7:0] pins during the address and data input phase in SDR mode.

Once the device is write enabled (WEL bit =1), the command is initiated by the following sequence: drive the /CS pin low; shift-in the command code “C2h” using the IO0 pin on the rising edge of CLK; transition to IO[7:0] when shifting in address/data input on rising edge of CLK, where address input is either a 24-bit or a 32-bit address (depending on Address Mode Configuration) and data input is 1 to 256 bytes of data; and subsequently drive the /CS pin high to initiate the internal program cycle. The Page Program Octal Address/Data command sequence is illustrated in Figure 11-5.

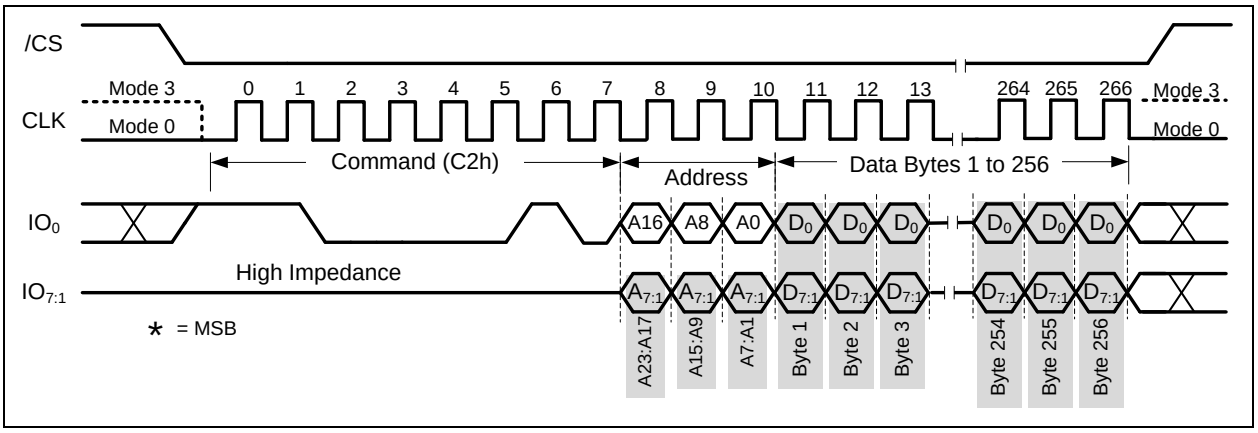


Figure 11-5. Page Program Octal Address/Data Command (SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.7.6 Page Program Octal Address/Data with 4-Byte Address (8Eh)

In SDR mode, the Page Program Octal Address/Data with 4-Byte Address command is similar to the Page Program Octal Address/Data command except that it requires a 32-bit address instead of a 24-bit address to access the entire 512Mb memory. The Address Mode configuration setting is not applicable (even in 3-Byte Address Mode.

Once the device is write enabled (WEL bit =1), the command is initiated by the following sequence: drive the /CS pin low; shift-in the command code “8Eh” using the IO0 pin on the rising edge of CLK; transition to IO[7:0] when shifting in address/data input on the rising edge of CLK, where address input is a 32-bit address and data input is 1 to 256 bytes of data; and subsequently drive the /CS pin high to initiate the internal program cycle. The Page Program Octal Address/Data command sequence is illustrated in Figure 11-6.

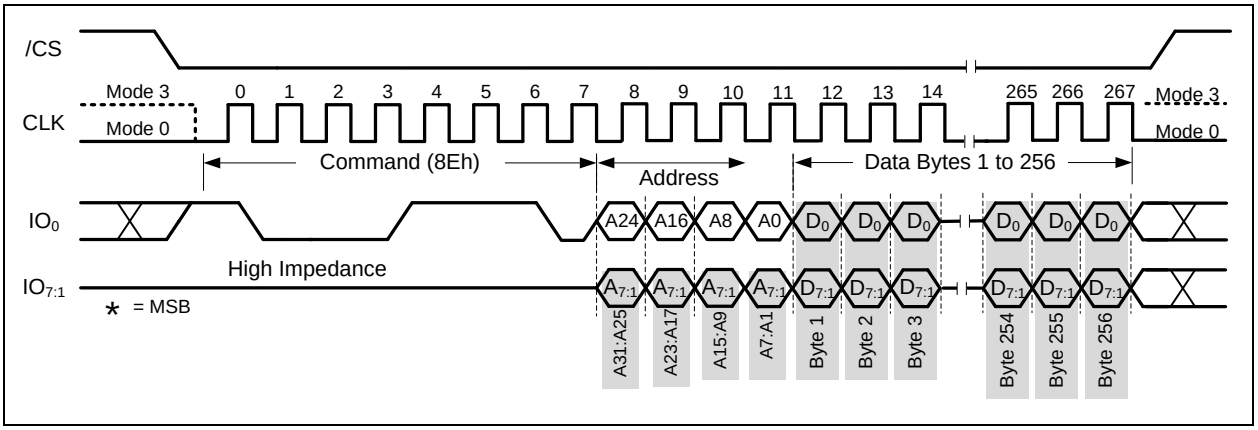


Figure 11-6. Page Program Octal Address/Data using 4-Byte Addr. (SDR Mode)

9.7.7 ODDR Page Program

The Octal DDR Page Program supports all the Page Program command codes 02h/12h 82h/84h, and C2h/12h in Octal DDR protocol. In the Octal DDR Page Program sequence, the command code is shifted-in using the IO[7:0] pins on both the rising and falling edge of CLK. The Address Mode Configuration used in ODDR mode is a 32-bit Address (4-Byte Address Mode) input. The Address and Data also use IO[7:0] pins on both the rising and falling edge of CLK to latch in data.

Once the device is write enabled (WEL bit =1), the Octal DDR Page Program command is initiated by the following sequence: drive the /CS pin low; shift-in the command code “02h/12h 82h/84h, or C2h/12h” on IO7:0 pins on both rising and falling edge of CLK; continue to shift-in 32-bit address and 1 to 256 bytes data input on IO[7:0] pins on both rising edge of CLK; and subsequently drive /CS pin high to initiate the internal program cycle. The Octal DDR Page Program command sequence is illustrated in Figure 11-7.

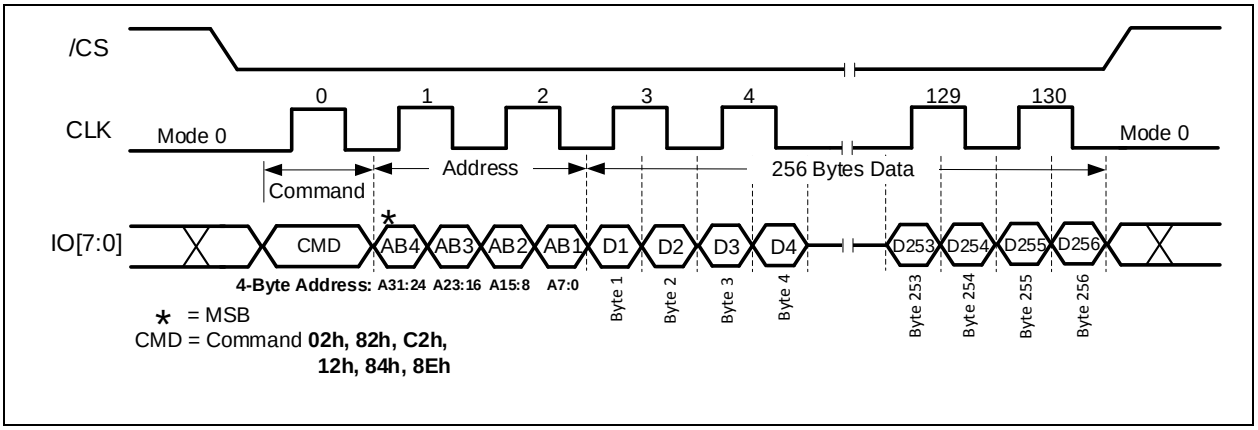


Figure 11-7. Octal DDR Page Program Commands (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR mode

9.8 Erase Memory Commands

The memory array of the W35T51NW is partitioned in 4-KBytes sectors, 32-KBytes Sub-Blocks, and 64-Kbytes Blocks. Each of the partitions can be erased individually. The erase commands set the target memory address range (sector, sub-block, block, full chip) to the erased state of FFh (all 1s). A Write Enable command must be executed before the device accepts any erase command (Status Register bit WEL= 1).

In SDR mode, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the erase command will not be executed, and the WEL bit will remain set with no error flag bits set.

When the erase cycle is initiated after the /CS pin is driven high, the self-timed erase cycle will commence for a time duration of tSE, tBE1, tBE2 or tCE (See AC Characteristics). While the erase cycle is in progress, the Read Status Register command can still access the Status Register's BUSY bit. The BUSY bit is '1' during the internal erase cycle and becomes '0' when the erase completes. After erase completion, the Write Enable Latch (WEL) bit of the Status Register is cleared to '0', and the device is ready to accept new commands. The erase commands will not be executed if the target address being erase is protected by the Block Protect bits (CMP, TB, BP3, BP2, BP1, and BP0).

If any of the aligned 16-byte memory is programmed more than once, the ECC functionality of those affected 16-byte aligned memories will automatically be turned off (ECC Off status). When the ECC Enable (ECC) bit is 1 (ECC enabled), read memory on aligned 16-byte memory with ECC Off status (ECCO or ECCOF bits are off) will directly access the memory location without any internal ECC check for error detection and correction. An erase operation on 16-byte aligned memory with ECC Off status will turn on the ECC functionality (ECC On status) of those affected aligned 16-byte memory addresses.

Sector Erase, Sector Erase with 4-Byte Address, 32KB Block Erase, 32KB Block Erase with 4-Byte Address, 64KB Block Erase, 64KB Block Erase with 4-Byte Address, and Chip Erase commands are all supported in SDR and ODDR mode. Details of each erase command sequence are described in the following sections.

9.8.1 Sector Erase (20h)

The Sector Erase command sets all bits within a specified sector (4K-bytes) to the erased state of FFh (all 1s). In SDR mode and when the device is write enabled (WEL=1), the operation is entered by driving the /CS pin low. This is followed by shifting in the command code "20h" and a 24-bit or 32-bit sector address (depending on the Address Mode Configuration) using the IO0 pin on the rising edge of CLK. Subsequently, the /CS pin is driven high to initiate the internal sector erase cycle. The Sector Erase command sequence is illustrated in Figure 12-1.

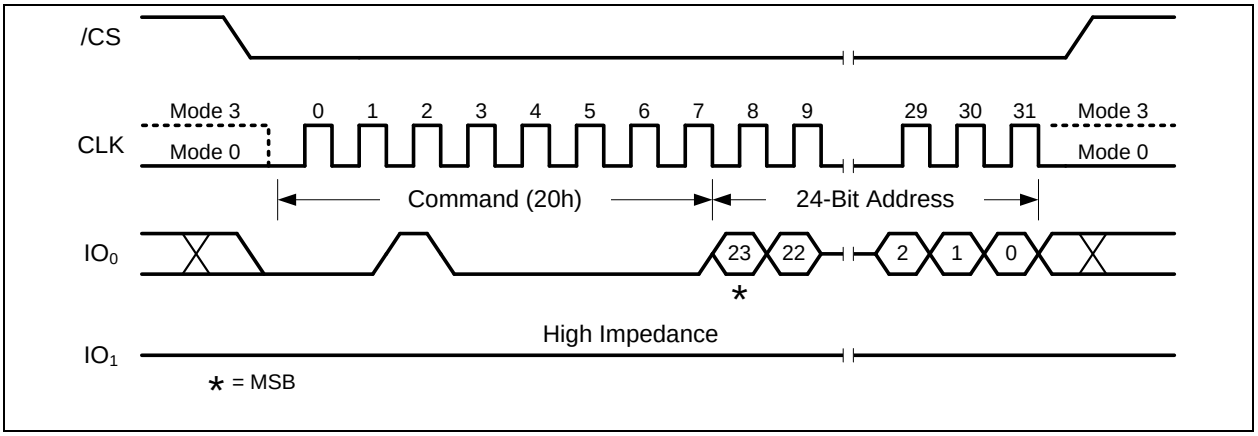


Figure 12-1. Sector Erase Command (SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.8.2 Sector Erase with 4-Byte Address (21h)

In SDR mode, the Sector Erase with 4-Byte Address command is similar to the Sector Erase command except that it requires a 32-bit address instead of a 24-bit address to access the entire 512Mb memory. The Address Mode Configuration setting is not applicable (even in 3-Byte Address Mode).

Once the device is write enabled (WEL=1), the command is entered by driving the /CS pin low. This is followed by shifting in the command code “20h” and a 32-bit sector address using the IO0 pin on the rising edge of CLK. Subsequently, the /CS pin is driven high to initiate the internal sector erase cycle. The Sector Erase with 4-Byte Address command sequence is illustrated in Figure 12-2.

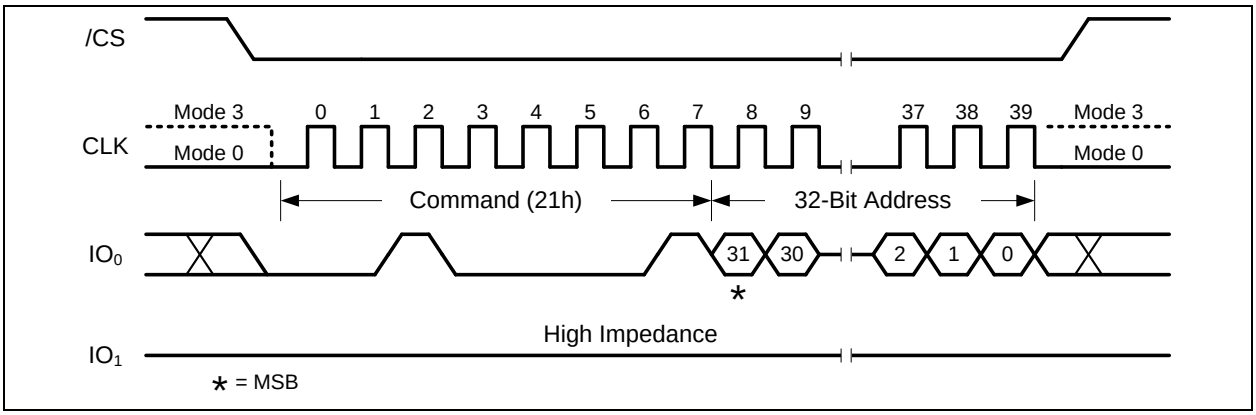


Figure 12-2. Sector Erase with 4-Byte Address Command (SDR Mode)

9.8.3 ODDR Sector Erase (20 or 21h)

In ODDR mode, Sector Erase command codes 20h and 21h are supported. In the Octal DDR Sector Erase sequence, the command code is shifted-in on IO[7:0] pins on both the rising and falling edge of CLK. Address Mode Configuration in ODDR mode only uses 32-bit Address (4-Byte Address Mode) input. Address and Data also use IO[7:0] pins on both rising and falling edge of CLK to latch in data.

Once the device is write enabled (WEL bit =1), the ODDR Sector Erase command is initiated by the following sequence: drive the /CS pin low; shift-in the command code “20 or 21h” using the IO7:0 pins on both the rising and falling edge of CLK; continue to shift-in a 32-bit sector address using the IO[7:0] pins on both the rising and falling edge of CLK; and subsequently drive the /CS pin high to initiate the internal sector erase cycle. The ODDR Sector Erase command sequence is illustrated in Figure 12-3.

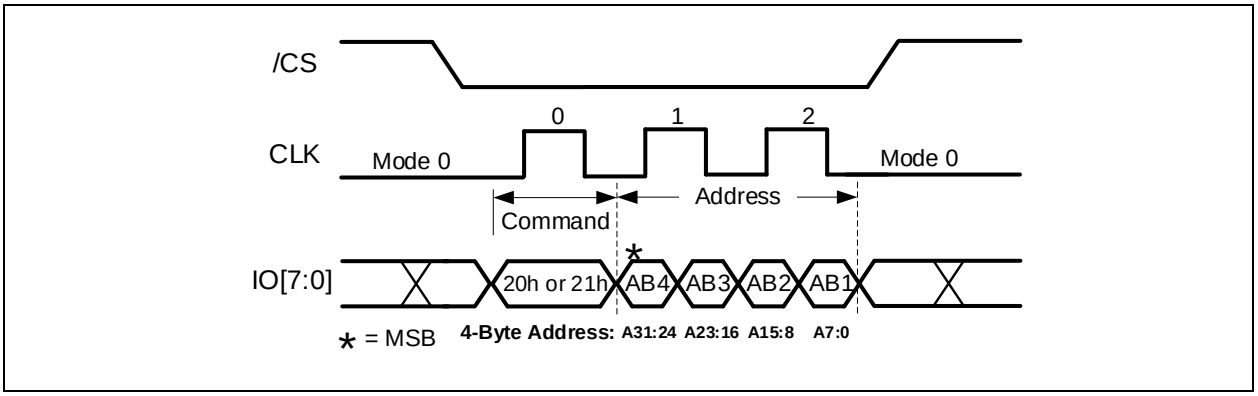


Figure 12-3. Octal DDR Sector Erase Command (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR mode

9.8.4 32KB Block Erase (52h)

The 32KB Block Erase command sets all bits within a specified block (32K-bytes) to the erased state of FFh (all 1s). In SDR mode and when the device is write enabled (WEL=1), the command is entered by driving the /CS pin low. This is followed by shifting in the command code “52h” and a 24-bit or a 32-bit sub-block address (depending on the Address Mode Configuration) using the IO0 pin on the rising edge of CLK. Subsequently, the /CS pin is driven high to initiate the internal sub-block erase cycle. The 32KB Block Erase command sequence is illustrated in Figure 12-4.

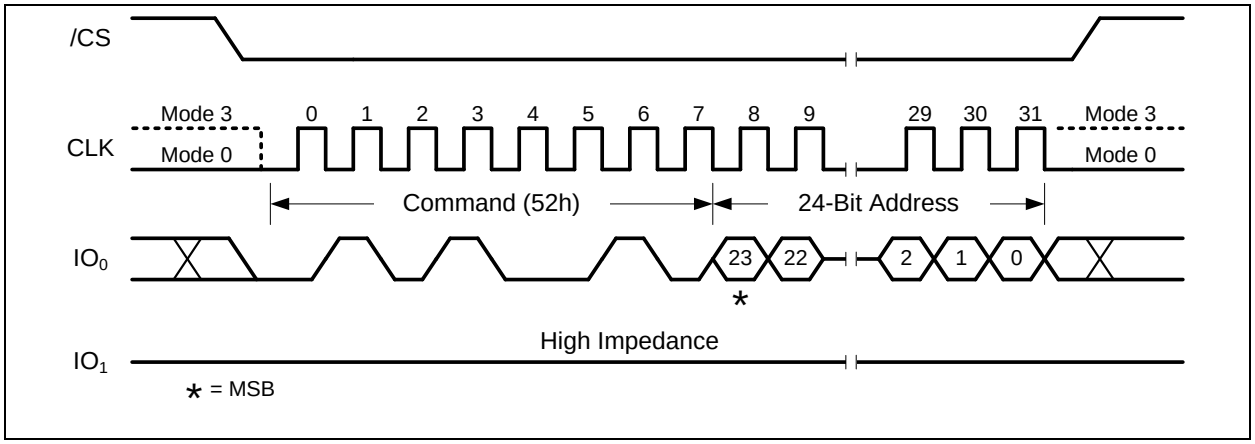


Figure 12-4. 32KB Block Erase Command (SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.8.5 32KB Block Erase with 4-Byte Address (5Ch)

In SDR mode, the 32KB Block Erase with 4-Byte Address command is similar to the 32KB Block Erase command except that it requires a 32-bit address instead of a 24-bit address to access the entire 512Mb memory. The Address Mode Configuration setting is not applicable (even in 3-Byte Address Mode).

Once the device is write enabled (WEL=1), the command is entered by driving the /CS pin low. This is followed by shifting in the command code “5Ch” and a 32-bit sub-block address using the IO0 pin on the rising edge of CLK. Subsequently, the /CS pin is driven high to initiate the internal sub-block erase cycle. The 32KB Block Erase using the 4-Byte Address command sequence is illustrated in Figure 12-5.

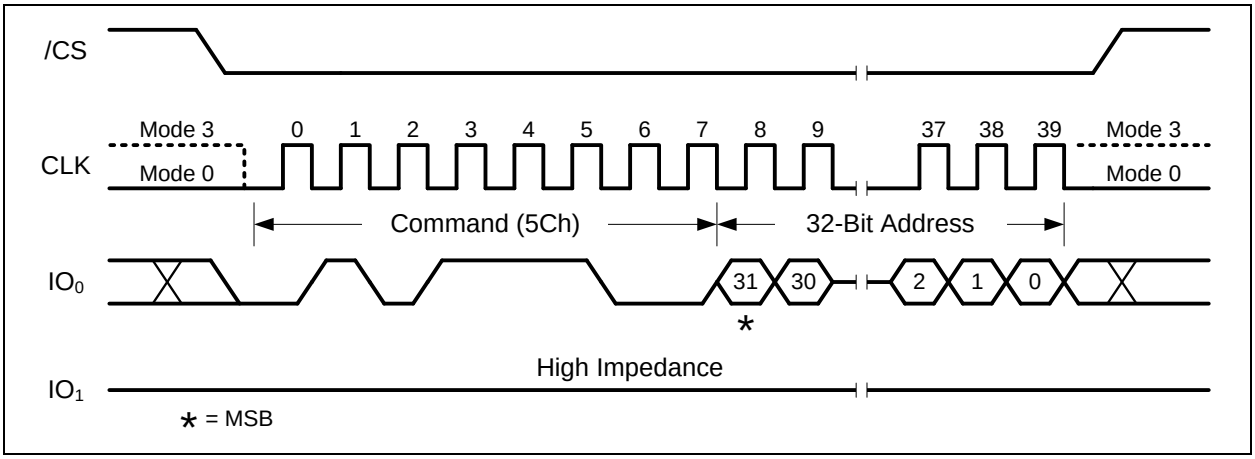


Figure 12-5. 32KB Block Erase using the 4-Byte Address Command (SDR Mode)

9.8.6 ODDR 32KB Block Erase (52 or 5Ch)

In ODDR mode, 32KB Block Erase command codes 52h and 5Ch are supported. In the ODDR 32KB Block Erase sequence, the command code is shifted-in using the IO[7:0] pins on both the rising and falling edge of CLK. Address Mode Configuration in ODDR mode uses only the 32-bit Address (4-Byte Address Mode) input. Address and Data also use IO[7:0] pins on both the rising and falling edge of CLK to latch in data.

Once the device is write enabled (WEL bit =1), the ODDR 32KB Block Erase command is initiated by the following sequence: drive the /CS pin low; shift-in the command code “52 or 5Ch” using the IO7:0 pins on both the rising and falling edge of CLK; continue to shift-in the 32-bit sub-block address using the IO[7:0] pins on both the rising and falling edge of CLK; and subsequently driving the /CS pin high to initiate the internal sub-block erase cycle. The ODDR 32KB Block Erase command sequence is illustrated in Figure 12-6.

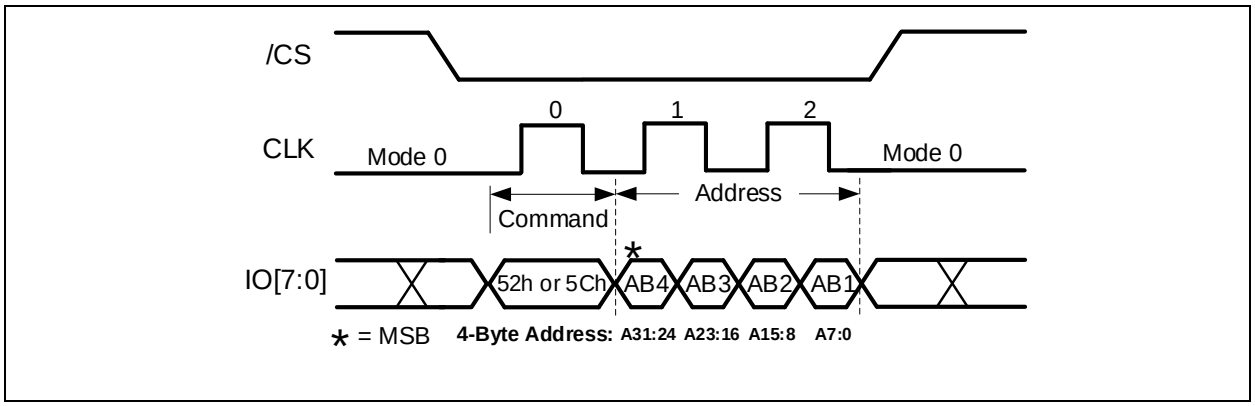


Figure 12-6. 32KB Block Erase Command (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR mode

9.8.7 64KB Block Erase (D8h)

The 64KB Block Erase command sets all bits within a specified block (64K-bytes) to the erased state of FFh (all 1s). In SDR mode and when the device is write enabled (WEL=1), the command is entered by driving the /CS pin low. This is followed by shifting in the command code “D8h” and a 24-bit or 32-bit block address (depending on the Address Mode Configuration) using the IO0 pin on the rising edge of CLK. Subsequently, the /CS pin is driven high to initiate the internal block erase cycle. The 64KB Block Erase command sequence is illustrated in Figure 12-7.

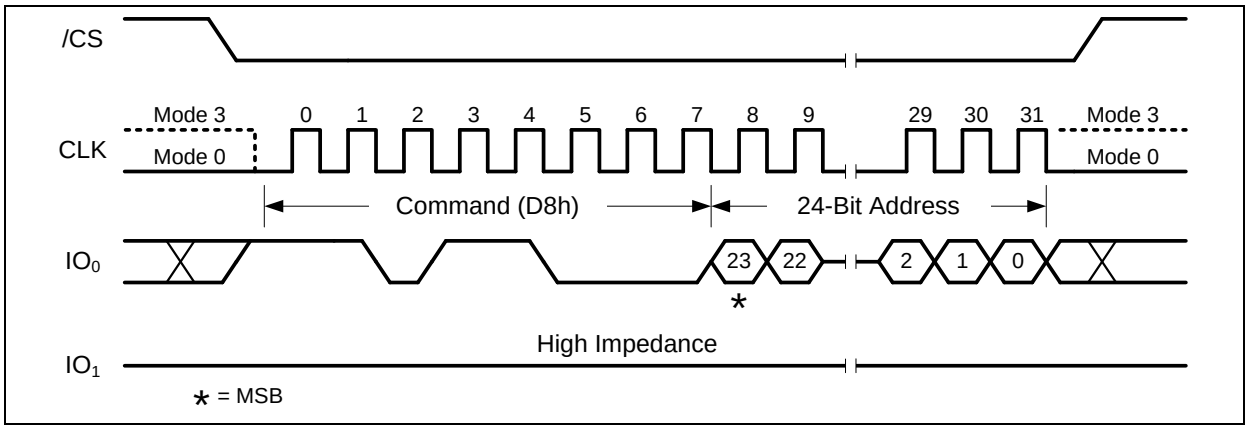


Figure 12-7. 64KB Block Erase Command (SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.8.8 64KB Block Erase with 4-Byte Address (DCh)

In SDR mode, the 64KB Block Erase using the 4-Byte Address command is similar to the 64KB Block Erase command except that it requires a 32-bit address instead of a 24-bit address to access the entire 512Mb memory. The Address Mode Configuration setting is not applicable (even in 3-Byte Address Mode).

Once the device is write enabled (WEL=1), the command is entered by driving the /CS pin low. This is followed by shifting in the command code “DCh” and a 32-bit block address using the IO0 pin on the rising edge of CLK. Subsequently, the /CS pin is driven high to initiate the internal block erase cycle. The 64KB Block Erase using the 4-Byte Address command sequence is illustrated in Figure 12-8.

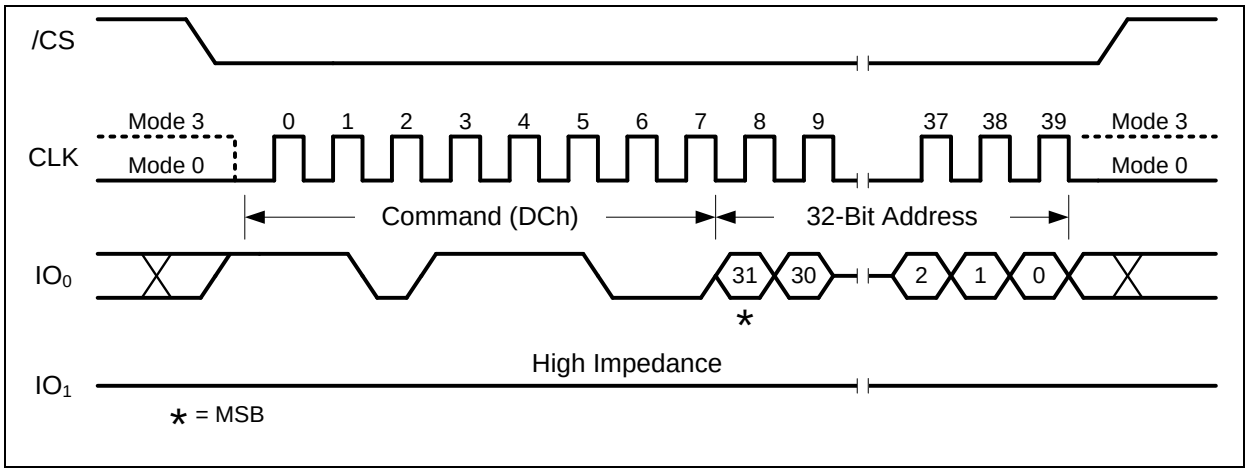


Figure 12-8. 64KB Block Erase using the 4-Byte Address Command (SDR Mode)

9.8.9 ODDR 64KB Block Erase (D8h or DCh)

In ODDR mode, 64KB Block Erase command codes D8h and DCh are supported. In the ODDR 64KB Block Erase sequence, command code is shifted-in using the IO[7:0] pins on both the rising and falling edge of CLK. Address Mode Configuration in ODDR mode uses a 32-bit Address (4-Byte Address Mode) input. Address and Data also use IO[7:0] pins on both rising and falling edge of CLK to latch in data.

Once the device is write enabled (WEL bit =1), the ODDR 64KB Block Erase command is initiated by the following sequence: drive the /CS pin low; shift-in the command code “D8h or DCh” using the IO7:0 pins on both the rising and falling edge of CLK; continue to shift-in a 32-bit block address using the IO[7:0] pins on both the rising and falling edge of CLK; and subsequently drive the /CS pin high to initiate the internal block erase cycle. The ODDR 64KB Block Erase command sequence is illustrated in Figure 12-9.

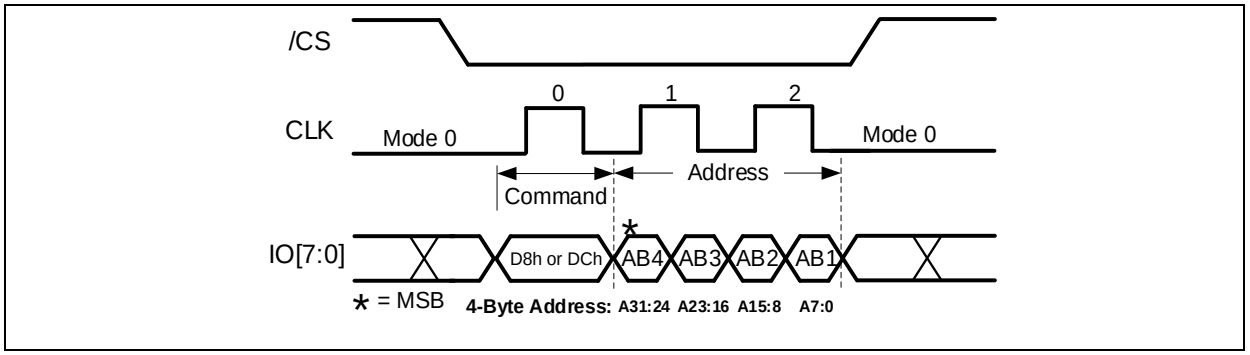


Figure 12-9. 64KB Block Erase Command (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR mode

9.8.10 Chip Erase (C7h / 60h)

The Chip Erase command sets all bits within the device to the erased state of FFh (all 1s). Once the device is write enabled (WEL bit =1), Chip Erase is entered by driving the /CS pin low. In SDR mode, the command code ‘C7h’ or ‘60h’ is shifted-in using the IO0 pin on the rising edge of CLK. In ODDR mode, the command code ‘C7’ or ‘60h’ is shifted-in using the IO[7:0] pins on the rising and falling edge of CLK. Driving the /CS pin high initiates the internal Chip Erase cycle. The Chip Erase sequences in SDR mode and ODDR mode are illustrated in Figure 12-10.

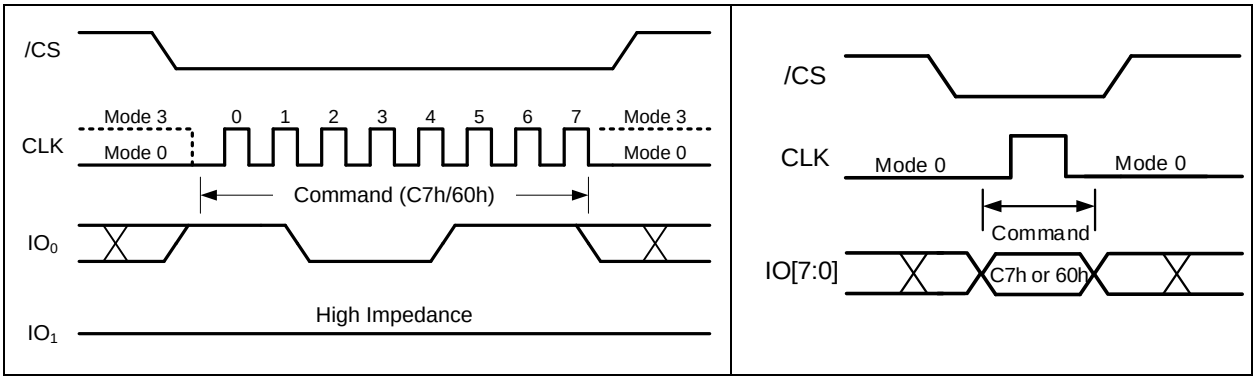


Figure 12-10. Chip Erase Command for SDR Mode (left) or ODDR Mode (right)

9.9 Suspend/Resume Commands

The Suspend/Resume command provides the host access to the device while it is busy with an internal program or erase operation. While the device is performing an internal program or erase operations, read access is not allowed and only Read Status Register, Read Flag Register, and Software Reset commands are acceptable. To read the device, the ongoing internal program or erase operation needs to be suspended temporarily by either a Program or Erase Suspend command. The Suspend command halts the ongoing internal program or erase operation, and the device memory range that is not suspended is read accessible. Read data on a suspended memory location returns indeterminate data.

There is a set of commands/operations the device can acknowledge or ignore when the device is erase suspended and a different set of commands/operations when the device is program suspended. The Device Operation Modes section (Section 6.10 Device Operating Modes or States) gives details on the acceptable commands when the device is in suspend mode.

When the device is erase suspended, all commands are accepted except for Write Status Register, Write NVCR/VCR, Program/Erase Security Register, and Erase Memory commands. A Page Program on a memory range that is not suspended is accepted when the device is erase suspended.

When the device is program suspended, all commands are accepted except for Write Status Register, Write NVCR/VCR, Program/Erase Security Register, Erase Memory commands, and Program memory.

The Erase/Program Resume command resumes a suspended erase/program operation. Nested suspend/resume operations are not supported.

9.9.1 Erase / Program Suspend (75h)

The Erase/Program Suspend command “75h”, allows the system to temporarily stop an internal Sector/Block Erase operation or a Page Program operation, then perform a read register or program memory outside the erase suspended memory range. In SDR mode, the Erase/Program Suspend command is entered by driving the /CS pin low, followed by shifting in the Erase/Program Resume command code ‘75h’ using the IO0 pin on the rising edge of CLK, and subsequently driving /CS pin high to initiate the command. Figure 13-1a illustrates the Erase/Program Suspend command sequence in SDR mode.

In ODDR mode, the Erase/Program Suspend command is entered by driving the /CS pin low, followed by shifting in the Erase/Program Resume command code ‘75h’ using the IO[7:0] pins on both the rising and falling edge of CLK, and subsequently driving the /CS pin high to initiate the command. Figure 13-1b illustrates the Erase/Program Suspend command sequence in ODDR mode.

The Write Status Register command (01h), Write Non-Volatile Configuration Register (B1h), Program/Erase Security Register (42h/44h), and Erase commands (20h, 21h, 52h, 5Ch, D8h, DCh, C7h, 60h) are not allowed during Erase Suspend. Erase Suspend is valid only during Sector or Block erase operations. If issued during the Chip Erase operation, the Erase Suspend command is ignored.

The Write Status Register command (01h), Write Non-Volatile Configuration Register (B1h), Program Security Register (42h), and Program commands (02h, 12h, 82h, 84h, C2h, 8Eh) are not allowed during Program Suspend. Program Suspend is valid only during Page Program or Octal Page Program operations.

There are two Flag Register bits associated with the Erase/Program Suspend command. One is the Erase Suspend Flag bit (Flag Register Bit 6) for erase suspend status and the other is the Program Suspend Flag bit (Flag Register Bit 2). Depending on the active internal operation (either erase or program), once a Erase/Program Suspend command is accepted, the corresponding suspend flag will be set (ESF for Erase Suspend or PSF for Program Suspend). A maximum time of ‘tSUS’ (see AC Characteristics) is required to suspend the erase or program operation. Then, the Flag Register Bit 7 (Ready Flag - RF) is set to ‘1’ and the Status Register Busy Bit (Bit 0) is cleared to a ‘0’. The device is in suspend mode after at least one byte of the RF flag (F7) is a ‘1’. When the device is in suspend mode, it is ready to accept or ignore commands as indicated in the device operation modes section.

If the internal erase or program time is less than the suspend latency time when the Erase/Program Suspend command is accepted, the suspend command is ignored. The internal erase or program operation will continue and will clear either the ESF or PSF bits to '0'.

The device accepts a Page Program command when the device is in the Erase Suspend mode, but the target page address has to be outside of the suspended sector. Block Programming on a suspended memory range is not recommended as it can cause data corruption.

Unexpected power off during the Erase/Program suspend state will reset the device and the suspend status. The PSF and ESF bits (the 8-bit Flag Register) status will be reset to '0'. The Flag Register will power up as default 80h. The data within the page, sector or block that was suspended may become corrupted. Design techniques against accidental power interruption and data preservation during the erase/program suspend state are highly recommended.

Details of supported commands while the device is suspended are listed on Section 6.10 Device Operating Modes or States.

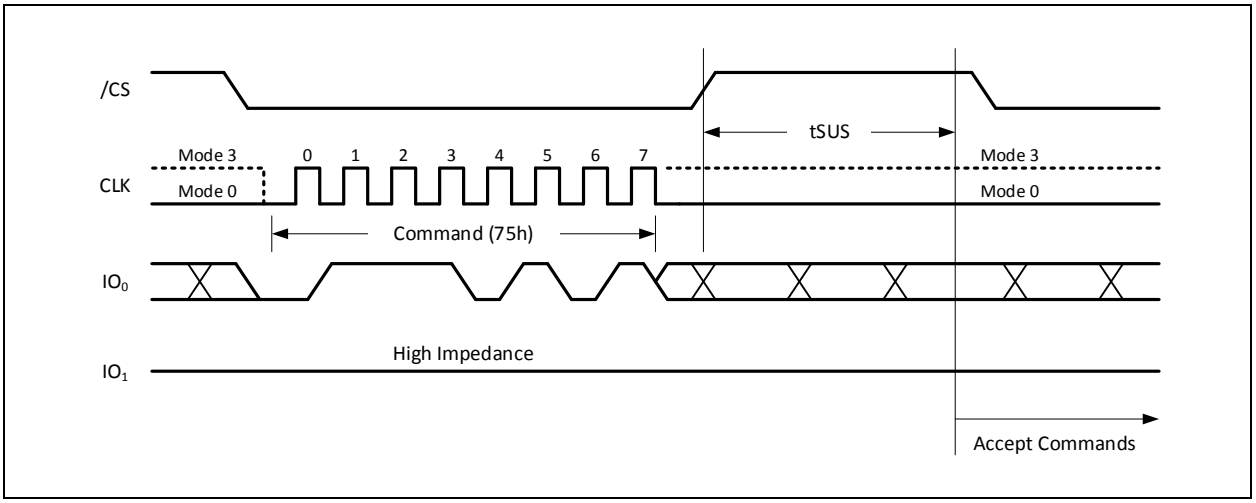


Figure 13-1a. Erase/Program Suspend Command (SDR Mode)

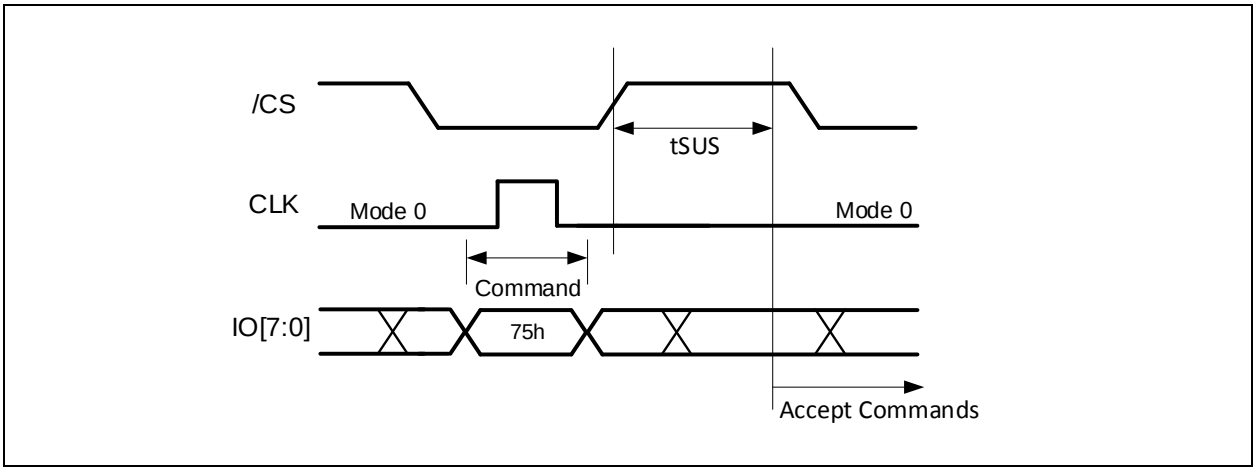


Figure 13-1b. Erase/Program Suspend Command (ODDR Mode)

9.9.2 Erase / Program Resume (7Ah)

The Erase/Program Resume command “7Ah” resumes a Sector Erase, Block Erase or Page Program operation that was suspended. The Resume command “7Ah” will be accepted by the device only if either the ESF or PSF bit and the RF bit of the Flag Register are set to ‘1’ and the BUSY bit of Status Register is cleared to ‘0’.

After an Erase/Program Resume command is issued, the ESF or PSF bit and RF bit of the Flag Register are cleared to ‘0’, and the BUSY bit of Status Register is set to ‘1’. Either the ESF or PSF bits will be cleared immediately from 1 to 0. The RF and BUSY bit will be set from 0 to 1 within 200ns. The internal sector or block erase operation or the internal page program operation on the targeted address range will resume.

In SDR mode, the Erase/Program Resume command is entered by driving the /CS pin low, followed by shifting in the Erase/Program Resume command code ‘7Ah’ using the IO0 pin on the rising edge of CLK, and subsequently driving /the CS pin high to initiate the command. Figure 13-2a illustrates the Erase/Program Resume command in SDR mode.

In ODDR mode, the Erase/Program Resume command is entered by driving the /CS pin low, followed by shifting in the Erase/Program Resume command code ‘7Ah’ using the IO[7:0] pins on both the rising and falling edge of CLK, and subsequently driving the /CS pin high to initiate the command. Figure 13-2b illustrates the Erase/Program Resume command in ODDR mode.

The Erase/Program Resume command is ignored if the device is not in Suspend mode when the ESF and PSF bits are ‘0’. The Resume command is ignored if the previous Erase/Program Suspend operation was interrupted by an unexpected power down.

It is also required that a subsequent Erase/Program Suspend command is not issued within a minimum of time of “t_{SUS}” following a previous Resume command.

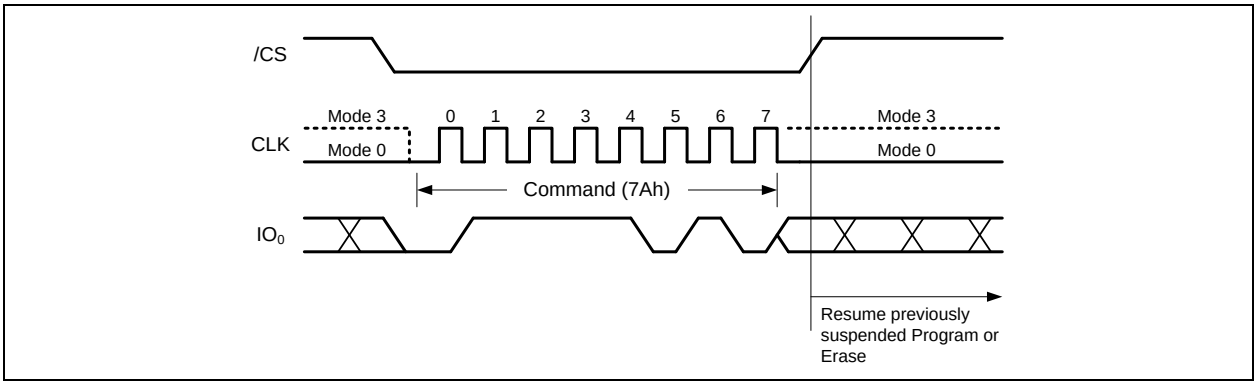


Figure 13-2a. Erase/Program Resume Command (SDR Mode)

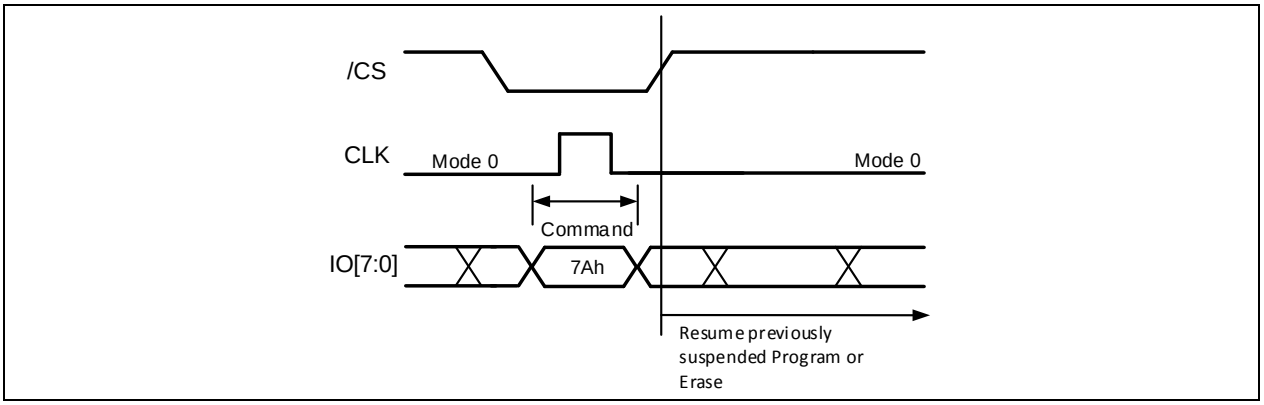


Figure 13-2b. Erase/Program Resume Command (ODDR Mode)

9.10 Unique ID and Security Register Commands

The W35T51NW has a 128-bit (16-Byte) Unique ID and three 1K-Byte Security Registers. The Unique ID is accessible by using the Read Unique ID (4Bh) command. The Security Registers are readable, programmable, erasable, and lockable (OTP or Volatile option). The Read Security Register (48h) command is used to read the Security Register. The Program Security Register (42h) command is used to program the Security Register, while the Erase Security Register (44h) is used to erase the register. The Unique ID and Security Register commands are supported in both SDR and ODDR mode.

9.10.1 Read Unique ID (4Bh)

The Read Unique ID (4Bh) command accesses a factory-set read-only 16-byte ID that is unique to each W35T51NW device. The ID number can be used in conjunction with a user software mechanism to help prevent copying or cloning of a system.

In SDR mode, the Read Unique ID command is initiated by driving the /CS pin low, shifting the command code “4Bh” using the IO0 pin on the rising edge of CLK, followed by 24/32bit dummy address clocks depending on the address mode setting, and an additional dummy byte; the 16-byte UID is then shifted out on the falling edge of CLK on the IO1 pin with the lower byte first as shown in Figure 14-1a.

In ODDR mode, the Read Unique ID command is initiated by driving the /CS pin low, shifting the command code ‘4Bh’ using the IO[7:0] pins on both the rising and falling edge of CLK. Four dummy bytes are shifted using the IO[7:0] pins on both the rising and falling edge of CLK. This is followed by 16 dummy CLK cycles, and IO[7:0] will transition from input to output on the last falling edge of the 16th dummy clock cycle. Each byte of UID data is shifted out on IO[7:0] on both the falling and rising edge of CLK starting with the upper byte (UID Byte[15]). Once the last UID Byte[0] is reached, a continuous CLK input will wrap back to data output UID Byte[15]. Driving the /CS pin high completes the command. Figure 14-1b illustrates Read Unique ID in ODDR mode.

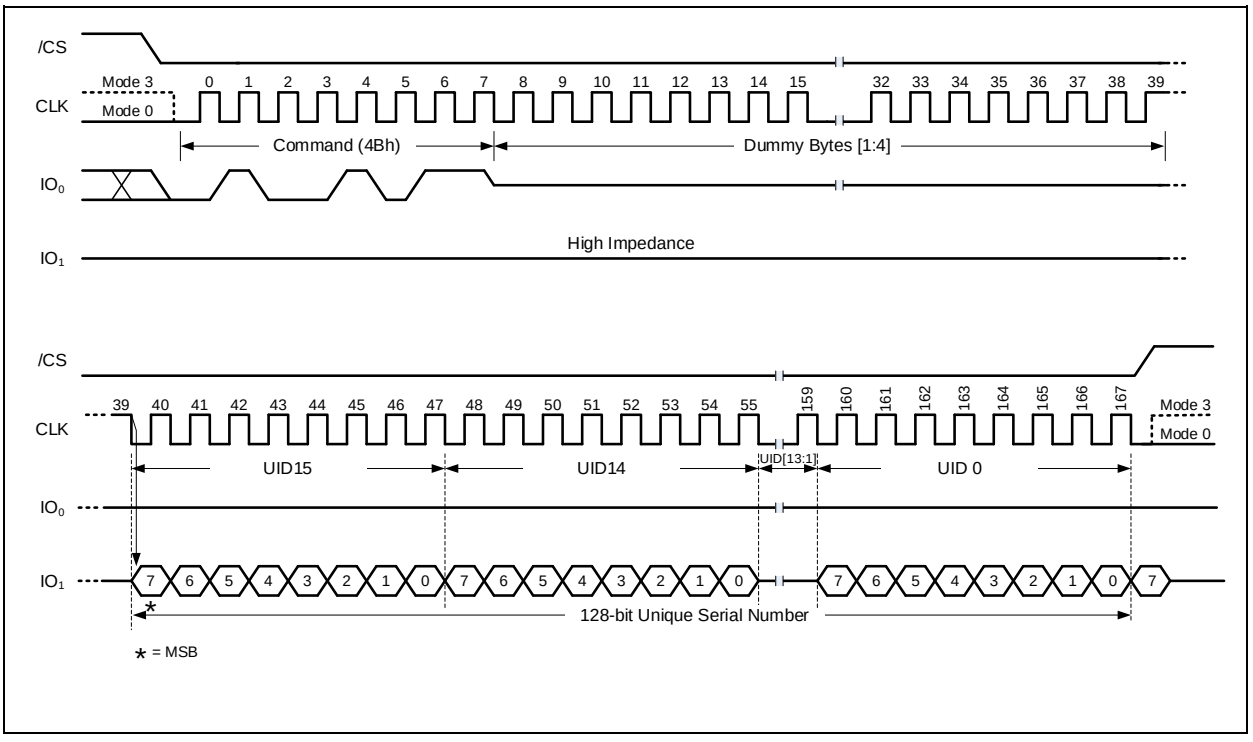


Figure 14-1a. Read Unique ID Command (SDR Mode)

5 Dummy Bytes are required when the device is operating in 4-Byte Address Mode

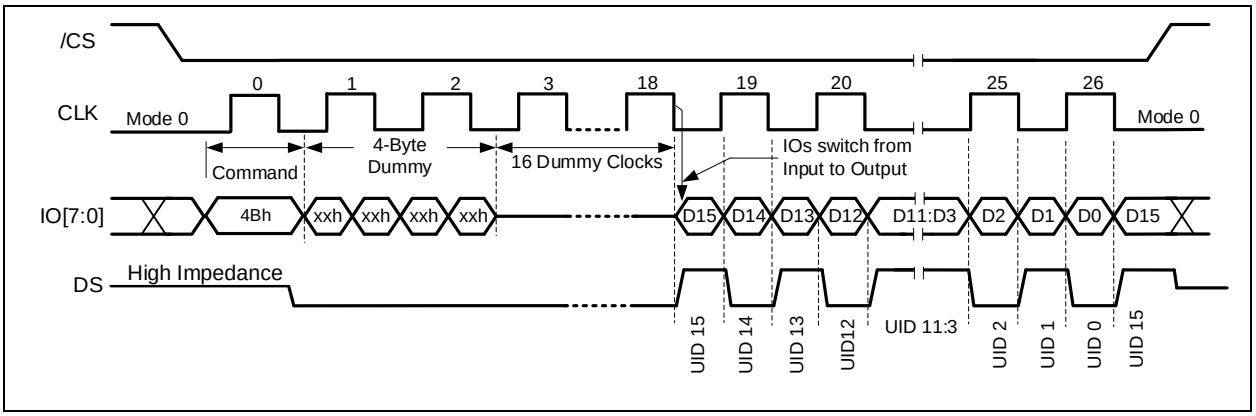


Figure 14-1b. Read Unique ID Command (ODDR Mode)

32-Bit Dummy Input is required when the device is operating in ODDR mode

9.10.2 Erase Security Registers (44h)

The Erase Security Register command is similar to the Sector Erase command. A Write Enable command must be executed before the device will accept an Erase Security Register Command (Status Register WEL bit must equal 1).

In SDR mode, erasing one of the three security registers is initiated by driving the /CS pin low and shifting the command code “44h” followed by a 24/32-bit address (A23/A31-A0) on the IO0 pin. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the command will not be executed. After the /CS is driven high, the self-timed Erase Security Register operation will commence for a duration of t_{SE} (See AC Characteristics). While the Erase Security Register cycle is in progress, the Read Status Register command may still be accessed for checking the status of the BUSY bit. The BUSY bit is 1 during the erase cycle and becomes 0 when the cycle is finished, and the device is ready to accept new commands. After the Erase Security Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Erase Security Register command sequence in SDR mode is shown in Figure 14-2a.

In ODDR mode, the Erase Security Register is initiated by the following sequence: drive the /CS pin low; shift-in the command code “44h” using the IO[7:0] pins on both the rising and falling edge of CLK; continue to shift-in a 32-bit address on IO[7:0] pins on both edges of CLK; and subsequently drive the /CS pin high to initiate the internal security register erase cycle. The Erase Security Register command sequence in ODDR mode is illustrated in Figure 14-2b.

ADDRESS	{A23/A31}-16	A15-12	A11-8	A7-0
Security Register #1	00h/0000h	0 0 0 1	Don’t Care	Don’t Care
Security Register #2	00h/0000h	0 0 1 0	Don’t Care	Don’t Care
Security Register #3	00h/0000h	0 0 1 1	Don’t Care	Don’t Care

The NVCR-OLB and VCR-VLB bits can provide security registers protection against program and erase. Once a lock bit is set to 1, the corresponding security register will either be OTP or volatile locked. The NVCR-OLB bits are one-time programmable lock bits and once set to ‘1’, the corresponding Security Register will be read only and locked permanently. The VCR-VLB bits are volatile and configurable and will reset to their default values by a reset or power cycle.

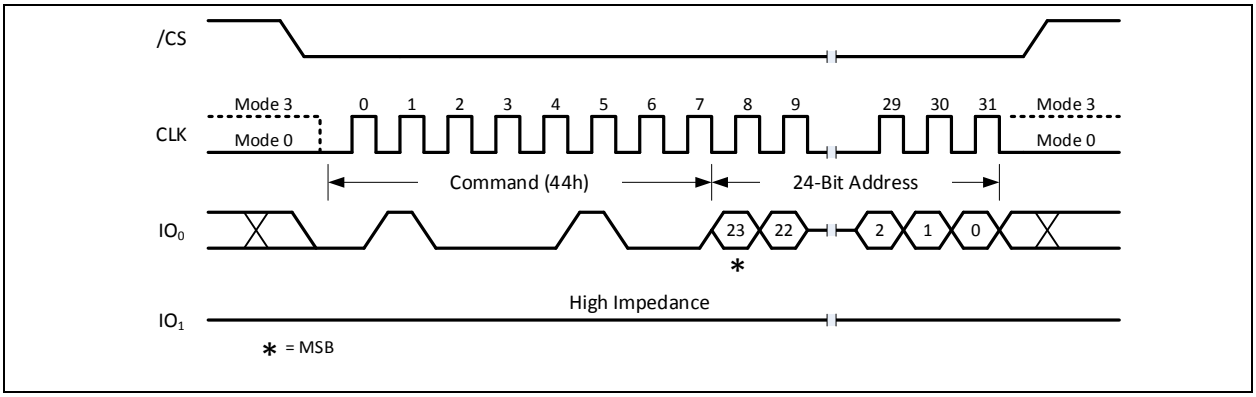


Figure 14-2a. Erase Security Registers Command (SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

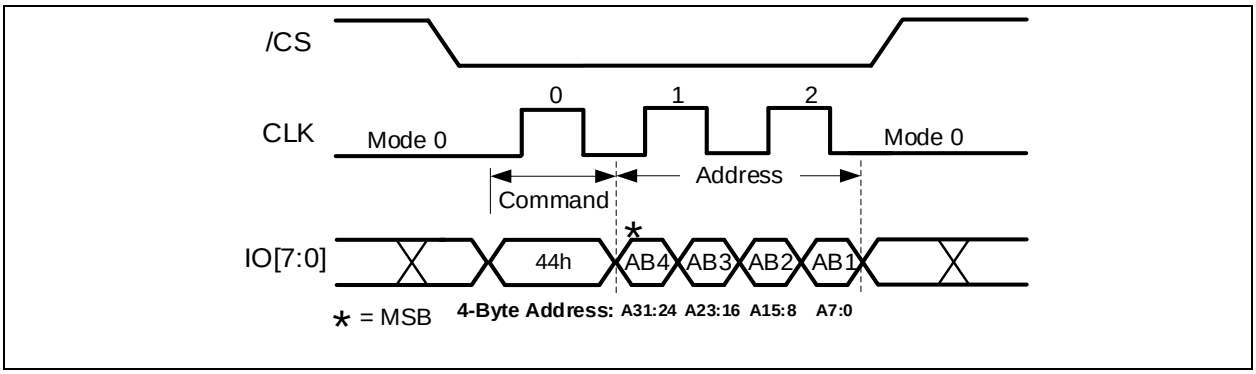


Figure 14-2b. Erase Security Registers Command (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR mode

9.10.3 Program Security Registers (42h)

The Program Security Register command is similar to the Page Program (02h) command. It allows the programming of one byte up to 256 bytes of the security register data at previously erased (FFh) memory locations. A Write Enable command must be executed before the device will accept the Program Security Register Command (Status Register bit WEL= 1).

In SDR mode, the command is initiated by driving the /CS pin low then shifting the command code “42h” followed by a 24/32-bit address (A23/A31-A0) and at least one data byte into the DI pin. The /CS pin must be held low for the entire length of the command while data is being sent to the device. The Program Security Register command sequence in SDR mode is shown in Figure 14-3a.

In ODDR mode, the Program Security Register is initiated by the following sequence: drive the /CS pin low; shift-in the command code “42h” using the IO[7:0] pins on both the rising and falling edge of CLK; continue to shift-in a 32-bit address and 1 to 256 bytes of data using the IO[7:0] pins on both edges of CLK; and subsequently drive the /CS pin high to initiate the internal security register program cycle. The Program Security Register command sequence in ODDR mode is illustrated in Figure 14-3b.

ADDRESS	{A23/A31}-16	A15-12	ADDRESS RANGE (A[11:0])
Security Register #1	00h/0000h	0 0 0 1	000H – 3FFH
Security Register #2	00h/0000h	0 0 1 0	000H – 3FFH
Security Register #3	00h/0000h	0 0 1 1	000H – 3FFH

The NVCR-OLB and VCR-VLB bits can provide security registers protection against program and erase. Once a lock bit is set to 1, the corresponding security register will either be OTP or volatile locked. The NVCR-OLB bits are one-time programmable lock bits and once set to ‘1’, the corresponding Security Register will be read only and permanently locked. The VCR-VLB bits are volatile and configurable and will reset to their default values by reset or power cycle.

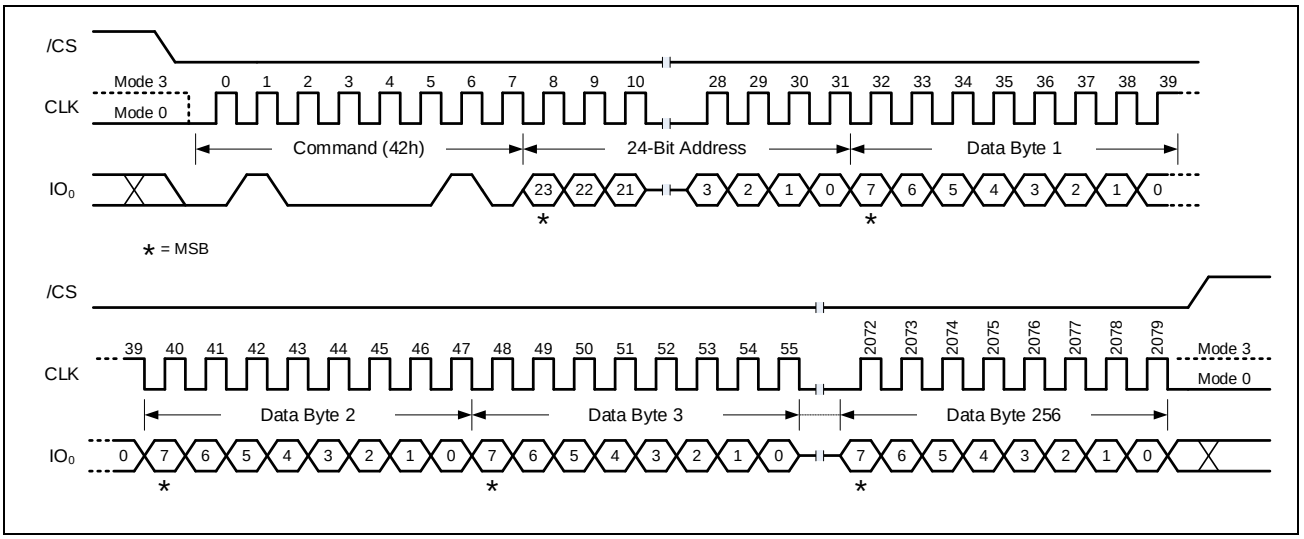


Figure 14-3a. Program Security Registers Command (SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

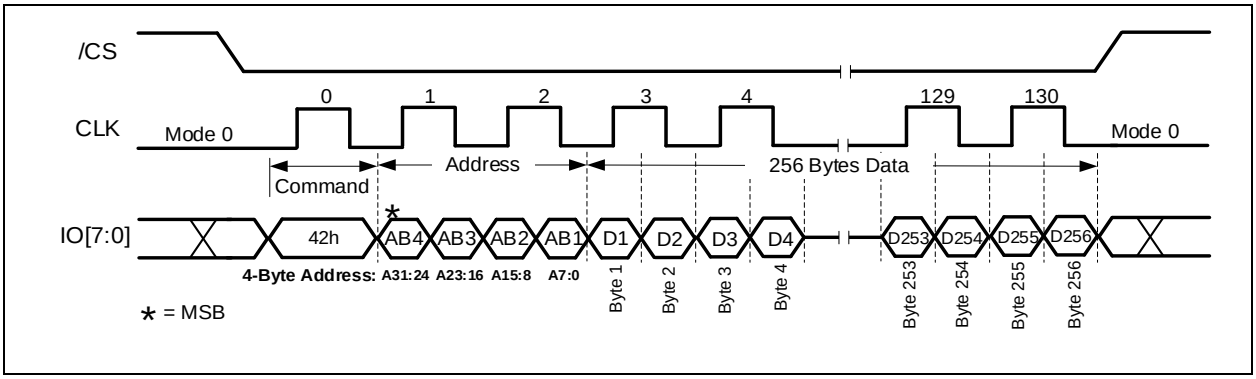


Figure 14-3b. Program Security Registers Command (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR mode

9.10.4 Read Security Registers (48h)

The Read Security Register command is similar to the Fast Read command and allows one or more data bytes to be sequentially read from one of the four security registers. In SDR mode, the command is initiated by driving the /CS pin low and then shifting the command code “48h” followed by a 24/32-bit address (A23/A31-A0) and eight “dummy” clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with the most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte address FFh), it will wrap around to the first byte of the target Security Register and continue to increment. The command is completed by driving /CS high. The Read Security Register command sequence in SDR mode is shown in Figure 14-4a.

In ODDR mode, the Read Security Register command is initiated by driving the /CS pin low and shifting the command code ‘48h’ using the IO[7:0] pins on both the rising and falling edge of CLK. A 32-bit address is shifted using the IO[7:0] pin on both the rising and falling edge of CLK after the command. This is followed by 16 dummy CLK cycles (default/programmable) and IO[7:0] will transition from input to output on the falling edge of the last dummy clock cycle. Each data byte (output data) is shifted out on IO[7:0] on both the falling and rising edge of CLK starting from the target address. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the highest memory address, it will wrap-around back to the target Security Register address 0000x000h. The command is completed by driving the /CS pin high. Figure 14-4b illustrates the Read Security Register sequence in ODDR mode.

If a Read Security Register command is issued while an Erase, Program or Write cycle is in process (BUSY=1), the command is ignored and will not have any effect on the current cycle. The Read Security Register command allows clock rates from D.C. to a maximum of F_R (see AC Electrical Characteristics).

ADDRESS	{A23/A31}-16	ADDRESS RANGE (A[15:A0])
Security Register #1	00h/0000h	1000H – 13FFH
Security Register #2	00h/0000h	2000H – 23FFH
Security Register #3	00h/0000h	3000H – 33FFH

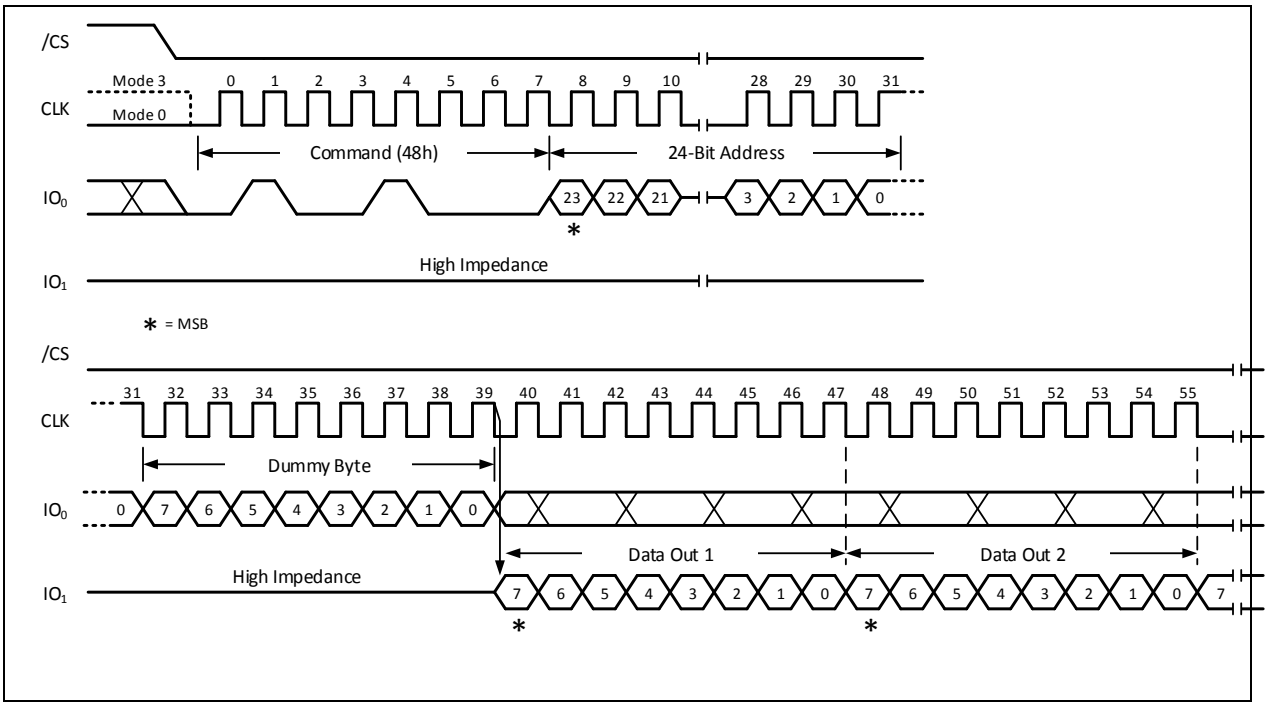


Figure 14-4a. Read Security Registers Command (SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

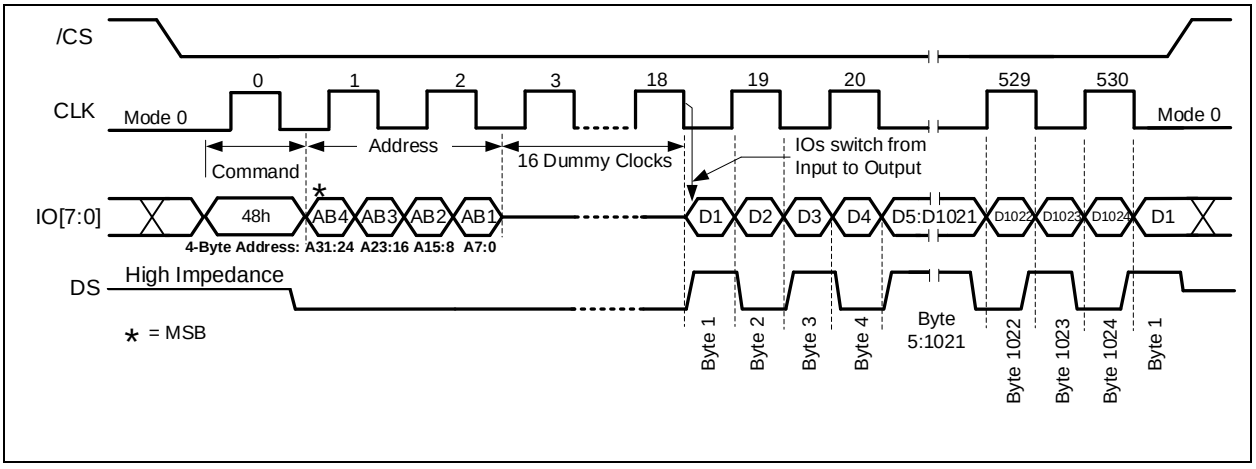


Figure 14-4b. Read Security Registers Command (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR Mode

9.11 Deep Power-down Commands

The Power-down and Release Power-down commands are two commands associated with power saving modes. When the device is idle and not in use, some applications may require lower power consumption from the flash device. The Power-down mode command gives flexibility to reduce standby current even further. Once the device is in power-down mode, all commands are ignored except for Release Power-down command. The Release Power-down command exits power-down mode and brings back the device to standby ready. The Power-down and Release Power-down commands are supported in both SDR and ODDR mode.

9.11.1 Power-down (B9h)

Although the standby current during normal operation is relatively low, it can be further reduced with the Power-down command. The lower power consumption is especially useful for battery powered applications.

In SDR mode, the Power-down command is initiated by driving the /CS pin low, shifting the command code “B9h” using the IO0 pin on the rising edge of CLK, and driving /the CS pin high as shown in Figure 15-1a.

In ODDR mode, the Power-down command is entered by driving the /CS pin low, shifting the command code “B9h” using the IO[7:0] pins on both the rising and falling edge of CLK, and driving the /CS pin high. This puts the device in power-down mode after tPD time as illustrated in Figure 15-1b.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done, the Power-down command will not be executed. After /CS is driven high, power-down state will be entered within a duration of tDP (See AC Characteristics). While in power-down state, only the Release Power-down (ABh) command, which restores the device to normal operation, will be recognized. All other commands are ignored including the Read Status Register command, which is always available during normal operation. Ignoring all but one command makes Power Down state a useful condition for maximum write protection. The device always powers-up in normal operation with the standby current of ICC1.

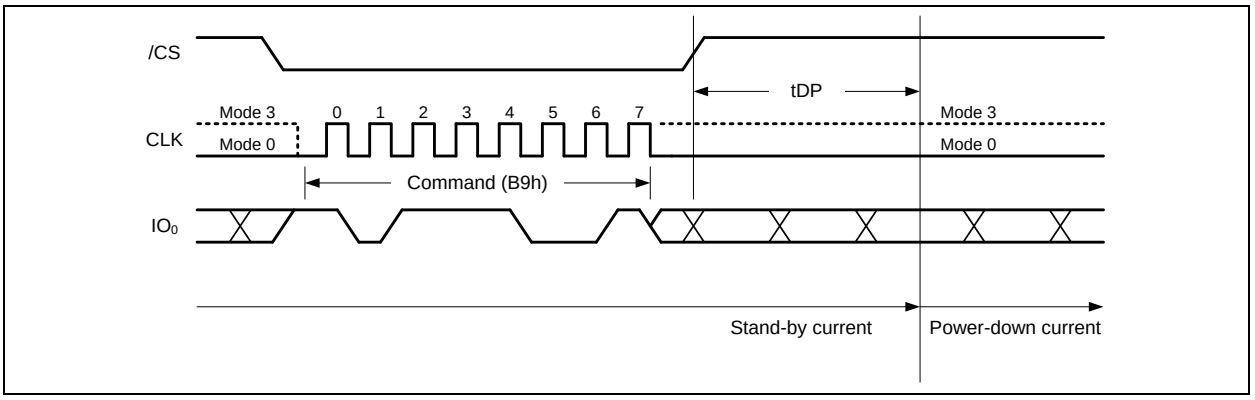


Figure 15-1a. Deep Power-down Command (SDR Mode)

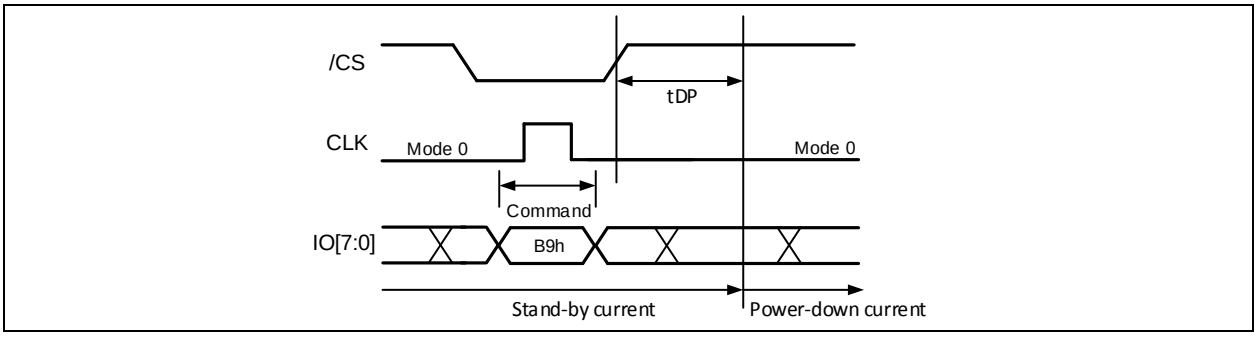


Figure 15-1b. Deep Power-down Command (ODDR Mode)

9.11.2 Release Power-down (ABh)

The Release Power-down command is used to release the device from the power-down state and back to standby mode. This command is supported in both SDR and ODDR mode.

To release the device from a power-down state in SDR mode, the Release Power-down command is entered by driving the /CS pin low, shifting the command code “ABh” using the IO0 pin on the rising edge of CLK, and driving the /CS pin high as illustrated in Figure 15-2a. In ODDR mode, the Release Power-down command is entered by driving the /CS pin low, shifting the command code “ABh” using the IO[7:0] pins on both the rising and falling edge of CLK, and driving the /CS pin high. The device exits power-down mode after time t_{RES1} as illustrated in Figure 15-2b.

Release from power-down will take a duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation. The /CS pin must remain high during this time t_{RES1}.

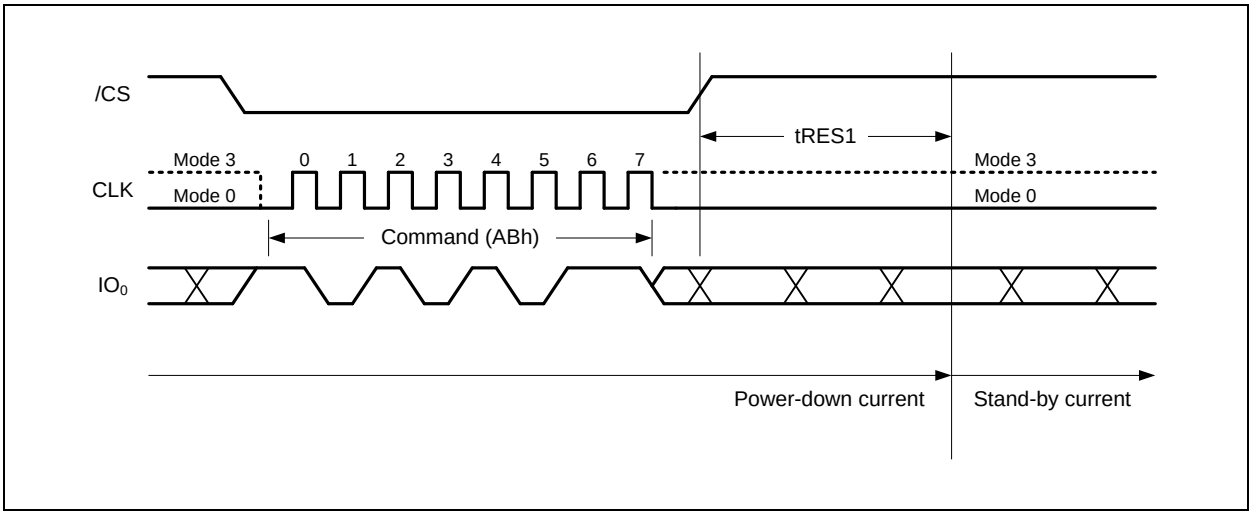


Figure 15-2a. Release Power-down Command (SDR Mode)

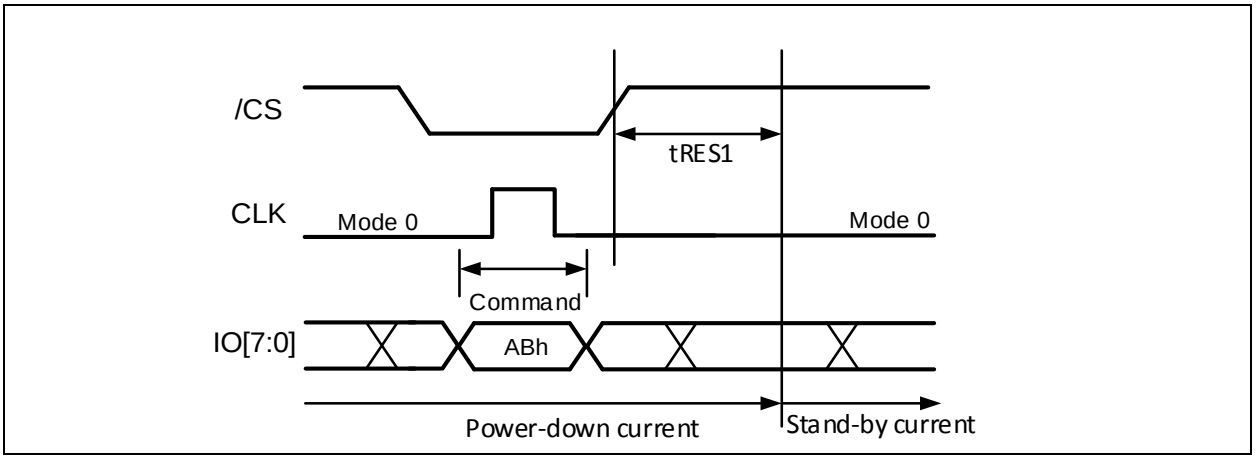


Figure 15-2b. Release Power-down Command (ODDR Mode)

9.12 ECC Registers Commands

The W35T51NW device has two ECC registers, the ECC Status Register and the 8-byte Advanced ECC Register, which controls the ECC settings and monitors ECC events. The ECC Status Register is read accessible by the Read ECC Status Register (25h) command, while the Write ECC Status Register (56h) command can write to its writable register bits. The Advanced ECC Register is accessible by the Read Advanced ECC Register (7Dh) and the Reset ECC Counters (72h) commands. The detailed timing sequence of ECC Register commands are defined in the next sections.

9.12.1 Read ECC Status Register (25h)

The ECC Status Register includes SEC, DED, ECC, INT, and ECC ON/OFF bits as described in Section 7.12.1 ECC Status Register. The Read ECC Status Register command is entered by driving /CS low and shifting the command code “25h” using the DI pin on the rising edge of CLK. The ECC Status Register bits are then shifted out on the DO pin at the falling edge of CLK with the most significant bit (MSB) first as shown in Figure 16-1a. The Read ECC Status Register command in ODDR mode sequence is shown in Figure 16-1b.

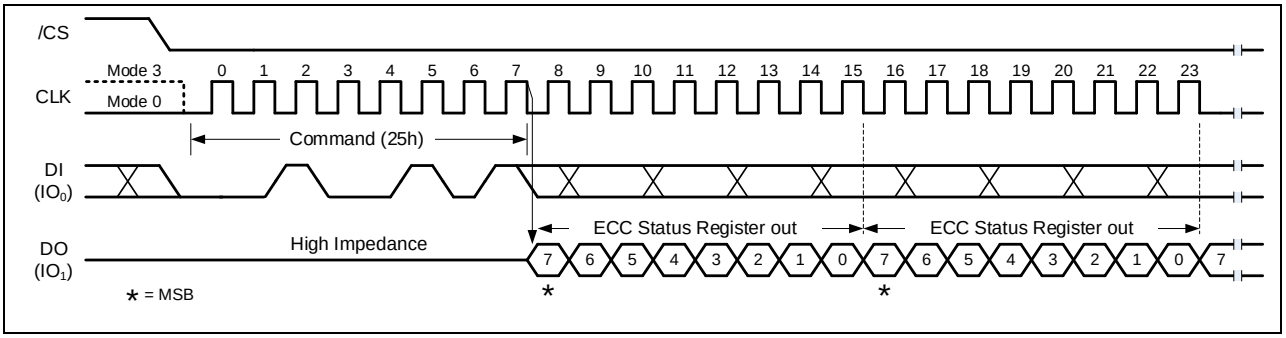


Figure 16-1a. Read ECC Status Register Command (SDR Mode)

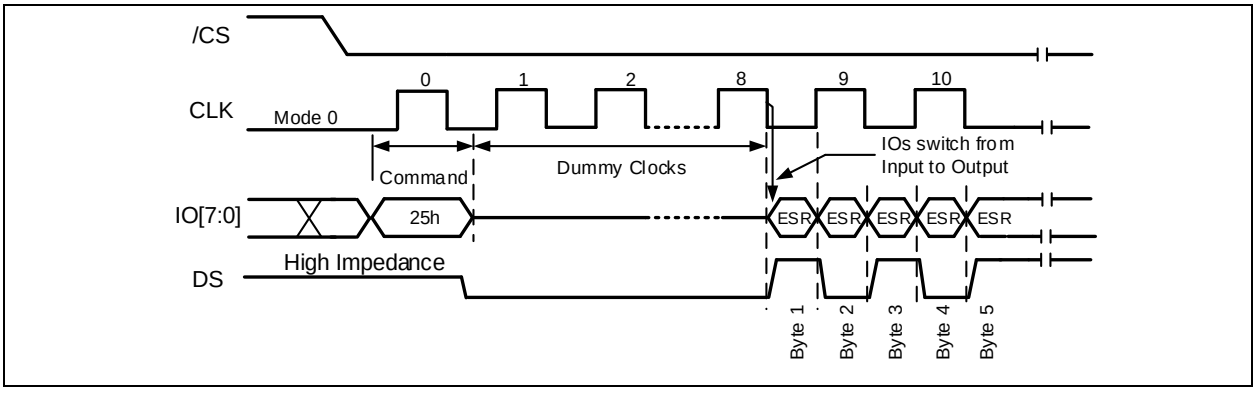


Figure 16-1b. Read ECC Status Register Command (ODDR Mode)

9.12.2 Write ECC Status Register (56h)

To write the ECC Status Register bits, a Write Enable (06h) command must be executed before the device accepts the Write ECC Status Register command (Status Register bit WEL must equal 1). Once write enabled, the command is entered by driving /CS low, sending the command code “56h”, and then writing the ECC Status Register data bits as illustrated in Figure 16-2a and 16-2b.

This write register (56h) is used to set ECC and INT bits (ER2 – ER1) which are described in Section 7.12.1 ECC Status Register.

Upon power-up or Software/Hardware Reset, the ECC Status Register bits are cleared to 0 with the exception of the ECC bit, which is default to 1.

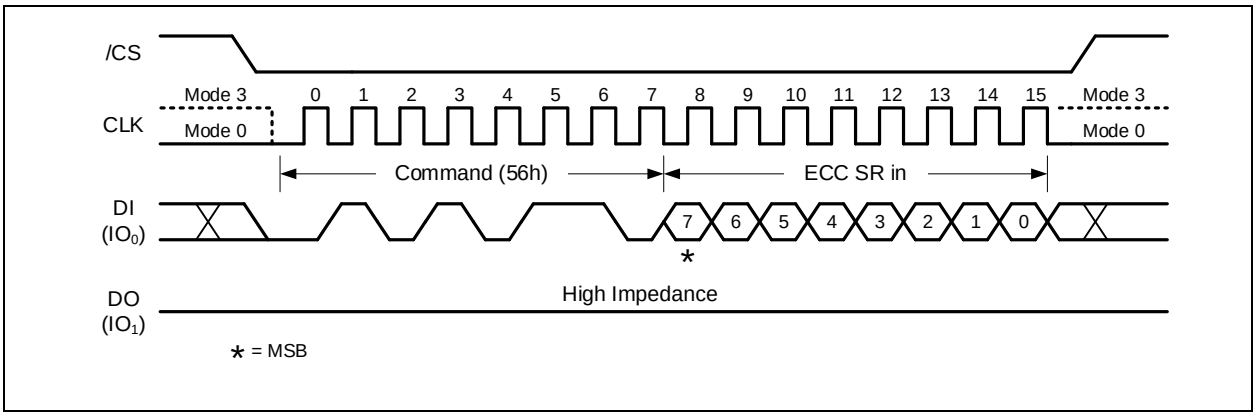


Figure 16-2a. Write ECC Status Register Command (SDR Mode)

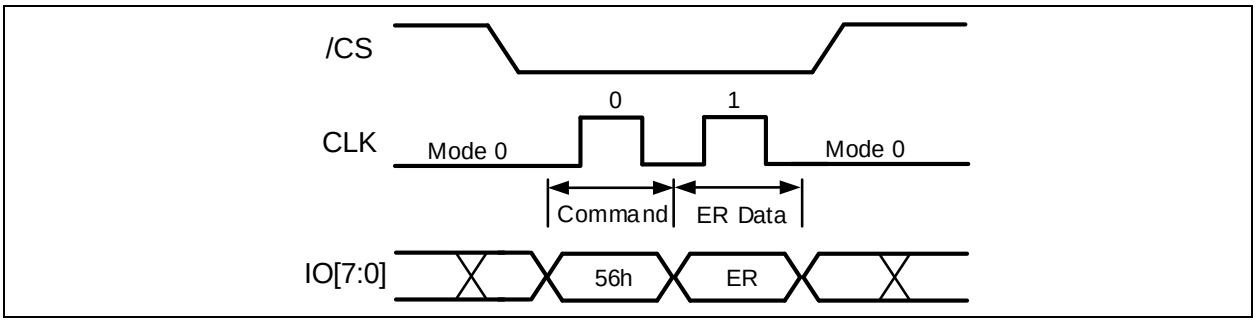


Figure 16-2b. Write ECC Status Register Command (ODDR Mode)

9.12.3 Reset ECC Counters (72h)

The Reset ECC Counters (72h) command clears the SEC Address Captured Valid Flag (SACVF), DED Address Captured Valid Flag (DACVF), Single Error Correction Counter (SC[3:0]) and the Double Error Detection Counter (DC[3:0] of the 8-Byte Advanced ECC Register) to zero (0b, 0b, '0000b', and 0000b respectively). After a successful power-on-reset or a hardware/software reset, the SACVF, DACVF, SC[3:0] and DC[3:0] counter values are also reset to zero (0b, 0b, '0000b', and 0000b respectively).

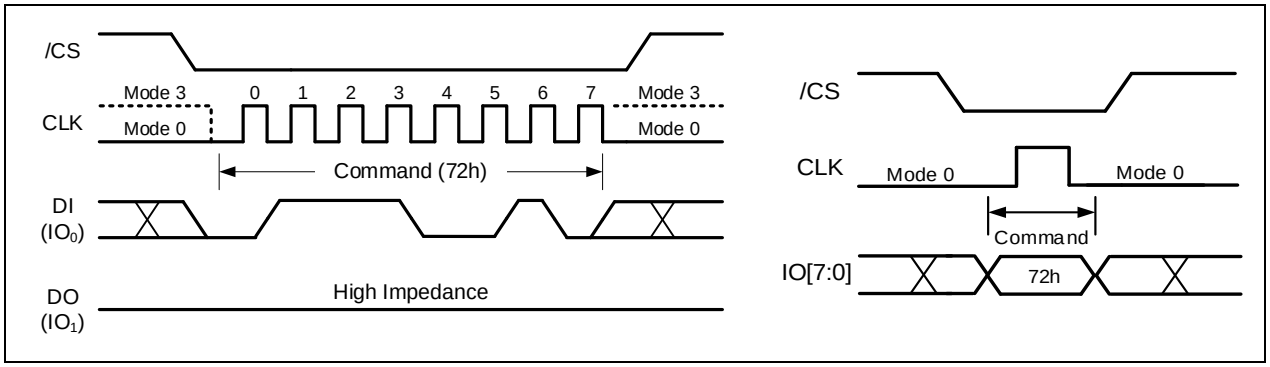


Figure 16-3. Reset ECC Counters for SDR Mode (left) or ODDR Mode (right)

9.12.4 Read Advanced ECC Register (7Dh)

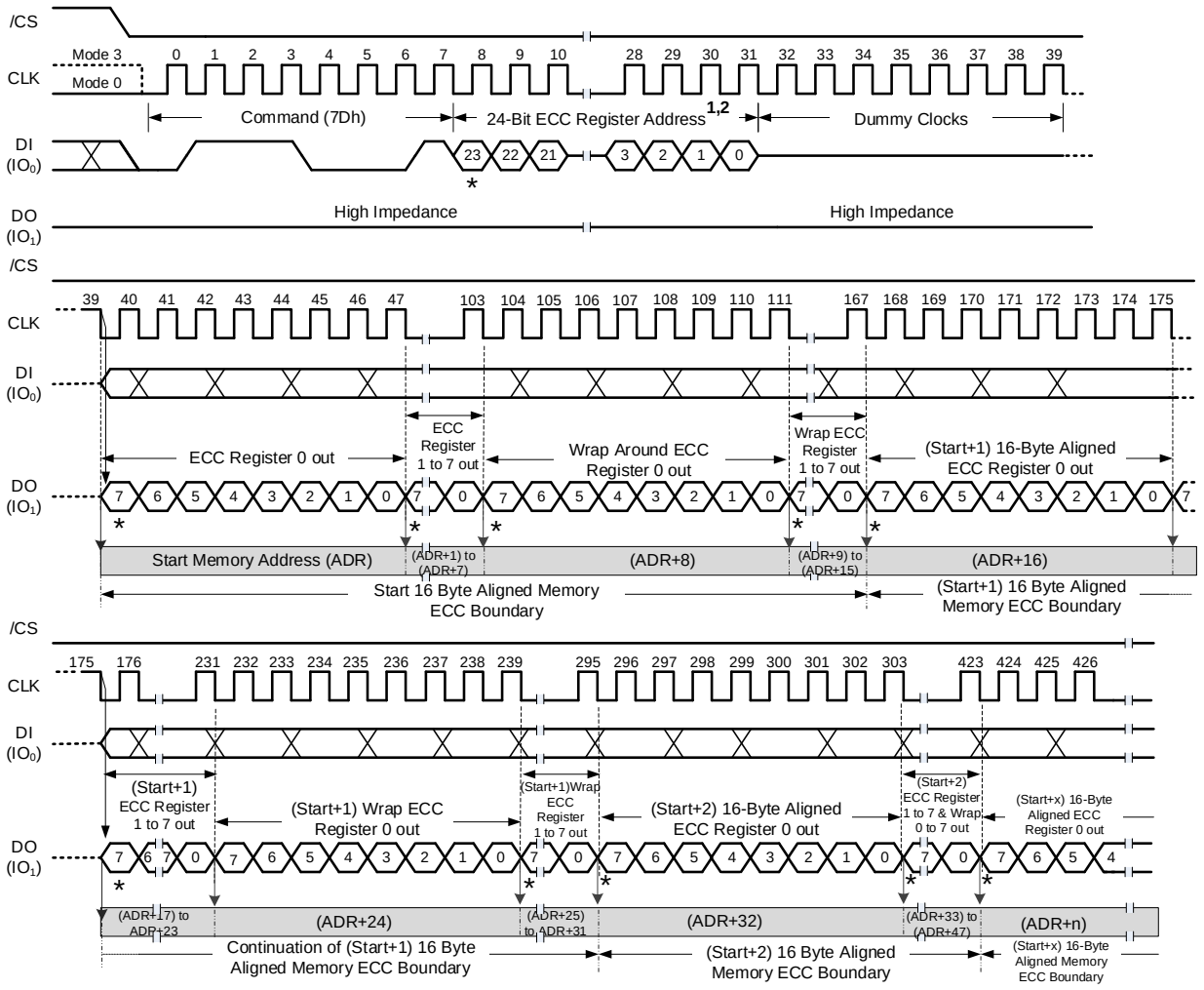
The Read Advanced ECC Register command (7Dh) is used to read the 8-byte Advanced ECC Register in standard SDR or ODDR mode. In standard SPI mode, the command is initiated by driving the /CS pin low and then shifting the command code “7Dh” followed by a 24-bit or a 32-bit ECC Register Address (ERA23-ERA0 or ERA31:ERA0) into the DI pin depending on the address mode setting. The code and the address bits are latched on the rising edge of CLK. A dummy byte follows the address input, then the Advanced ECC register data output of the target ECC Register will be shifted out from the DO pin on the falling edge of CLK starting with the most significant bit (MSB) first. The ECC status of the start of the linked 16-byte aligned memory address is also checked. The ECC address and the linked memory address are automatically incremented to the next higher ECC and then the linked memory address after each byte of data is shifted out. The ECC flag status of the entire memory can be accessed with a single command as long as the clock continues. The data output sequence is shown in the timing diagrams in Figure 16-4a and Figure 16-4b are as follows:

- The data output sequence shadows each of the aligned 16-byte ECC memory starting with the input ECC Register Address ERA[2:0] = 000b and MSBs ERA[23:3] or ERA[31:3], which is also the starting linked memory address.
- The first 16-byte data output is composed of two contiguous 8-byte Advanced ECC Register sequences, that provide ECC Flag Status (ECCOF, DEDF, and SECF) of the target ECC Register Address and the aligned 16-byte ECC memory; the captured addresses, counters, and valid captured address flags (SRA[25:4], SC[3:0], DRA[25:4], DC[3:00], SACVF, and DACVF) with the ECC event from the previously read memory operations. The captured ECC addresses, counters, and valid captured address flags are the same throughout the Advanced ECC Register data output sequence.
- The next 16-byte output sequence is the ECC Flag Status (ECCOF, DEDF, and SECF) of the next 16-byte aligned memory. The remaining register output of the captured ECC addresses, counters, and valid captured address flags (SRA[25:4], SC[3:0], DRA[25:4], DC[3:00]), SACVF, and DACVF) are recurrence of the previously captured ECC addresses, counters, and valid captured address flags output (from the previous 16-byte ECC addresses/counters/valid captures address flags value). The next series of 16-byte outputs are a similar type of data reflecting each successive 16-byte ECC memory alignment across the memory and the recurring ECC addresses, counters, and valid captured address flags.

The command is completed by driving the /CS high.

The Read Advanced ECC Register command sequence in ODDR mode is similar to the standard SDR sequence except that it uses IO[7:0] in the input and output sequences.

In ODDR mode, the Read Advanced ECC Register command (7Dh) is initiated by driving the /CS pin low and then shifting the command code “7Dh” followed by a 32-bit ECC Register Address (ERA31:ERA0) using the IO[7:0] pins depending on the address mode setting. The code is latched on the rising edge of the CLK pin, while the address bits are latched on the rising and falling edge of CLK. A 16-dummy clocks follow the address input, then the Advanced ECC register data of the target ECC Register Address location will be shifted out using the IO[7:0] pins on both the falling and rising edge of CLK starting with the most significant bit (MSB) first. The start of the linked aligned 16-byte memory address is also checked for ECC status. The ECC address as well as the linked memory address are automatically incremented to the next higher ECC address and the linked memory address after each byte of data is shifted out. The ECC flag of the entire memory can be accessed with a single command as long as the clock continues. The data output sequence is similar to the Read Advanced ECC Register (7Dh) SDR command. The command is completed by driving the /CS high. The Read Advanced ECC Register command sequences are shown in Figure 16-4a and 16-4b.



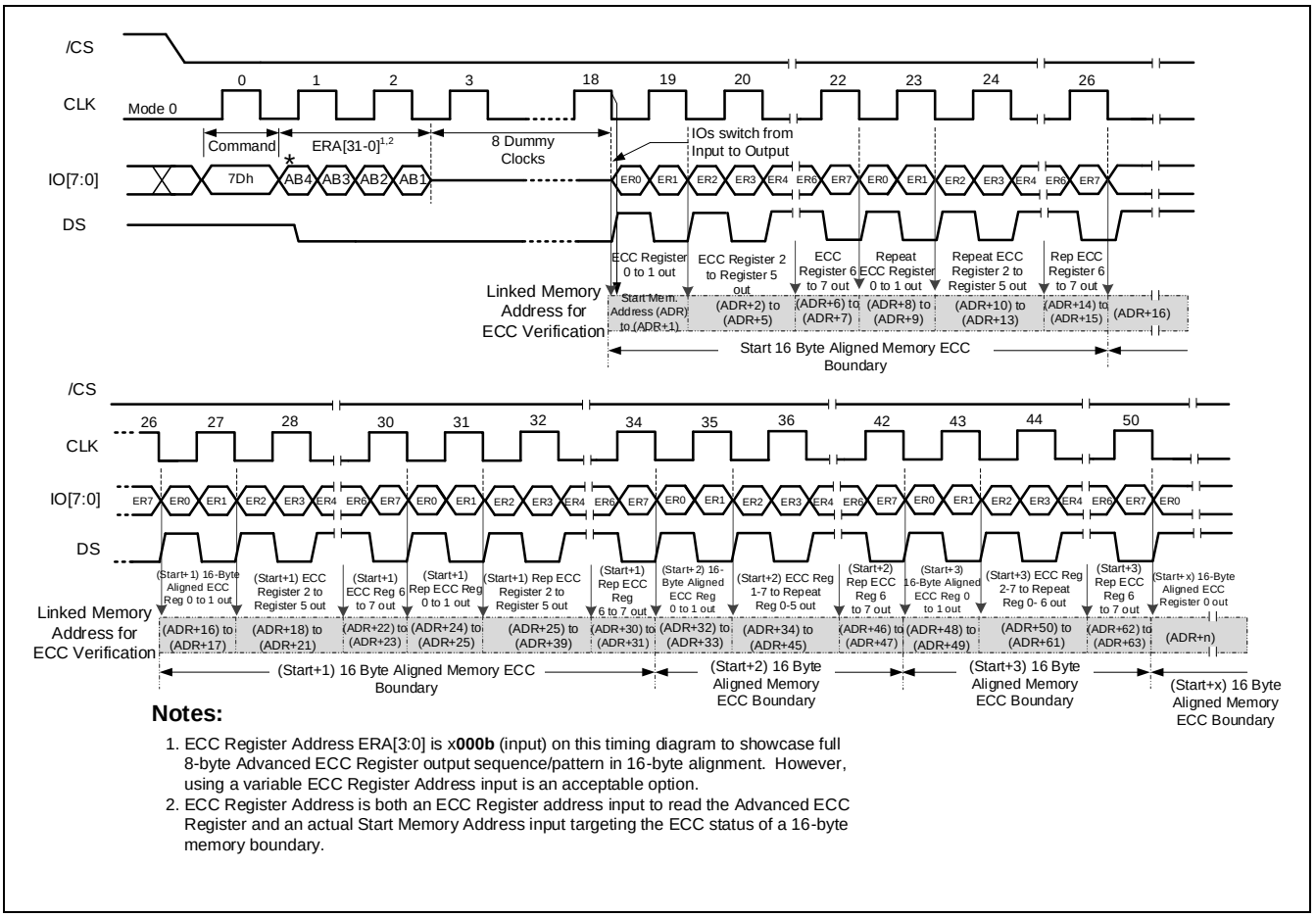
Notes:

* = MSB

1. ECC Register Address ERA[3:0] is x**000b** (input) on this timing diagram.
2. ECC Register Address is both an ECC Register address input to read the Advanced ECC Register and an actual Start Memory Address input targeting the ECC status of a 16-byte memory boundary.

Figure 16-4a. Read Advanced ECC Status Register Command (SDR Mode)

A 32-Bit Addressing is required when the device is operating in the 4-Byte Address Mode



Notes:

1. ECC Register Address ERA[3:0] is x**000b** (input) on this timing diagram to showcase full 8-byte Advanced ECC Register output sequence/pattern in 16-byte alignment. However, using a variable ECC Register Address input is an acceptable option.
2. ECC Register Address is both an ECC Register address input to read the Advanced ECC Register and an actual Start Memory Address input targeting the ECC status of a 16-byte memory boundary.

Figure 16-4b. Read Advanced ECC Status Register Command (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR Mode

9.13 Data Learning Pattern Commands

The 256-byte DLP Register is accessed by using the Data Learning Pattern (DLP) commands that include read, program, and erase sequences in both SDR and ODDR mode. The next sections detail the protocols for Read DLP, Program DLP, and Erase DLP commands.

9.13.1 (1-1-1) Read DLP (23h)

In SDR mode (1-1-1), the Read DLP (23h) command reads out the 256-byte DLP pattern on the DLP Register. It is initiated by driving the /CS pin low, by shifting in the command code '23h' and followed by either a 24-bit or 32-bit address (depending on Address Mode Configuration) using the IO0 pin on the rising edge of CLK. After the command and address, the target DLP Register address byte data is shifted out of the IO1 pin on the falling edge of CLK starting with the most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out with the corresponding clock edge. Once the byte address reaches the highest memory address, it will wrap-around back to DLP address xxxx00h/xxxxxx00h. Driving the /CS pin high, completes the command. Figure 17-1 illustrates the (1-1-1) Read DLP command in SDR mode sequence.

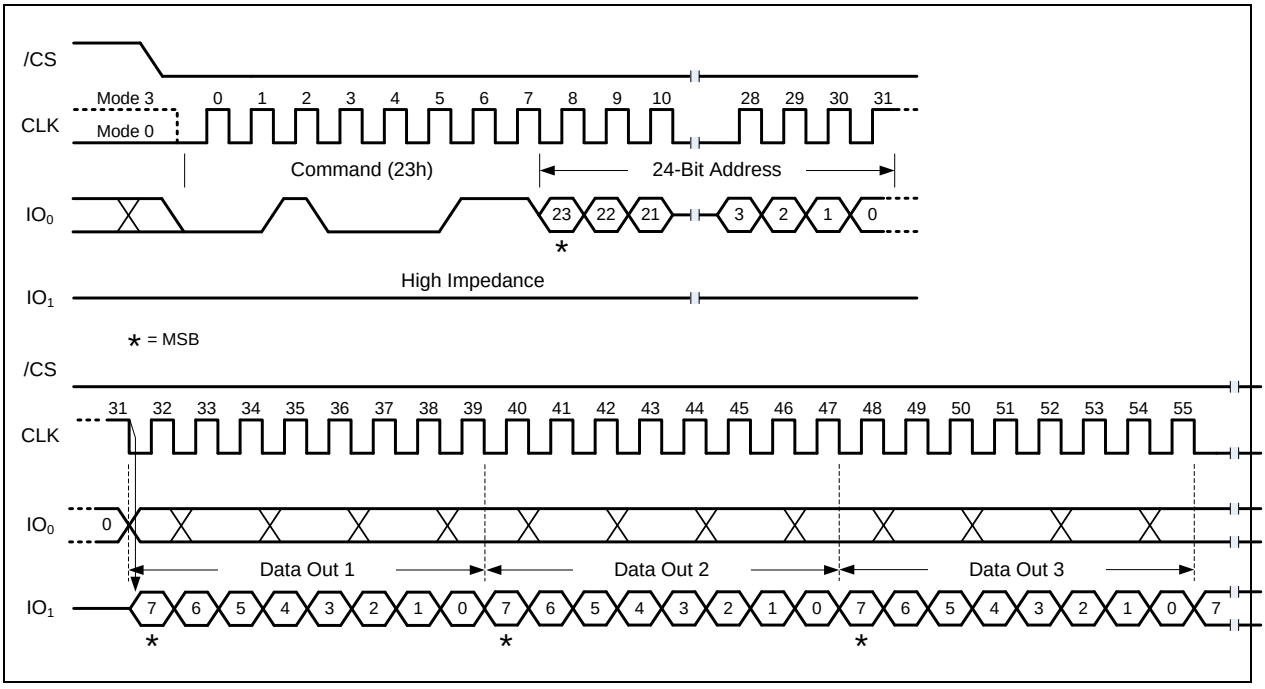


Figure 17-1. (1-1-1) Read DLP Command (1-1-1 SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.13.2 (1-1-8) Read DLP (8Ch)

In SDR mode (1-1-8), the Read DLP (8Ch) command is initiated by driving the /CS pin low, followed by shifting in command code '8Ch', followed by either a 24-bit or 32-bit address (depending on Address Mode Configuration) using the IO0 pin on the rising edge of CLK, and a required eight "dummy" clocks (default and programmable via NVCR-DC/ VCR-DC address 01h). After the input command, address and dummy cycles, the target DLP Register address byte data is shifted out of IO[7:0] pins on the falling edge of CLK. The byte address is automatically incremented to the next byte address after each byte of data is shifted out with the corresponding clock edge. Once the byte address reaches the highest memory address, it will wrap-around back to DLP address xxxx00h/xxxxxx00h. Driving the /CS pin high completes the command. Figure 17-2 illustrates the (1-1-8) Read DLP command in SDR mode sequence.

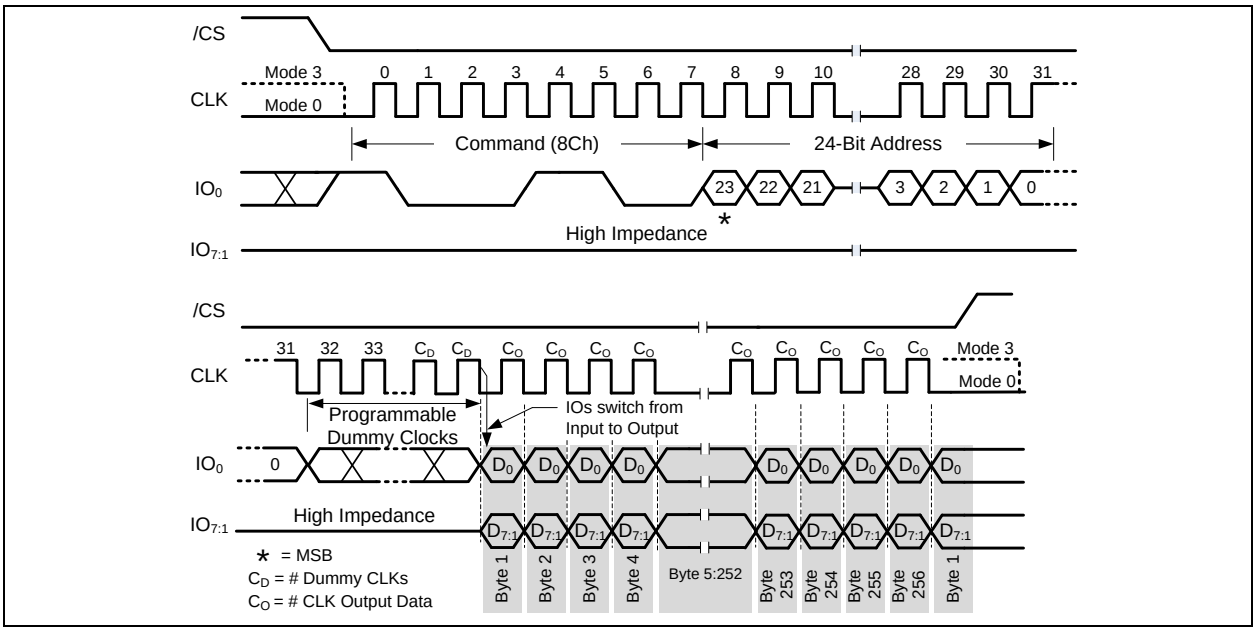


Figure 17-2. (1-1-8) Read DLP Command (1-1-8 SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.13.3 (1-1d-8d) and (8d-8d-8d) Read DLP (9Ch)

(1-1d-8d) Read DLP (9Ch) command is supported in SDR mode, while (8d-8d-8d) Read DLP (9Ch) command is supported in ODDR Mode.

In SDR mode (1-1d-8d), the Read DLP (9Ch) command is initiated by driving the /CS pin low, followed by shifting in command code '9Ch' using the IO0 pin on the rising edge of CLK, followed by either a 24-bit or 32-bit address (depending on Address Mode Configuration) using the IO0 pin on the rising and falling edge of CLK, and then followed by a required eight "dummy" clocks (default and programmable via NVCR-DC/ VCR-DC address 01h). **A[0] must be 0 in Read DLP commands. If A0≠0, wrong data will be read from Read DLP commands.** After the input command, address and dummy cycles, the target DLP Register address data is shifted out of the IO[7:0] pins on the falling and rising edge of CLK. The byte address is automatically incremented to the next byte address after each byte of data is shifted out with the corresponding clock edge. Once the byte address reaches the highest memory address, it will wrap-around back to DLP address xxxx00h/xxxxxx00h. Driving the /CS pin high completes the command. Figure 17-3a illustrates the (1-1d-8d) Read DLP command in SDR mode sequence.

In ODDR mode (8d-8d-8d), the Read DLP (9Ch) command is initiated by driving the /CS pin low and shifting the command code '9Ch' using the IO[7:0] pins on both the rising and falling edge of CLK. A 32-bit address is shifted using the IO[7:0] pins on both the rising and falling edge of CLK after the command. **A[0] must**

be 0 in ODDR Read DLP commands. If A0≠0, wrong data will be read from ODDR DLP Read commands. This is followed by 16 dummy CLK cycles (default/programmable) and IO[7:0] will transition from input to output on the falling edge of the last dummy clock cycle. Each data byte (output data) is shifted out on IO[7:0] on both falling and rising edge of CLK starting from the target address. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the highest memory address, it will wrap-around back to address xxxxxx00h. The command is completed by driving the /CS pin high. Figure 17-3b illustrates (8d-8d-8d) the Read DLP (9Ch) command.

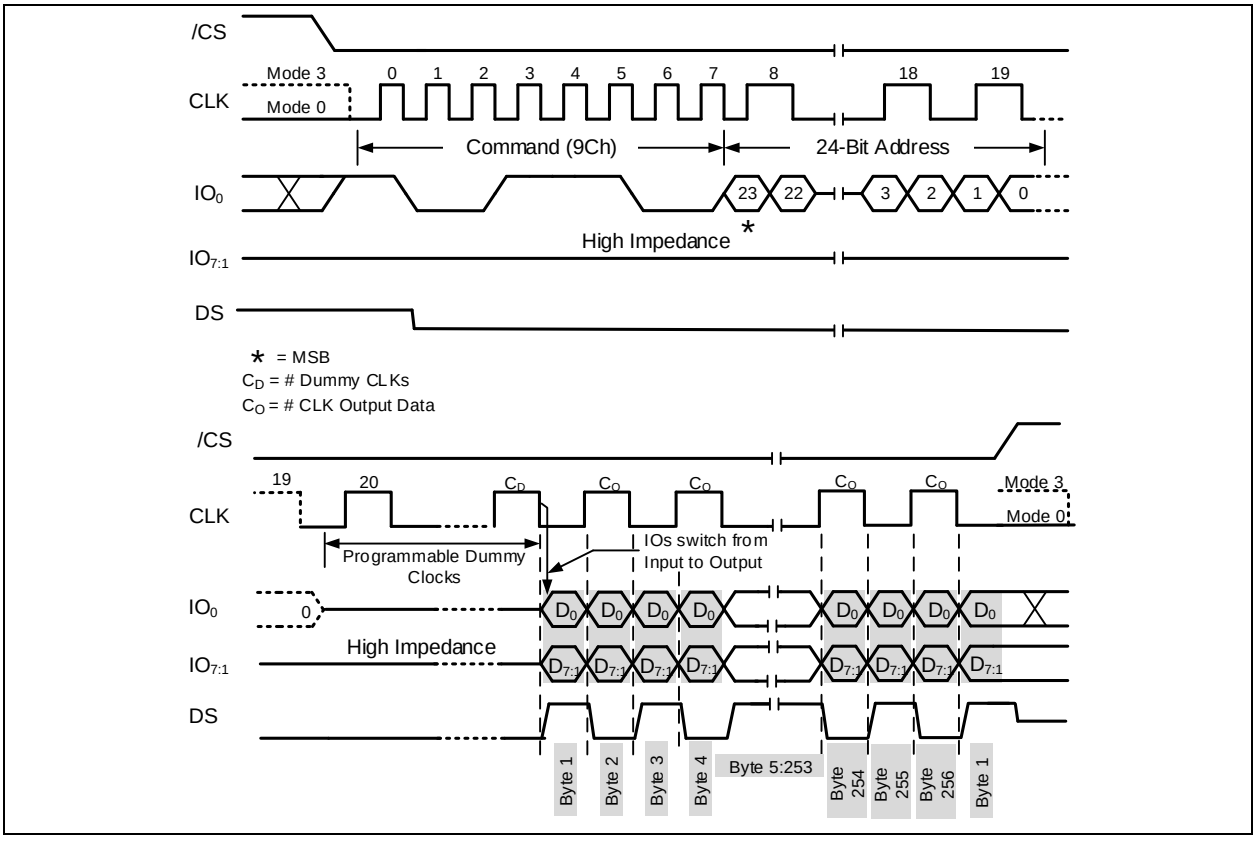


Figure 17-3a. (1-1d-8d) Read DLP Command (1-1d-8d SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

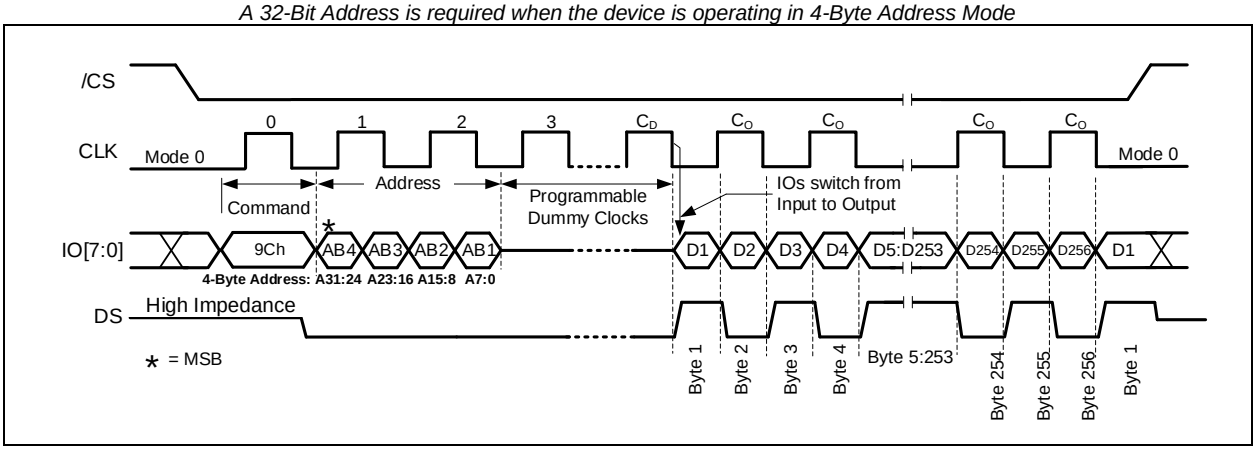


Figure 17-3b. (8d-8d-8d) Read DLP Command (ODDR Mode)

9.13.4 (1-1-1) Program DLP Register (40h)

The Program DLP Register (40h) command is similar to the Page Program (02h) command. It allows programming one byte up to 256 bytes of security register data at previously erased (FFh) memory locations. A Write Enable command must be executed before the device will accept a Program DLP Register Command (Status Register bit WEL= 1).

In SDR mode (1-1-1), the Program DLP Register command is entered by driving the /CS pin low, followed by shifting in command code '40h', a 24/32-bit DLP address and at least one byte of data using the IO0 pin on the rising edge of CLK. Driving the /CS pin high initiates programming the data range from the target address in the DLP Register. The /CS pin must be held low for the entire length of the command while data is being sent to the device. After the /CS pin is driven high, the self-timed Program DLP Register operation is performed for a duration of t_{PP} (See AC Characteristics). While the Program DLP Register cycle is in progress, the Read Status Register command may still be accessed for checking the BUSY bit. The BUSY bit is '1' during the program cycle and becomes '0' when the cycle is finished; and the device is ready to accept valid commands. After a Program DLP Register cycle is completed, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. Figure 17-4 illustrates the (1-1-1) Program DLP Register command sequence.

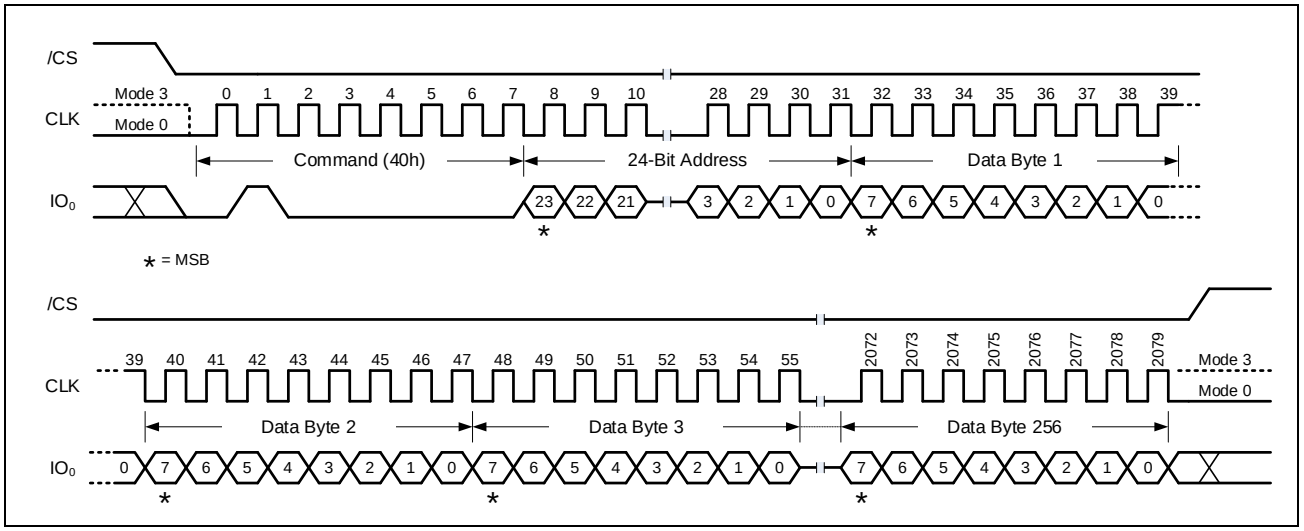


Figure 17-4. Program Tuning Data Pattern Command (1-1-1 SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.13.5 (1-1-8) and (8d-8d-8d) Program DLP Register (78h)

The (1-1-8) Program DLP Register (78h) command is similar to the (1-1-8) Page Program Octal Data (82h) command, and the (8d-8d-8d) Program DLP Register (78h) command is similar to program commands in ODDR mode. It is also performed in a similar setup and method as the (1-1-1) Program DLP Register (40h) command except it uses the IO[7:0] pins.

Once the device is write enabled (WEL bit =1), the command is initiated by the following sequence: drive the /CS pin low; shift-in the command code "78h" followed by a 24-bit or 32-bit address (depending on Address Mode Configuration) using the IO0 pin on the rising edge of CLK; transition to IO[7:0] and shift-in 1 to 256 bytes of data on the rising edge of CLK; and subsequently drive the /CS pin high to initiate the internal program cycle. The WEL bit is cleared to '0' after the self-timed Program DLP Register is completed. The (1-1-8) Program DLP Register command sequence is illustrated in Figure 17-5a.

Once the device is write enabled (WEL bit =1), the (8d-8d-8d) Program DLP Register command is initiated by the following sequence: drive the /CS pin low; shift-in the command code "78h" using the IO[7:0] pins on both the rising and falling edge of CLK; continue to shift-in a 32-bit address and 1 to 256 bytes data using the IO[7:0] pins on the rising edge of CLK; and subsequently drive /the CS pin high to initiate the internal program cycle. The WEL bit is cleared to '0' after the self-timed Program DLP Register is completed. The (8d-8d-8d) Program DLP Register command sequence is illustrated in Figure 17-5b.

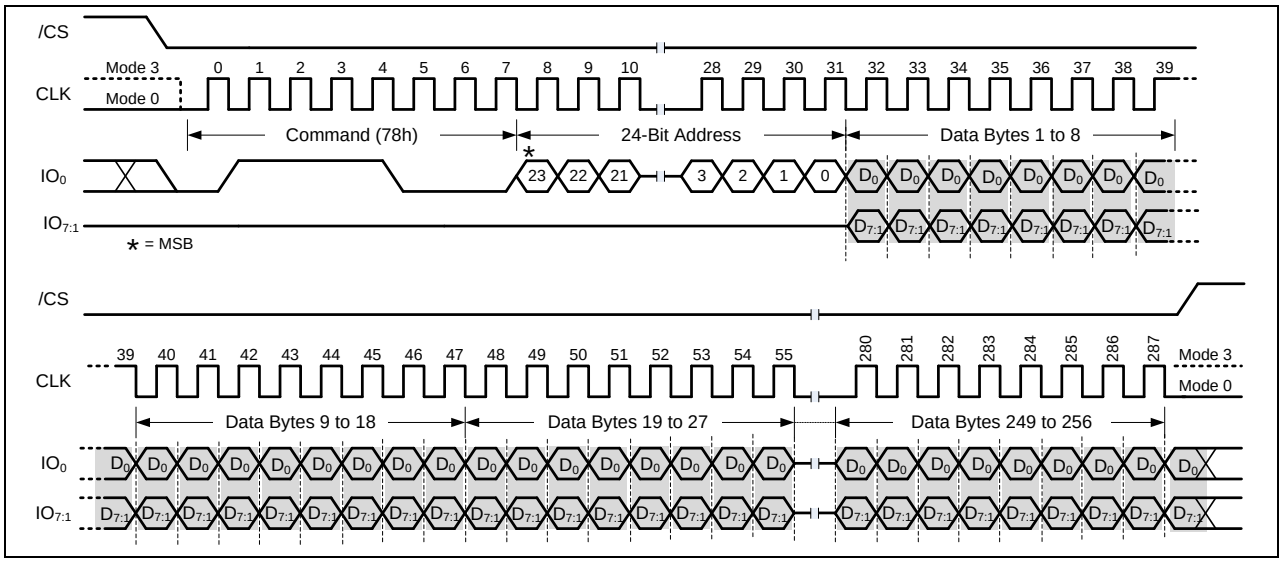


Figure 17-5a. (1-1-8) Program DLP Register Command (1-1-8 SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

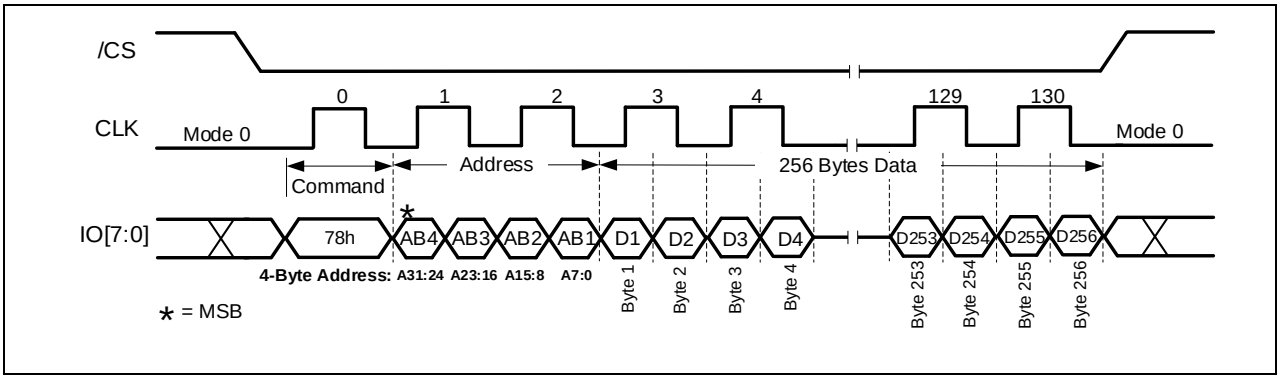


Figure 17-5b. (8d-8d-8d) Program DLP Register Command (8d-8d-8d ODDR Mode)

9.13.6 (1-1-0) or (8d-8d-0) Erase DLP Register (B8h)

The (1-1-0) and (8d-8d-0) Erase DLP Register (B8h) commands erase the 256-byte DLP Register to FFh (all 1s). The Erase DLP sequence is similar to the Sector Erase command. A Write Enable command must be executed before the device will accept the Erase Security Register Command (Status Register WEL bit must equal 1).

In SDR mode (1-1-0), the Erase DLP (B8h) sequence is entered by driving the /CS pin low, followed by shifting in the command code 'B8h' followed by either a 24/32-bit DLP address using the IO0 pin on the rising edge of CLK. Driving the /CS pin high initiates erasing the DLP Register. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the command will not be executed. After the /CS pin is driven high, the self-timed Erase DLP Register operation is performed for a time duration of t_{SE} (See AC Characteristics). While the Erase DLP Register cycle is in progress, the Read Status Register command may still be accessed for checking the BUSY bit. The BUSY bit is '1' during the erase cycle and becomes '0' when the cycle is finished; and the device is ready to accept valid commands. After the Erase DLP Register cycle is completed, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. Figure 17-6a illustrates the (1-1-0) Erase DLP Register (B8h) command sequence in SDR mode.

The method to implement the (8d-8d-0) Erase DLP Register command in ODDR mode is the same as described in the SDR mode section except for the use of 8-bit I/Os on both edges of the clock. In ODDR mode (8d-8d-0), the Erase DLP (B8h) command is initiated by the following sequence: drive the /CS pin low; shift-in the command code "B8h" using the IO[7:0] pins on both the rising and falling edge of CLK; continue to shift-in 32-bit address using the IO[7:0] pins on both edges of CLK; and subsequently drive the /CS pin high to initiate the internal DLP register erase cycle. The (8d-8d-0) Erase DLP Register command sequence in ODDR mode is illustrated in Figure 17-6b.

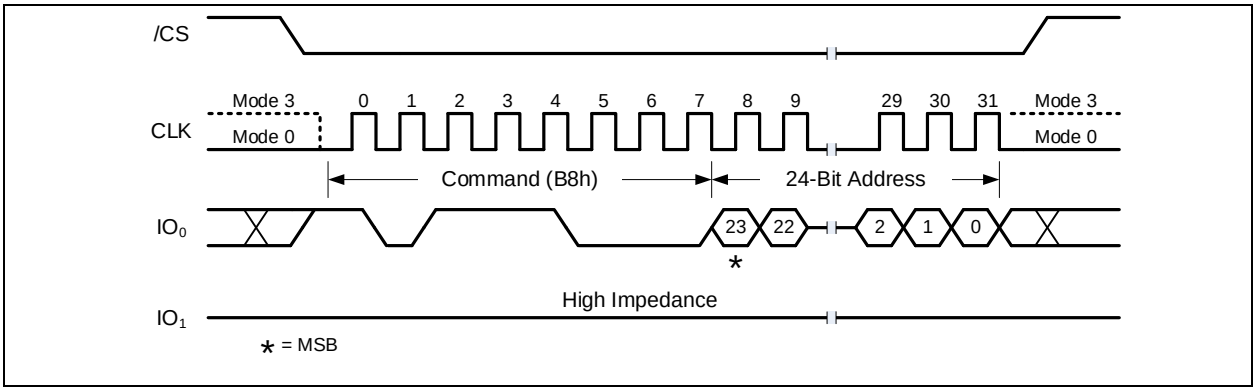


Figure 17-6a. (1-1-0) Erase DLP Register Command (1-1-0 SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

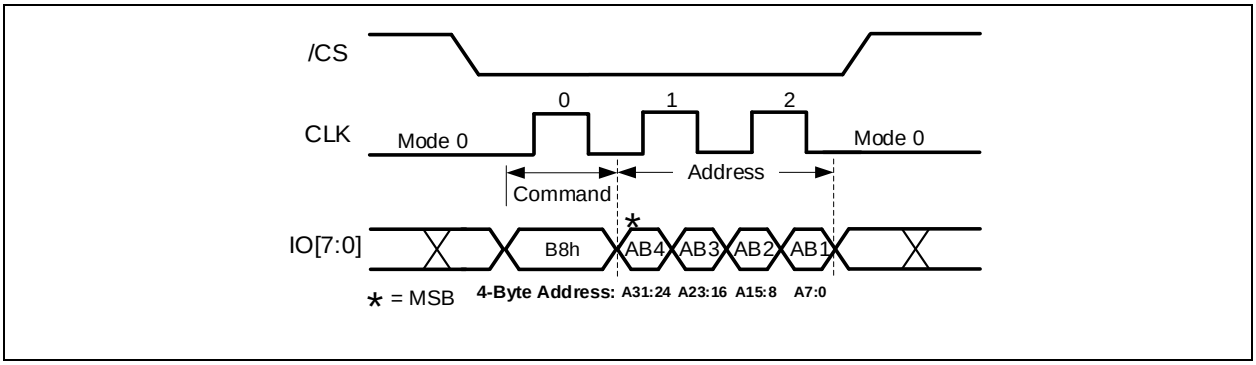


Figure 17-6b. (8d-8d-0) Erase DLP Register Command (8d-8d-0 ODDR Mode)

9.14 Data Integrity Check (Cyclic Redundancy Check at Rest and in Transit)

The W35T51NW supports the Cyclic Redundancy Check (CRC) feature at rest and in transit. The CRC command is used to detect abnormal changes to programmed data during programming or after a period of time to check data integrity. Once the CRC is initiated, it will calculate a current 8-byte CRC value and compare it to the 8-byte CRC value used in the CRC command 8-byte CRC value input sequence. The Flag Register Bit 4 (PF) indicates whether the CRC operation passed (PF=0) or failed (PF=1). If the CRC operation fails, proper corrective action can be taken by either verifying with a normal read operation and/or performing erase/re-programming of the memory array.

See Section 6.9 Cyclic Redundancy Check (CRC) for details.

9.14.1 CRC-At-Rest

9.14.1.1 CRC-At-Rest Full Memory (9Bh)

The CRC-At-Rest Full Memory command calculates the 8-byte CRC code of the full range of memory, stores it in the CRC Register, and compares it to the actual 8-byte CRC input value used in the CRC command sequence. The command is supported in both SDR and ODDR modes.

In SDR mode, the CRC-At-Rest command is initiated by the following sequence: drive the /CS pin low; shift-in the command code '9Bh', sub-command code '27h', the Full Memory value 'FFh' data, and the 8-byte CRC value input to be compared with the calculated value (with 1st Byte CRC value first); and subsequently driving the /CS pin high to initiate the internal CRC calculation and compare it to the CRC input value. The CRC-At-Rest Full Memory sequence is illustrated in Figure 18-1a.

In ODDR mode, the CRC command sequence is similar to the command in SDR mode except for the IO mode configuration and latch in sequence. ODDR CRC command sequence is initiated by the following sequence: drive the /CS pin low; shift-in command code '9Bh' using the IO[7:0] on both the rising and falling edge of CLK; continue to shift-in the sub-command code '27h' using the IO[7:0] on the rising edge of CLK followed by the Full Memory range value using the IO[7:0] pins on the falling edge of CLK; next shift in the 8-byte CRC value input to be compared to the calculated value (with 1st Byte CRC value first); and subsequently drive the /CS pin high to initiate the internal CRC calculation and compare it to the CRC input value. The ODDR CRC-At-Rest Full Memory sequence is illustrated in Figure 18-1b.

During the internal CRC calculation, after the /CS pin is driven high, the self-timed CRC cycle will commence for a duration of tCRC (See AC Characteristics). While the CRC operation is in progress, the Read Status Register and Read Flag Register commands may still access the Status Register and Flag Register to check the BUSY bit and the Ready Flag bit status. When the BUSY bit is '1' during the CRC command cycle, the device is busy with internal CRC calculation. When the BUSY bit transitions from '1' to '0', the internal CRC calculation has completed, and the device is ready to accept other commands. Alternatively, the Ready Flag is '0' when busy and '1' when the internal CRC calculation has completed.

After the CRC-At-Rest command is completed, if the calculated CRC value matches the 8-byte CRC input used in the CRC command sequence, the Program Flag (PF) bit in the Flag Register is '0' (indicating Pass). If the calculated CRC value does not match the 8-byte CRC input, the Program Flag (PF) bit in the Flag Register is set to '1' (indicating an error/fail). It is recommended that proper corrective action be taken by either verifying with a normal read operation and/or performing erase/re-programming of the memory array if an error or failure occurred during CRC check.

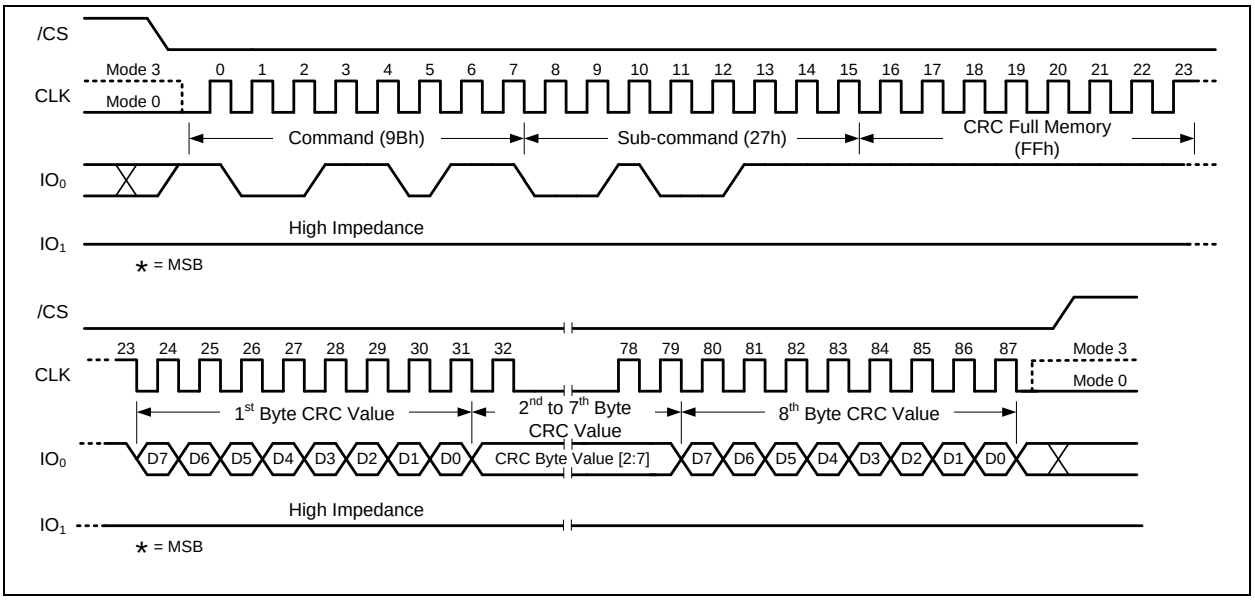


Figure 18-1a. CRC-At-Rest Full Memory Command Sequence (SDR Mode)

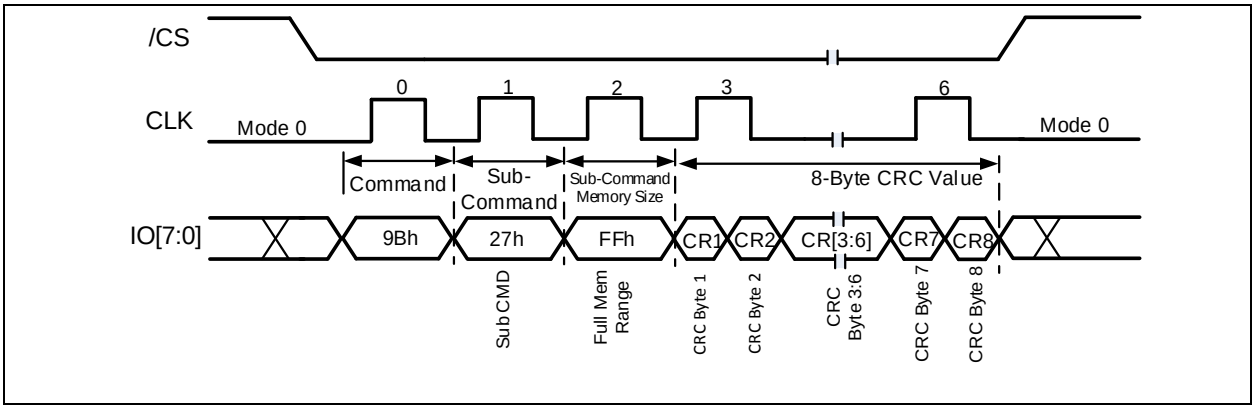


Figure 18-1b. ODDR CRC-At-Rest Full Memory Command Sequence (ODDR Mode)

9.14.1.2 CRC-At-Rest Memory Range (9Bh)

The CRC-At-Rest Memory Range command calculates the 8-byte CRC value of a memory range, stores it in the CRC Register and compares it with the actual 8-byte CRC value used in the CRC command sequence. The command is supported in both SDR and ODDR modes.

In SDR mode, the CRC-At-Rest command is initiated by the following sequence: drive the /CS pin low; shift-in the command code '9Bh', sub-command code '27h' using the IO0 pin on the rising edge of CLK, the Memory range value 'FEh', the 8-byte CRC value input to be compared to the calculated value (with 1st Byte CRC value first); 32-bit start address and the 32-bit stop address; and subsequently drive the /CS pin high to initiate the internal CRC calculation and compare it to the CRC input value. The CRC-At-Rest Memory Range sequence is illustrated in Figure 18-2a.

In ODDR mode, the CRC-At-Rest command sequence is similar to the command in SDR mode except for the IO mode configuration and latch in sequence. The ODDR CRC command sequence is initiated by the following sequence: drive the /CS pin low; shift-in command code '9Bh' using the IO[7:0] pins on both the rising and falling edge of CLK; continue to shift-in sub-command code '27h' followed by the Full Memory range value using the IO[7:0] pins on the falling edge of CLK; next shift in the 8-byte CRC value to be compared with the calculated value (with 1st Byte CRC value first); followed by shifting in the 32-bit start address and the 32-bit stop address using the IO[7:0] pins on both the rising and falling edges of CLK; and subsequently driving the /CS pin high to initiate the internal CRC calculation and compare it to the CRC input value. The ODDR CRC-At-Rest Memory Range sequence is illustrated in Figure 18-2b.

During the internal CRC calculation, after the /CS pin is driven high, the self-timed CRC cycle will commence for a duration of tCRC (See AC Characteristics). While the CRC operation is in progress, the Read Status Register and Read Flag Register commands may still access the Status Register and Flag Register to check the BUSY bit and Ready Flag bit status. When the BUSY bit is '1' during the CRC cycle, the device is busy with an internal CRC calculation. When the BUSY bit transitions from '1' to '0', the internal CRC calculation has completed, and the device is ready to accept other commands. Alternatively, the Ready Flag is '0' when busy and '1' when internal CRC operation has completed.

After the CRC-At-Rest command is completed, if the calculated CRC value matches the 8-byte CRC input used in the CRC command, the Program Flag (PF) bit in the Flag Register is '0' (indicating Pass). If the calculated CRC value does not match the 8-byte CRC input used in the CRC command, the Program Flag (PF) bit in the Flag Register is set to '1' (indicating an error/fail). It is recommended that proper corrective action be taken by either verifying with a normal read operation and/or performing erase/re-programming the memory array if an error or failure occurred during the CRC check.

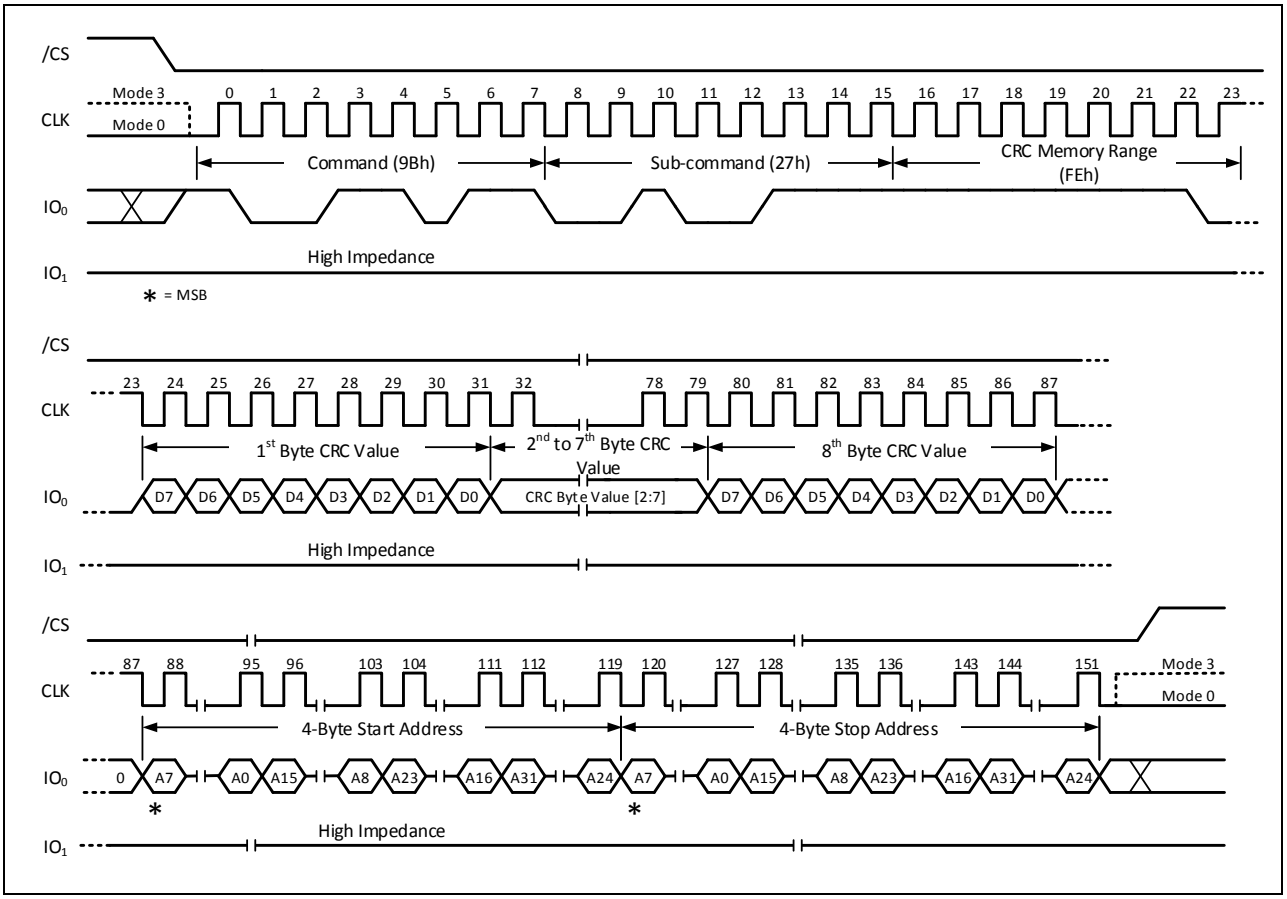


Figure 18-2a. CRC-At-Rest Memory Range Command Sequence (SDR Mode)

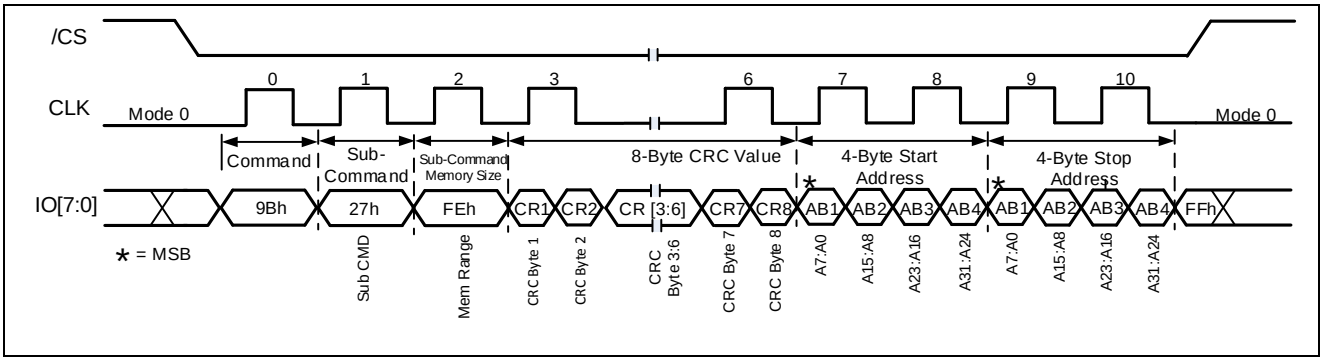


Figure 18-2b. ODDR CRC-At-Rest Memory Range Command Sequence (ODDR Mode)

9.14.1.3 Read 8-Byte CRC Code (1Bh)

The CRC-At-Rest Memory (9Bh) command has to be executed to calculate an internal 8-byte CRC code and store it in the CRC Register. The Read 8-Byte CRC Code (1Bh) command reads the 8-Byte CRC code stored in the CRC Register. In SDR mode, the Read 8-Byte CRC Code is initiated by driving the /CS pin low and then shifting the command code '1Bh' followed by either a 24-bit or 32-bit address input with value 000000h or 00000000h (depending on Address Mode Configuration) using the IO0 pin on the rising edge of CLK, and a required eight "dummy" clocks. After the command, address 000000h/00000000h input, and dummy cycles are received, the data byte of the 8-Byte CRC code will be shifted out on the IO1 pin on the falling edge of CLK with the most significant bit (MSB) first. The data output sequence is least significant CRC code byte first; and it is automatically incremented to the next CRC byte after each byte of data is shifted out. Once the CRC output data reaches the 8th byte CRC code, continuous clock input will output the 8-Byte CRC code repeatedly. The command is completed by driving the /CS pin high. Figure 18-3a illustrates the Read 8-Byte CRC Code command.

In ODDR mode, the ODDR Read 8-Byte CRC Code (1Bh) command is initiated by driving the /CS pin low and shifting the command code '1Bh using the IO[7:0] pins on both the rising and falling edge of CLK. A 32-bit address input with value 00000000h must be shifted using the IO[7:0] pins on both the rising and falling edge of CLK. This is followed by 16 dummy CLK cycles (default/programmable) and IO[7:0] will transition from input to output on the falling edge of the last dummy clock cycle. Each data byte (output data) is shifted out on IO[7:0] on both falling and rising edge of CLK starting from 1st byte CRC code. After every clock edge, the CRC code byte output is automatically incremented to the next CRC code byte until the 8th byte CRC code. Continuous clock input will repeatedly output the 8-byte CRC code pattern. The command is completed by driving the /CS pin high. Figure 18-3b illustrates the ODDR Read 64-Byte CRC Code command.

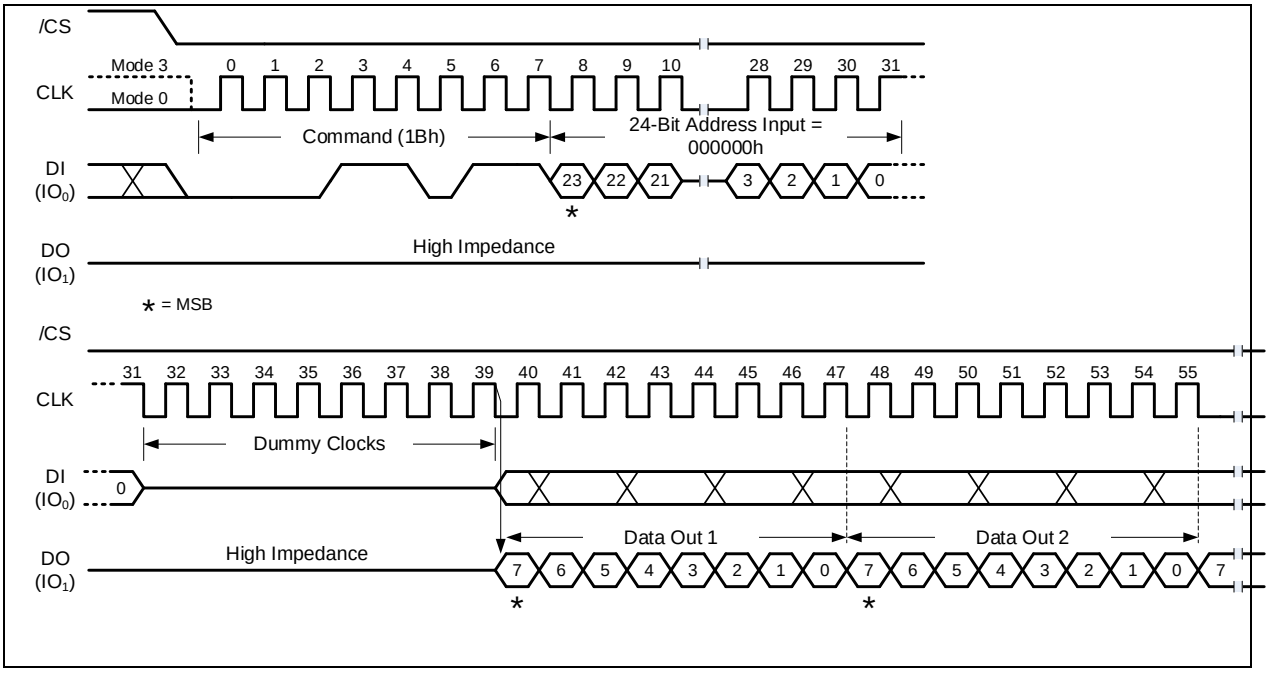


Figure 18-3a. Read 8-Byte CRC Code Command Sequence (1-1-1 SDR Mode)

A 32-Bit Address is required when the device is operating in 4-Byte Address Mode

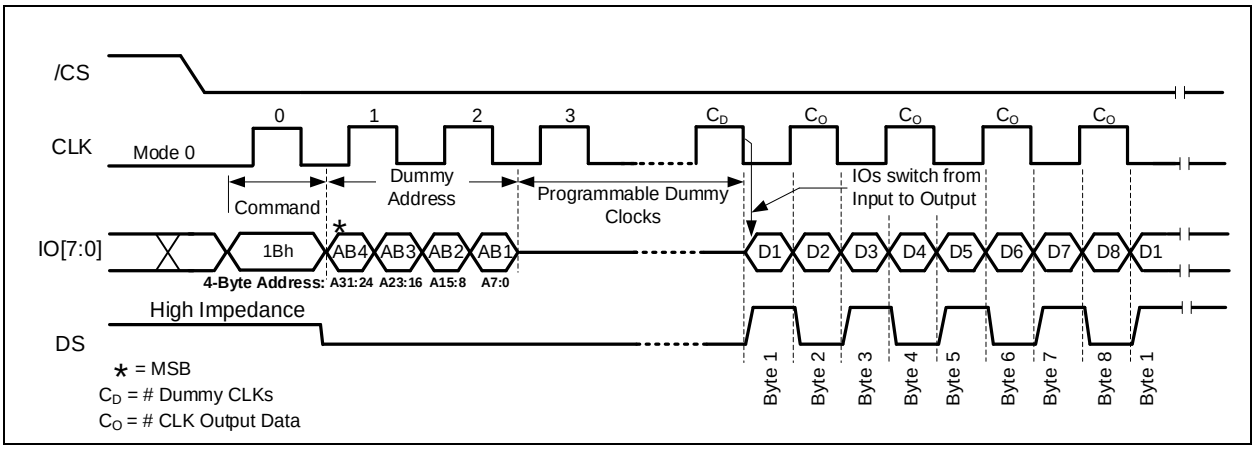


Figure 18-3b. ODDR Read 8-Byte CRC Code Command Sequence (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR Mode

9.14.2 CRC-In-Transit Mode

The CRC-In-Transit mode with parity check function is operated only in ODDR mode. It is not supported in SPI or Octal SPI mode. The CRC-In-Transit mode is entered by setting either the NVCR-CRC or VCR-CRC Register Address 04h to a 16/32/64/128 Byte Partition configuration.

A transmission error during the input sequence will set the CRCTF bit of the Flag Register (F3), and the initiated command will not be executed. If a data output CRC-In-Transit error occurs during the data output phase, the external interfacing controller has to manage the error event.

The set of supported CRC-In-Transit Commands and their protocols are covered in detail in the following sections.

9.14.2.1 8d-0-0 CRC-In-Transit Commands Protocol

The listed 8d-0-0 CRC-In-Transit Commands in the table below support the (Command Cycle – CRC Input Field) protocol illustrated in Figure 18-4a.

ODDR CRC-In-Transit Commands	Command Cycle Opcode	CRC-In-Transit Field On Input Supported (Command – CRC Input Field)
Enable Reset	**66h**	✓
Reset Device	**99h**	✓
Clear Flag Register	**50h**	✓
Write Enable	**06h**	✓
Enable Volatile Write Status Register	**08h**	✓
Write Disable	**04h**	✓
Enter 4-Byte Address Mode	**B7h**	✓
Exit 4-Byte Address Mode	**E9h**	✓
Chip Erase	**C7h/60h**	✓
Erase / Program Suspend	**75h**	✓
Erase / Program Resume	**7Ah**	✓
Power-down	**B9h**	✓
Exit Power-down	**ABh**	✓
Reset ECC Counters	**72h**	✓

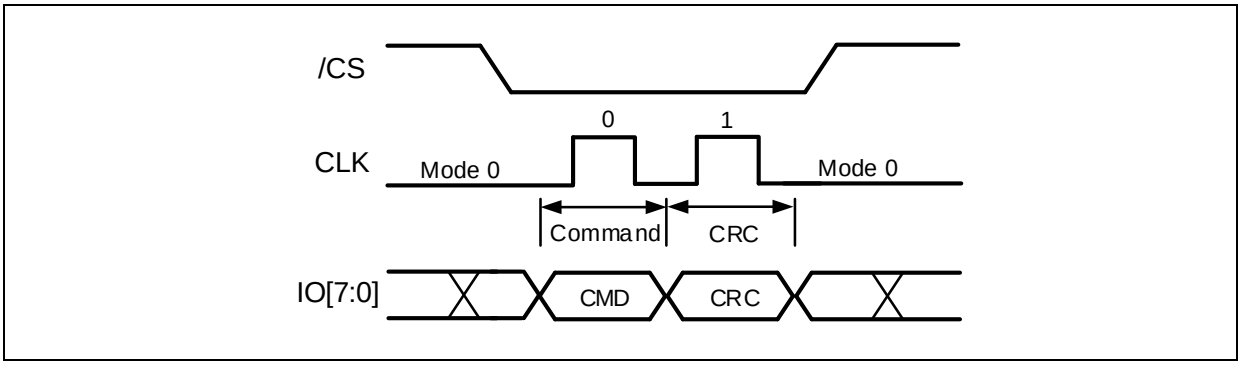


Figure 18-4a. 8d-0-0 CRC-In-Transit Command Protocol (ODDR Mode)

9.14.2.2 8d-0-8d Write Register CRC-In-Transit Commands Protocol

The listed 8d-0-8d Write Register CRC-In-Transit Commands in the table below support the (Command Cycle – Data Input Cycle – CRC Input Field) protocol illustrated in Figure 18-4b.

ODDR CRC-In-Transit Commands	Command Cycle Opcode	CRC-In-Transit Field on Input Supported (Command – Data – CRC Input Field)
Write Status Register	**01h**	✓
Write ECC Status Register	**56h**	✓

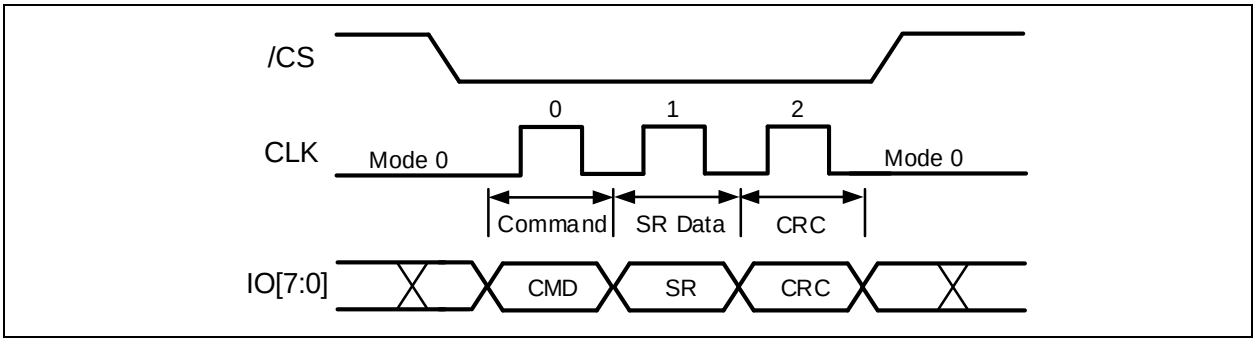


Figure 18-4b. 8d-0-8d Write Register CRC-In-Transit Command Protocol (ODDR Mode)

9.14.2.3 8d-8d-8d Write Register with Address CRC-In-Transit Commands Protocol

The listed 8d-8d-8d Write Register with Address CRC-In-Transit Commands in the table below support the (Command Cycle – Address Cycle – CRC Input Field – Data Input Cycle) protocol illustrated in Figure 18-4c.

ODDR CRC-In-Transit Commands	Command Cycle Opcode	CRC-In-Transit Field on Input Supported (Command – Address – CRC Input Field – Data Input)
Write Non-Volatile Configuration Register	**B1h**	✓
Write Volatile Configuration Register	**81h**	✓

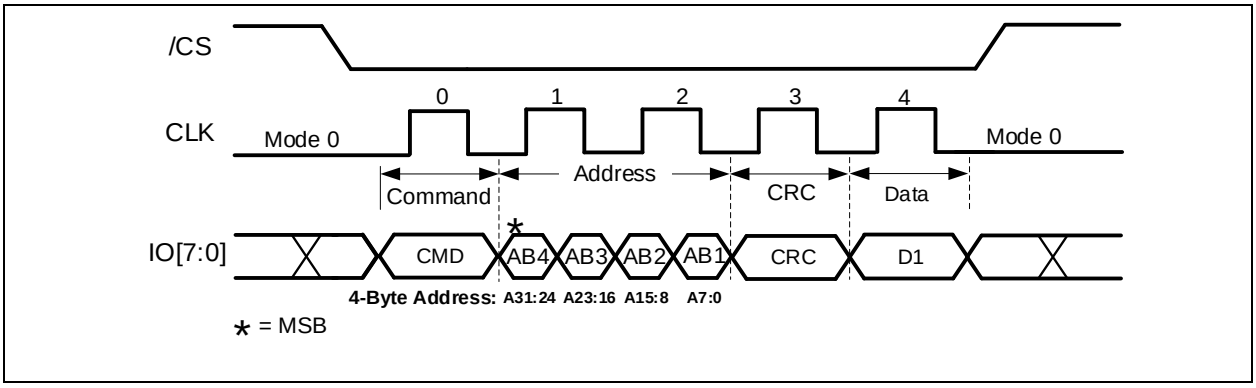


Figure 18-4c. 8d-8d-8d Write Register with Address CRC-In-Transit Command Protocol (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR Mode

9.14.2.4 8d-0-8d Read Register CRC-In-Transit Commands Protocol

The listed 8d-0-8d Read Register CRC-In-Transit Commands in the table below support the (Command Cycle – CRC Input Field – Dummy Cycle – Data Output Cycle) protocol illustrated in Figure 18-4d.

ODDR CRC-In-Transit Commands	Command Cycle Opcode	CRC-In-Transit Field on Input Supported (Command – CRC Input Field – Dummy)	CRC-In-Transit Field on Output Supported
Read Status Register	**05h**	✓	×
Read Flag Register	**70h**	✓	×
Read ECC Status Register	**25h**	✓	×

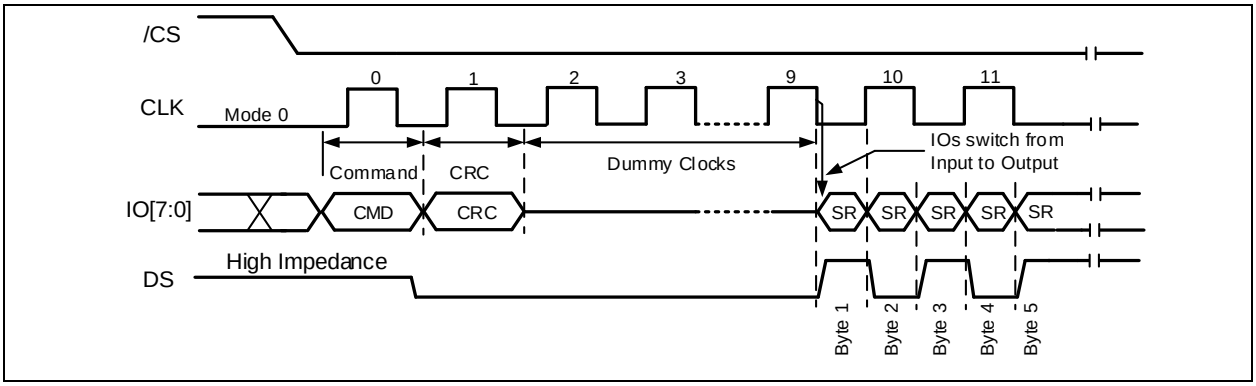


Figure 18-4d. 8d-0-8d Read Register CRC-In-Transit Command Protocol (ODDR Mode)

9.14.2.5 8d-8d-8d Read Register with Address CRC-In-Transit Commands Protocol

The listed 8d-8d-8d Read Register with Address CRC-In-Transit Commands in the table below support the (Command Cycle – Address Cycle – CRC Input Field – Dummy Cycle – Data Output Cycle) protocol illustrated in Figure 18-4e.

ODDR CRC-In-Transit Commands	Command Cycle Opcode	CRC-In-Transit Field on Input Supported (Command – Address – CRC Input Field - Dummy)	CRC-In-Transit Field Output Supported
Read Non-Volatile Configuration Register	**B5h**	✓	×
Read Volatile Configuration Register	**85h**	✓	×
Read Advanced ECC Register	**7Dh**	✓	×

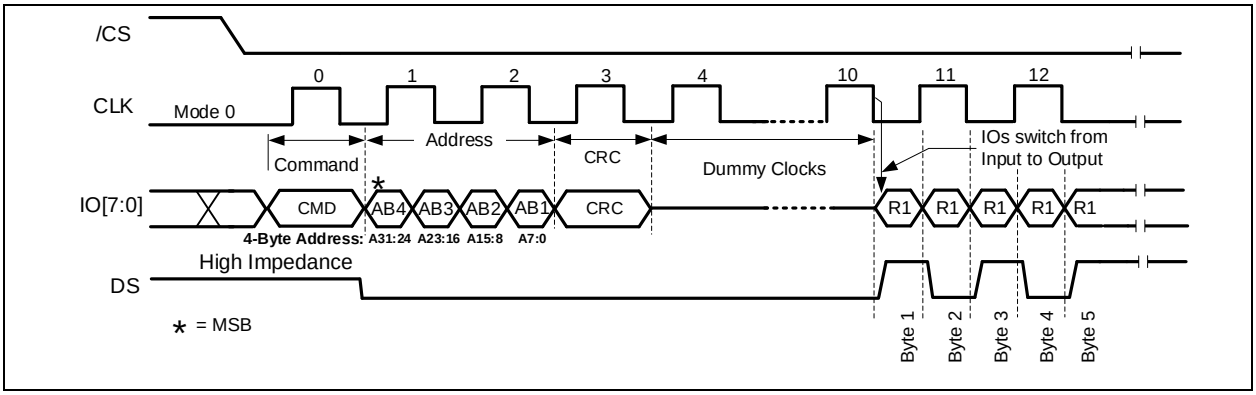


Figure 18-4e. 8d-8d-8d Read Register with Address CRC-In-Transit Command Protocol (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR Mode

9.14.2.6 8d-0-8d Read ID CRC-In-Transit Commands Protocol

The listed 8d-0-8d Read ID CRC-In-Transit Commands in the table below support the (Command Cycle – CRC Input Field – Dummy Cycle – 16/32/64/128 Byte Data Partition – CRC Output Field…) protocol. The data output sequence depends on the CRC-In-Transit partition setting (16/32/64/128 bytes) on either NVCR-CRC or VCR-CRC. The 8d-0-8d Read ID CRC-In-Transit protocol in Figure 18-4f shows the (Command Cycle – CRC Input Field – Dummy Cycle – 16/32/64/128-Byte Data Partition – CRC Output Field…) protocol. As shown in the data partition, after the 6th data output byte sequence, data FFh will be the remaining data being shifted out until the end of the 16/32/64/128 Byte partition followed by the CRC Output Field.

ODDR CRC-In-Transit Commands	Command Cycle Opcode	CRC-In-Transit Field on Input Supported (Command – CRC Input Field – Dummy)	CRC-In-Transit Field on Output Supported (Data Output – CRC Output Field)
Read JEDEC ID	**9Fh**	✓	✓
Read ID	**9Eh**	✓	✓

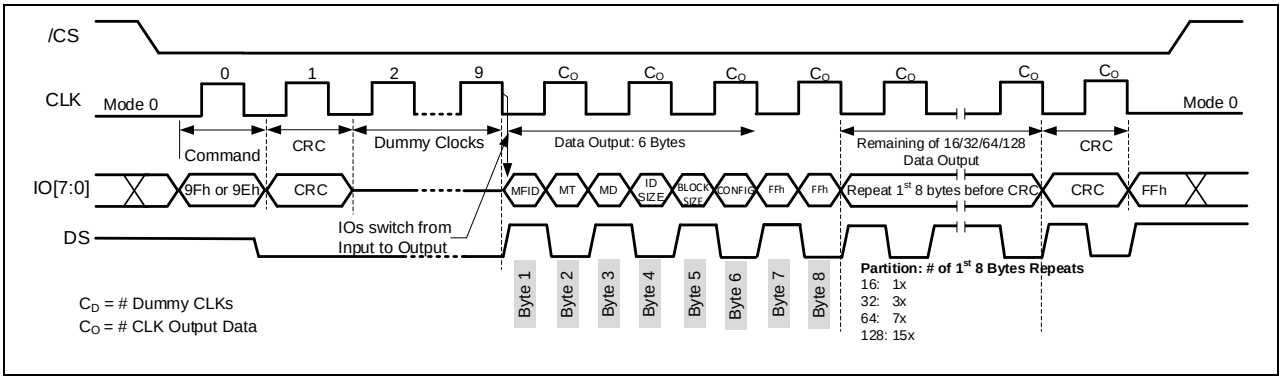


Figure 18-4f. 8d-8d-8d Read ID CRC-In-Transit Command Protocol (ODDR Mode)

9.14.2.7 8d-8d-8d Read SFDP CRC-In-Transit Commands Protocol

The 8d-0-8d Read SFDP CRC-In-Transit Commands in the table below support the (Command Cycle – Address Cycle – CRC Input Field – Dummy Cycle – 16/32/64/128 Byte Data Partition – CRC Output Field…) protocol shown in Figure 18-4g. The data output sequence will depend on the CRC-In-Transit partition setting (16/32/64/128 bytes) on either NVCR-CRC or VCR-CRC Register.

ODDR CRC-In-Transit Commands	Command Cycle Opcode	CRC-In-Transit Field on Input Supported (Command – Address -CRC Input Field– Dummy)	CRC-In-Transit Field on Output Supported
Read SFDP	**5Ah**	✓	✓

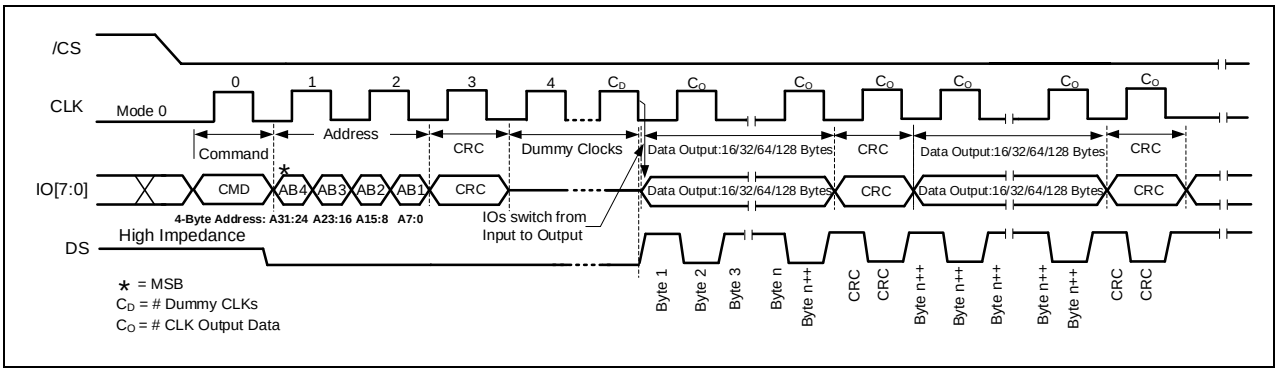


Figure 18-4g. CRC-In-Transit 8d-8d-8d Read SFDP Command Protocol (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR Mode

9.14.2.8 8d-8d-8d Program Memory, Program Security Registers, (8d-8d-8d) Program DLP Register CRC-In-Transit Commands Protocol

The listed 8d-8d-8d Program Memory (02h, 82h, C2h, 12h, 84h, and 8Eh), Program Security Register (42h), and (8d-8d-8d) Program DLP Register (78h) CRC-In-Transit Commands in the table below support the (Command Cycle – Address Cycle – CRC Input Field – 16/32/64/128 Byte Data Input Cycle – CRC Input Field…) protocol illustrated in Figure 18-4h.

The data input sequence depends on the CRC-In-Transit partition setting (16/32/64/128 bytes) on either NVCR-CRC or VCR-CRC Register. If the last portion of the input data size is less than the required partition, fill the remaining partition with FFh data to meet the required data input partition. The 2-Byte CRC Input Field has to be the last input cycle before /CS de-assertion for the internal programming to be initiated. The data input in the programming sequence in CRC-In-Transit mode will follow the page wrap feature of the standard Page Program protocol.

ODDR CRC-In-Transit Commands	Command Cycle Opcode	CRC-In-Transit Field on Input Supported (Command – Address -CRC Field)	CRC-In-Transit Field on Data Input Supported
Page Program	**02h**	✓	✓
Page Program Octal Data	**82h**	✓	✓
Page Program Octal Address/Data	**C2h**	✓	✓
Page Program with 4-Byte Address	**12h**	✓	✓
Page Program Octal Data with 4-Byte Address	**84h**	✓	✓
Page Program Octal Address/Data with 4-Byte Address	**8Eh**	✓	✓
Program Security Registers	**42h**	✓	✓
(8d-8d-8d) Program DLP Register	**78h**	✓	✓

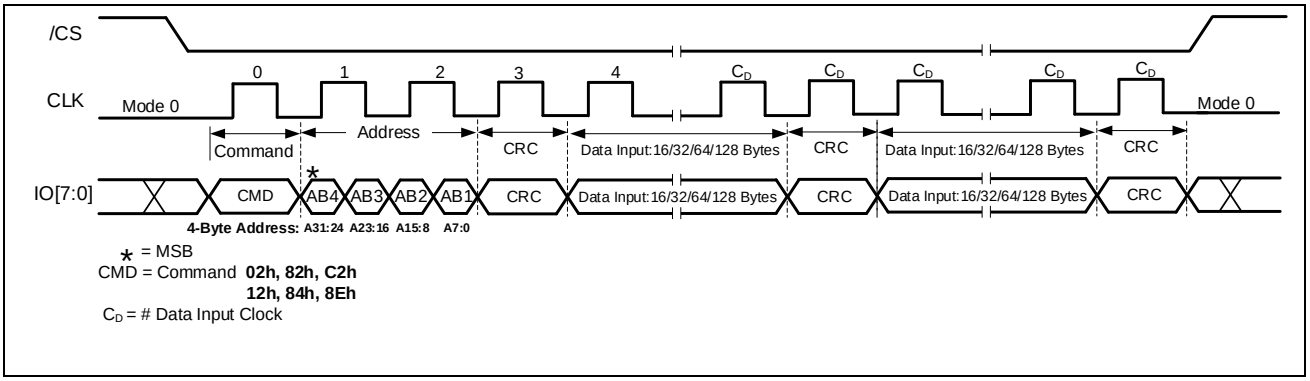


Figure 18-4h. CRC-In-Transit 8d-8d-8d Page Program Command Protocol (ODDR Mode)

A 32-Bit Address is required when the device is operating in ODDR Mode

9.14.2.9 8d-8d-8d CRC-At-Rest Commands Protocol

The CRC-At-Rest Memory is the same as the Page Program protocol except that it does not support the page wrap feature of the Page Program. Their Data Input Cycle + CRC Input Field will require an exact number of clock inputs depending on the selected data partition for the command to be executed. Figure 18-4i and 18-4j illustrate the CRC-In-Transit mode protocol for CRC-At-Rest Memory commands.

ODDR CRC-In-Transit Commands	Command Cycle Opcode	CRC-In-Transit Field on Input Supported (Command – Sub-Commands -CRC Field)	CRC-In-Transit Field on Data Input Supported
CRC-At-Rest Memory	**9Bh+27h**	✓	✓

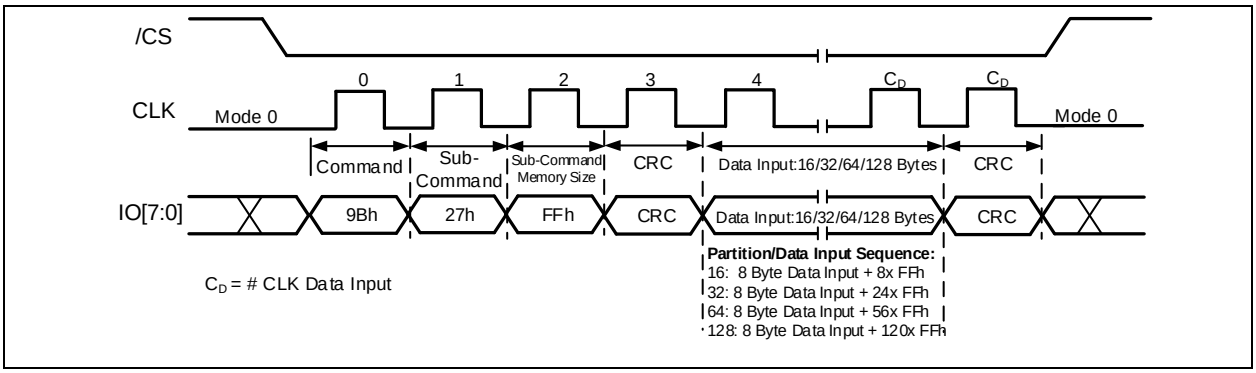


Figure 18-4i. CRC-In-Transit 8d-8d-8d CRC-At-Rest Full Memory Command Protocol (ODDR Mode)

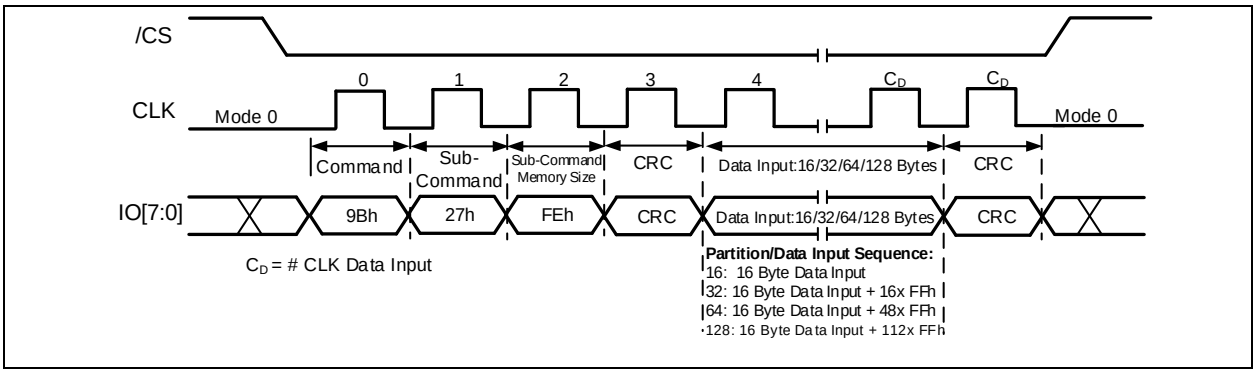


Figure 18-4j. CRC-In-Transit 8d-8d-8d CRC-At-Rest Memory Range Command Protocol (ODDR Mode)

9.14.2.10 8d-8d-0 Sector/Block Erase and Erase DLP Register CRC-In-Transit Commands Protocol

The listed 8d-8d-0 Sector/Block Erase (20h, 52h, D8h, DCh, 21h, and 5Ch), Erase Security Register (44h) and (8d-8d-0) Erase DLP Register (B8h) CRC-In-Transit Commands in the table below support the (Command Cycle – Address Cycle – CRC Input Field) protocol illustrated in Figure 18-4k.

ODDR CRC-In-Transit Commands	Command Cycle Opcode	CRC-In-Transit Field on Input Supported (Command – Address - CRC Input Field)
Sector Erase	**20h**	✓
32KB Block Erase	**52h**	✓
64KB Block Erase	**D8h**	✓
Sector Erase with 4-Byte Address	**DCh**	✓
32KB Block Erase with 4-Byte Address	**21h**	✓
64KB Block Erase with 4-Byte Address	**5Ch**	✓
Erase Security Registers	**44h**	✓
(8d-8d-0) Erase DLP Register	**B8h**	✓

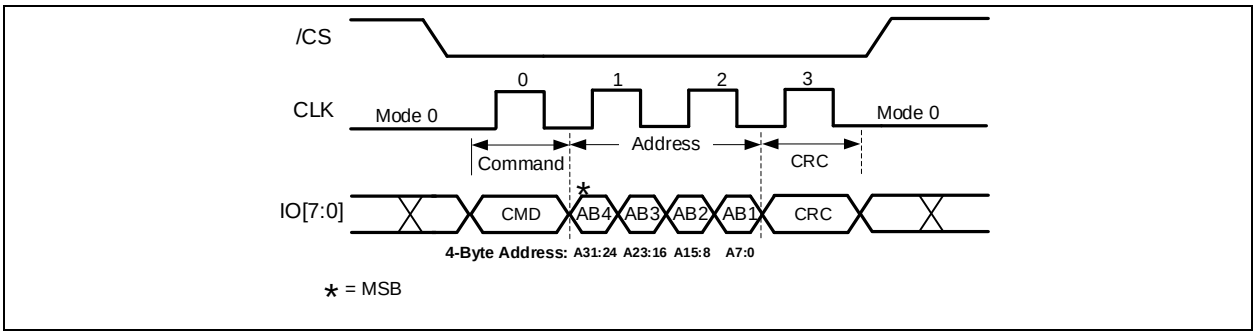


Figure 18-4k. CRC-In-Transit 8d-8d-0 Sector/Block Erase and Erase DLP Register Command Protocol (ODDR Mode)

9.14.2.11 8d-8d-8d Read Memory, Security Register, CRC, & DLP CRC-In-Transit Commands Protocol

The 8d-8d-8d Read Memory (0Bh, 8Bh, CBh, 9Dh, 0Ch, 7Ch, CCh, and FDh) and (8d-8d-8d) Read DLP (9Ch) CRC-In-Transit Commands in the table below support the (Command Cycle – Address Cycle – CRC Input Field – Dummy Cycle – 16/32/64/128 Byte Data Partition – CRC Output Field…) protocol shown in Figure 18-4l. The data output sequence depends on the CRC-In-Transit partition setting (16/32/64/128 bytes) on either NVCR-CRC or VCR-CRC Register.

The CRC-in-Transit Read Unique ID (4Bh) and Read 8-Byte CRC Code (1Bh) will have repeated (wrap-around) data output, wrap 16-byte for Unique ID and wrap 8-Byte CRC code value for CRC Code in 16/32/64/128 Byte data output partition followed by the CRC Output Field.

ODDR CRC-In-Transit Commands	Command Cycle Opcode	CRC-In-Transit Field on Input Supported (Command – Address-CRC Field-Dummy)	CRC-In-Transit Field on Output Supported
Fast Read	**0Bh**	✓	✓
Fast Read Octal-Output	**8Bh**	✓	✓
Fast Read Octal-I/O	**CBh**	✓	✓
Fast Read DDR Single-Address-Input and Octal-Output	**9Dh**	✓	✓
Fast Read with 4-Byte Address	**0Ch**	✓	✓
Fast Read Octal-Output with 4-Byte Address	**7Ch**	✓	✓
Fast Read Octal-I/O with 4-Byte Address	**CCh**	✓	✓
Fast Read DDR Octal I/O with 4-Byte Address	**FDh**	✓	✓
Read Register	**4Bh**	✓	✓
Read 8-Byte CRC code	**1Bh**	✓	✓
(8d-8d-8d) Read DLP	**9Ch**	✓	✓
Read Security Registers	**48h**	✓	✓

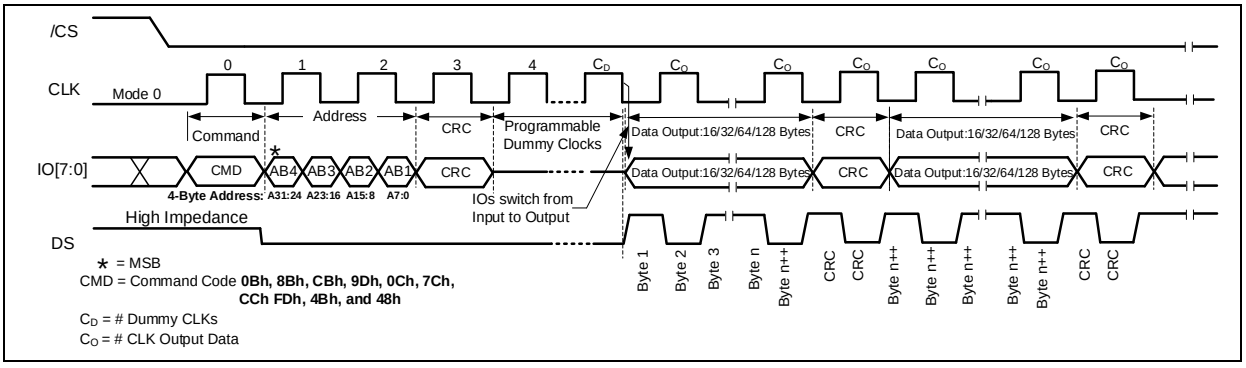


Figure 18-4l. 8d-8d-8d Read Memory CRC-In-Transit Command Protocol (ODDR Mode)

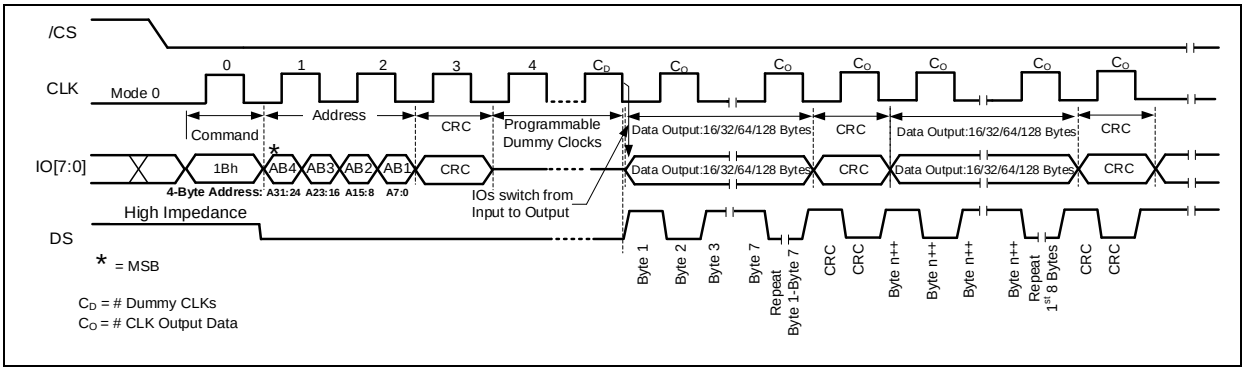


Figure 18-4m. 8d-8d-8d CRC-In-Transit Read 8-Byte CRC code Command Protocol (ODDR Mode)

9.14.2.12 8d-8d-8d / 0-8d-8d XIP Read Memory CRC-In-Transit Commands Protocol

The 8d-8d-8d XIP Read Memory (0Bh, 8Bh, CBh, 9Dh, 0Ch, 7Ch, CCh, and FDh) with XIP Entry (XIP Mode Bit – XMb bit) CRC-In-Transit Commands in the table below support the (Command Cycle – Address Cycle – CRC Input Field – Dummy Cycle with XIP Mode Bit (XMb bit) – 16/32/64/128 Byte Data Partition – CRC Output Field…) protocol shown on Figure 18-4m. The data output sequence depends on the CRC-In-Transit partition setting (16/32/64/128 bytes) on either NVCR-CRC or VCR-CRC Register.

In XIP Mode, the 0-8d-8d XIP Read Memory with XIP Mode Bit (XMb bit) sequence is shown in Figure 18-4n. In XIP mode sequence, the Command opcode is omitted and starts directly with Address Input to initiate the 0-8d-8d XIP Read Memory. It follows the Address Input – CRC Input Filed – Dummy Cycle with XIP Mode Bit (XMb bit) – 16/32/64/128 Byte Data Partition – CRC Output Field…) protocol.

ODDR CRC-In-Transit Commands	Command Cycle Opcode	CRC-In-Transit Field on Input Supported (Command – Address - CRC Field - Dummy)	CRC-In-Transit Field on Output Supported
Fast Read	**0Bh**	✓	✓
Fast Read Octal-Output	**8Bh**	✓	✓
Fast Read Octal-I/O	**CBh**	✓	✓
Fast Read DDR Single-Address-Input and Octal-Output	**9Dh**	✓	✓
Fast Read with 4-Byte Address	**0Ch**	✓	✓
Fast Read Octal-Output with 4-Byte Address	**7Ch**	✓	✓
Fast Read Octal-I/O with 4-Byte Address	**CCh**	✓	✓
Fast Read DDR Octal I/O with 4-Byte Address	**FDh**	✓	✓

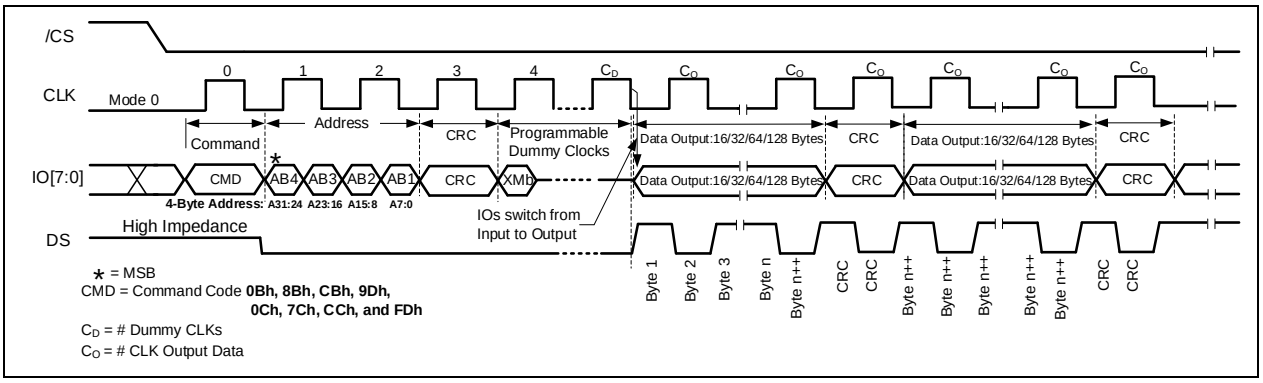


Figure 18-4n. 8d-8d-8d Read Memory with XIP Entry CRC-In-Transit Command Protocol (ODDR Mode)

ODDR XIP Mode CRC-In-Transit Protocol	Command Cycle Opcode	CRC-In-Transit Field on Input Supported (Address - CRC Input Field - Dummy)	CRC-In-Transit Field on Output Supported
0-8d-8d XIP Read Memory	**N/A**	✓	✓

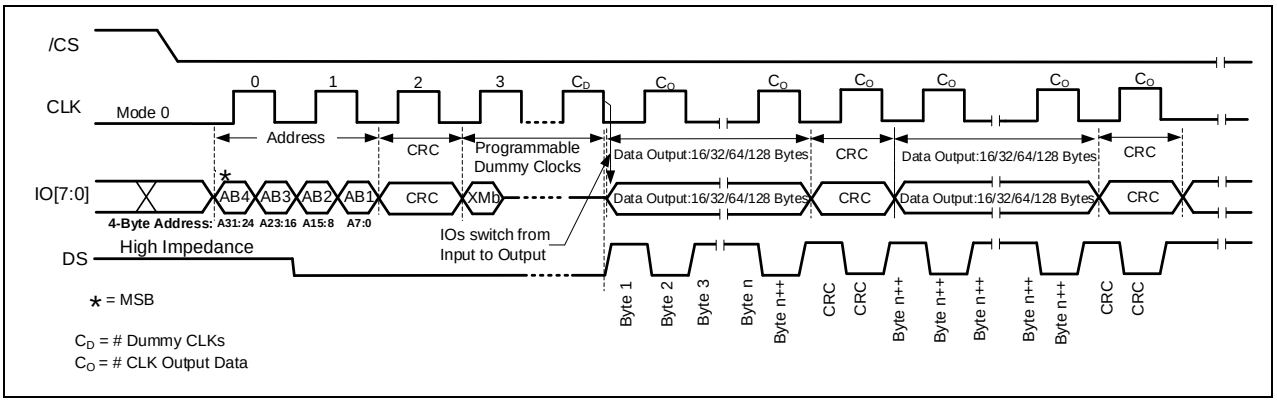


Figure 18-4o. 0-8d-8d XIP Read Memory CRC-In-Transit Command Protocol (ODDR Mode)

10. ELECTRICAL CHARACTERISTICS

10.1 Absolute Maximum Ratings (1)

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to +2.4	V
Voltage Applied to Any Pin	VIO	Respect to Ground	–0.6 to VCC+0.6	V
Transient Voltage on Any Pin	VIOT	<20nS Transient Respect to Ground	–2.0V to VCC+2.0V	V
Storage Temperature	TSTG		–65 to +150	°C
Lead Temperature	TLEAD		See Note (2)	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(3)	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

10.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC	**TFBGA PACKAGE:** F_{SDR} = 166 MHz, F_{DDR}= 200 MHz f_R = 54 MHz	1.65	2.0	V
Ambient Temperature, Operating	TA	Industrial	-40	+85	°C
		Industrial Plus	-40	+105	

10.3 Power-up Power-down Timing and Requirements

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	t_{VSL}[1]	10		µs
Time Delay Before Write Command	t_{PUW}[1]	5		ms
Write Inhibit Threshold Voltage	V_{WI}[1]	1.0	1.4	V
The minimum duration for ensuring initialization will occur	t_{PWD}[1]	100		µs
VCC voltage needed to below VPWD for ensuring initialization will occur	V_{PWD}[1]		0.8	V

Notes:

1. These parameters are characterized only.

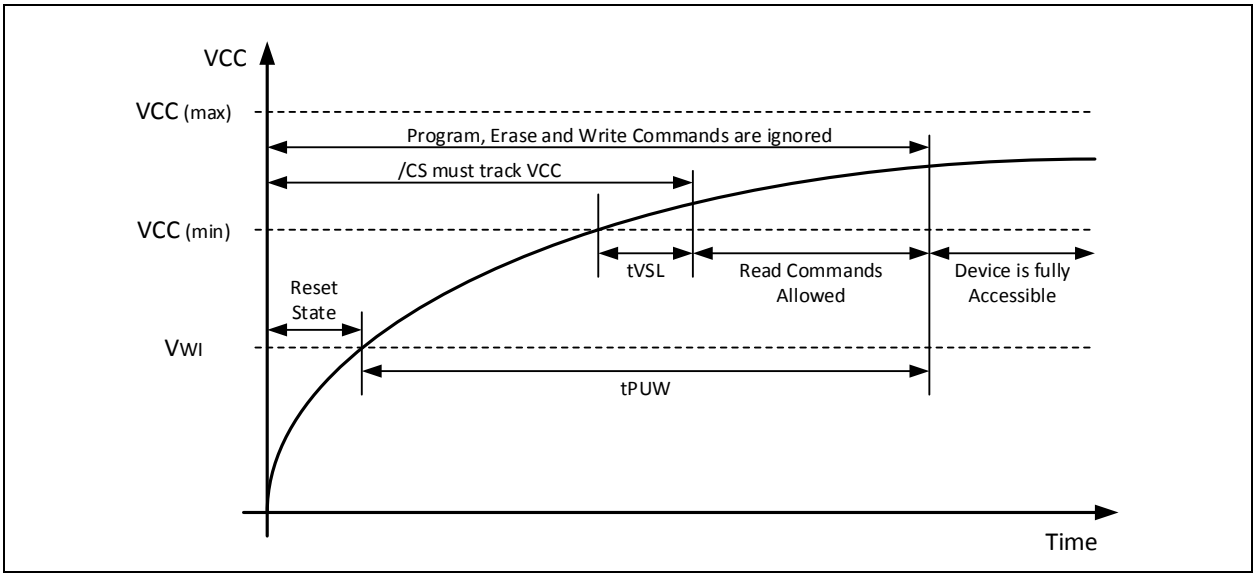


Figure 19-1. Power-up Timing and Voltage Levels

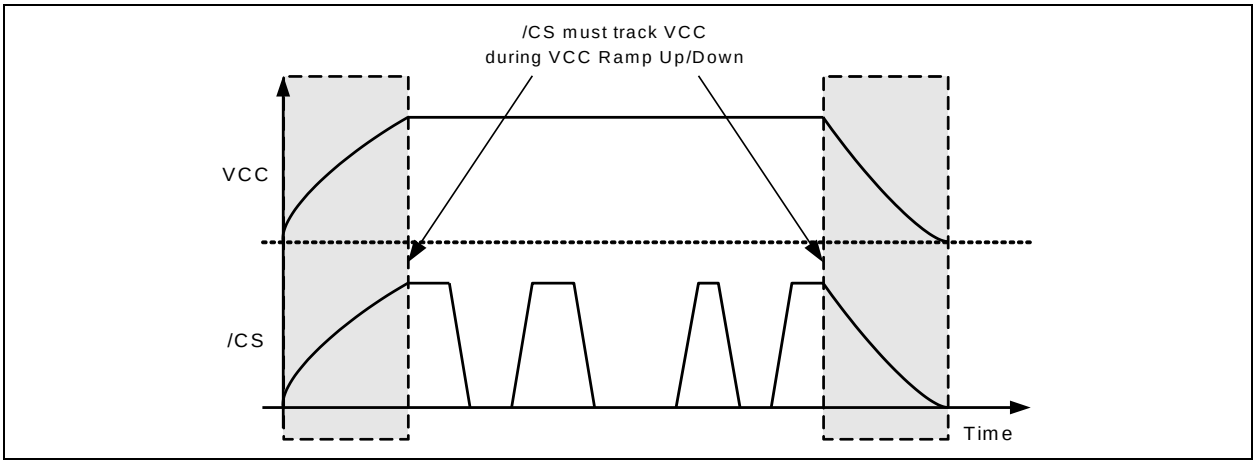
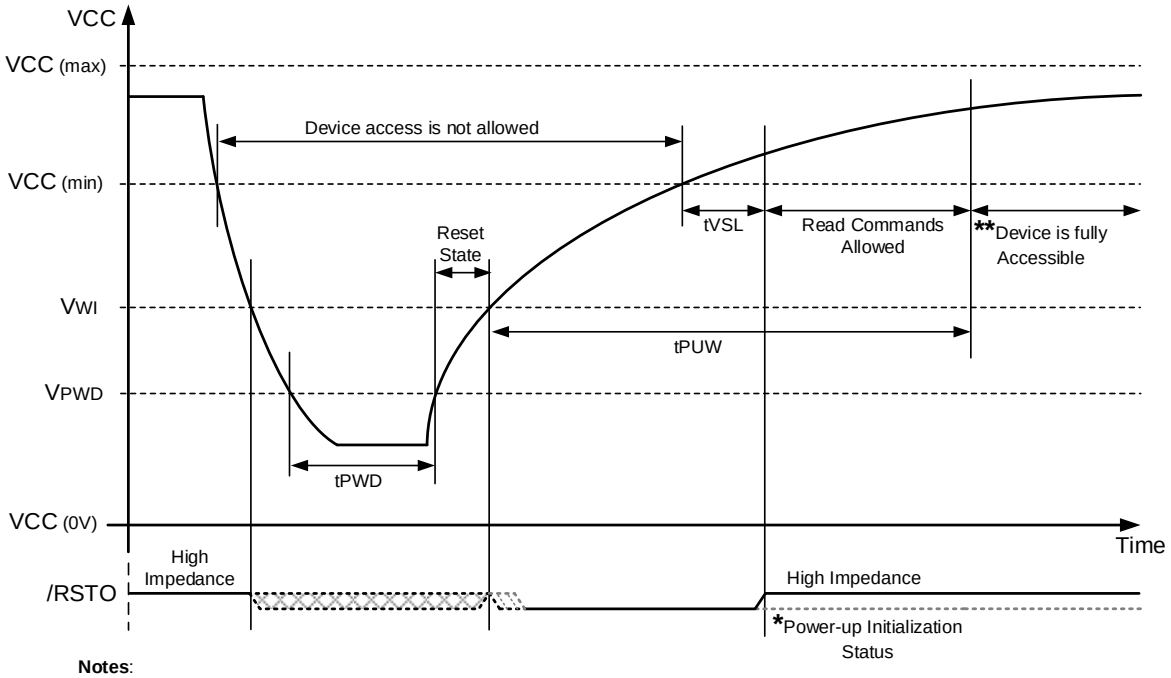


Figure 19-2. Power-up, Power-Down Requirement

10.3.1 Power Cycle Requirement

During a power off and on cycle, the device internal power-on-reset voltage threshold will not be triggered until Vcc drops down to VPWD. The Vcc level has to remain below VPWD for tPWD time before Vcc ramps up again to properly initialize the device during power-on-reset. For stable power up, it is recommended that the IOs trail Vcc or drive low during the power cycle sequence.



Notes:

* Power-up Initialization Status:
  - A hardware /RSTO pin transition from low to high impedance signals a successful power on reset.
  - A hardware /RSTO pin staying low after a power-up sequence signals a power-up initialization failure. Depending on the type of power-up initialization failure, device may not respond to valid commands or operate normally. The Status Register BUSY bit is set to '1', Status Register WEL bit is '0', and Flag Register READY Flag (RF) is cleared to '0' after a power-up failure event. A Software Reset, Hardware Reset, or JEDEC Hardware Reset will only reset (clear) the /RSTO pin, BUSY bit, and READY Flag fail status and will not guarantee device normal operation. Please check Fail/ Safe Power-up detection sections for detailed operation.

** It is recommended to perform read, program, erase, and write commands after Vcc ramps and a stable (normal) operating voltage is reached.

Figure 19-3. Power Cycle Requirement

10.4 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	I_{CC1}	/CS = VCC, VIN = VSS or VCC (85^0 C)		15	200	µA
		/CS = VCC, VIN = VSS or VCC (105^0 C)			300	
Power-down Current	I_{CC2}	/CS = VCC, VIN = VSS or VCC (85^0 C)		1	30	µA
		/CS = VCC, VIN = VSS or VCC (105^0 C)			80	
Read Data Current SPI 54MHz(1)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		15	20	mA
Read Data Current SPI SDR 133MHz(1)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		20	30	mA
Read Data Current Octal SDR 166MHz(1)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		30	40	mA
Read Data Current Octal DDR 108MHz(1)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		30	40	mA
Read Data Current Octal DDR 200MHz(1)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		40	60	mA
Write Status Register Current	I_{CC4}	/CS = VCC		5	15	mA
Page Program Current	I_{CC5}	/CS = VCC		20	35	mA
Sector/Block Erase Current	I_{CC6}	/CS = VCC		20	35	mA
Chip Erase Current	I_{CC7}	/CS = VCC		20	35	mA
Input Low Voltage	V_{IL}		–0.3		VCC x 0.3	V
Input High Voltage	V_{IH}		VCC x 0.7		VCC + 0.3	V
Output Low Voltage	V_{OL}	I_{OL} = 100µA			VCC x 0.15	V
Output High Voltage	V_{OH}	I_{OH} = –100 µA	VCC x 0.85			V

Notes:

1. Checker Board Pattern.

10.5 IO Capacitance(1)

PARAMETER	SYMBOL	TEST CONDITION	SPEC(2)		UNIT
			MIN	MAX	
Input Output Capacitance IO[7:0], DS, RST#	$C_{IN/OUT}$	V_{OUT} = 0V		5	pF
Input Capacitance	C_{IN}	V_{IN} = 0V		3	pF
Input/Chip Select	C_{IN} //CS			4	pF

Notes:

1. Tested on sample basis and specified through design and characterization data: TA = 25° C, VCC = 1.8V, CLK = 54 MHz.
2. IO capacitance value for the BGA package.

10.6 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance(1)	C_L		12	pF
Input Rise and Fall Times	T_R, T_F		1.2	ns
Input Pulse Voltages	V_{IN}	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Notes:

1. Output Hi-Z is defined as the point where data out is no longer driven. Output drivers are configurable by NVCR-DS or VCR-DS Address 03h.

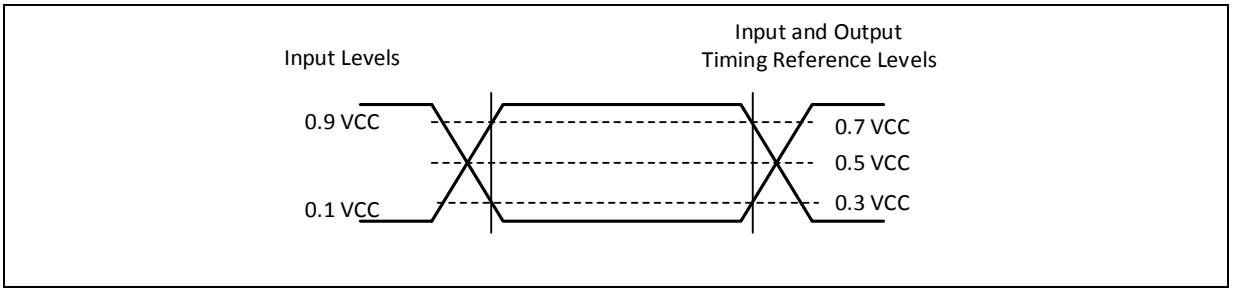


Figure 19-4. AC Measurement I/O Waveform

10.7 AC Electrical Characteristics (Operating Temperature –40°C to +85°C)

DESCRIPTION	SYMBOL	ALT	MODE	TFBGA-24 (1)		UNIT
				MIN	MAX	
Clock frequency except for Read	F_R	f_C	SDR	D.C.	166	MHz
			DDR	D.C.	200	
Clock frequency for Read (03h/13h/23h)	fR		SDR	D.C.	54	MHz
Clock High Time	t_{CLH}, t_{CLL}(2)	tCH	SDR/DDR	0.45*T	0.55*T	ns
Clock High, Low Time for Read Data (03h/13h/23h) command	t_{CRLH}, t_{CRLL}(2)	tCL	SDR/DDR	0.45*T	0.55*T	ns
Clock Rise Time peak to peak / Clock Fall Time peak to peak	t_{CLCH} / t_{CHCL}(3,4)		FR ≦100Mhz	0.6		V/ns
			FR ≦133Mhz	0.8		
			FR ≦166Mhz	1		
			FR >166Mhz	1.2		
/CS Active Setup Time respect to CLK	tSLCH	tCSS	SDR/DDR	2.5		ns
/CS Not Active Hold Time respect to CLK	tCHSL		SDR/DDR	2		ns
Data In Setup Time	tDVCH	tDSU	SDR/DDR	1.8/0.4		ns
	tDVCL		DDR	0.4		ns
Data In Hold Time	tCHDX	tDH	SDR/DDR	1.8/0.4		ns
	tCLDX		DDR	0.4		ns
/CS Active Hold Time respect to CLK	tCHSH		SDR	3		ns
			DDR	3		ns
	tCLSH		DDR	3		ns
/CS Not Active Setup Time respect to CLK	tSHCH		SDR	2		ns
			DDR	2		ns
/CS Deselect Time (for Array Read → Array Read)	tSHSL1	tCSH	SDR/DDR	10		ns
/CS Deselect Time (for Erase or Program → Read Status Registers) Volatile Status Register Write Time	tSHSL2	tCSH	SDR/DDR	30		ns

Continued – next page

AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	MODE	TFBGA-24 (1)		UNIT
				MIN	MAX	
Output Disable Time	t_{SHQZ}(3)	t_{DIS}	SDR/DDR		8	ns
Output Hold Skew	t_{QHS}		DDR		0.5	ns
DS to Output Data Valid	t_{DSSQ}		DDR		0.4	ns
DS low after falling edge of CLK	t_{DSL}(6)		DDR		10	ns
/CS not Active time to DS High-Z	t_{SHDSZ}		DDR		6	ns
Data Valid Window	t_{DVW}		DDR	1.3		ns
Clock Low to Output Valid under 12pF	t_{CLQV}(5)	t_V	SDR/DDR		5	ns
	t_{CHQV}(5)		DDR		5	ns
Output Hold Time	t_{CLQX}	t_{HO}	SDR/DDR	1.3		ns
	t_{CHQX}		DDR	1.3		ns
Write Protect Setup Time Before /CS Low	t_{WHSL}(3)		SDR/DDR	20		ns
Write Protect Hold Time After /CS High	t_{SHWL}(3)		SDR/DDR	100		ns
/CS High to Power-down Mode	t_{DP}(3)		SDR/DDR		3	µs
/CS High to Release Power-down to Standby Mode	t_{RES1}(3)		SDR/DDR		30	µs
CRC Check Time: main block	t_{CRC}		SDR/DDR		10	ms
CRC Check Time: full chip	t_{CRCF}		SDR/DDR		10	s

Notes:

1. AC measurements by TFBGA-24. 200 MHz maximum CLK frequency is maximum timing supported by the BGA package with the DS pin. Check the supported Clock Frequency with Required Dummy Clock Cycles Section based on the target address byte-alignment for more details.
2. Clock high + Clock low must be less than or equal to 1/fC.
3. Value guaranteed by design and/or characterization, not 100% tested in production.
4. Expressed as slew rate.
5. The specification only applies when DS is disabled.
6. DS will be pulled down at the first falling edge of clock after /CS low regardless of Mode0 or Mode3.

10.8 Register and Suspend Time Specification

PARAMETER	SYMBOL	SPEC			UNIT
		MIN	TYP	MAX	
Internal Erase to Suspend Time	t_{ESUS}			20	µs
Internal Program to Suspend Time	t_{PSUS}			20	µs
Erase Resume to Suspend Latency Time	t_{ERSL}	100			µs
Program Resume to Suspend Latency Time	t_{PRSL}	100			µs
Write Status Register Time	t_W		10	15	ms
Write Non-Volatile Register Time	t_{WNVCR}		10	15	ms
Page Program Time	t_{PP}[1]		0.2	1.5	ms
Sector Erase Time (4KB)	t_{SE}		50	200	ms
Block Erase Time (32KB)	t_{BE}[2]		150	800	ms
Block Erase Time (64KB)	t_{BE}[3]		180	2,000	ms
Chip Erase Time	t_{CE}		100	400	s

Notes:

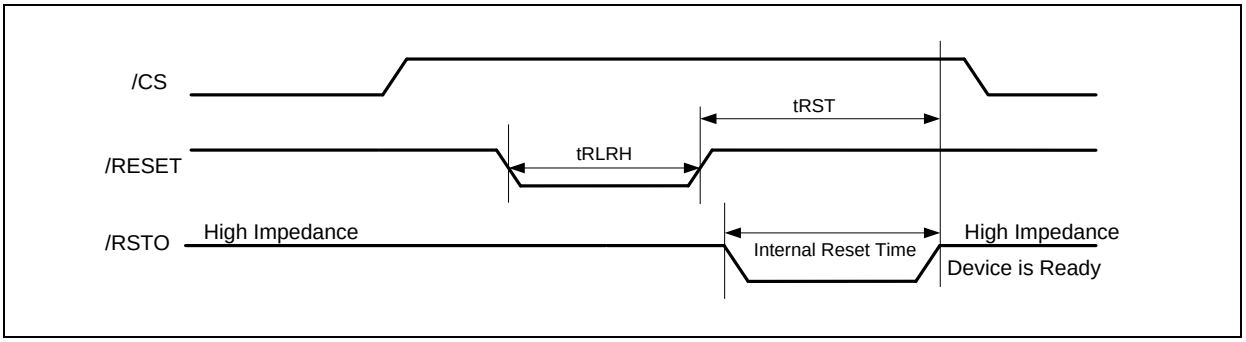
1. t_{PP} TYP measured under TA = 25°C, VCC = 1.8V with Checker Board Pattern.
2. For multiple bytes after first byte within a page, $t_{BPN} = t_{BP1} + t_{BP2} * N$ (typical) and $t_{BPN} = t_{BP1} + t_{BP2} * N$ (max), where N = number of bytes programmed.
3. Tested on sample basis and specified through design and characterization data. TA = 25°C, VCC = 1.8V, 25% driver strength.

10.9 Reset Timing

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
/RESET pin Low period to reset the device	t_{RLRH}(1,2)	50		ns
/CS High to next Command after Software/Hardware Reset	t_{RST} (1,3)	40 ns	35 µs	ns/µs

Notes:

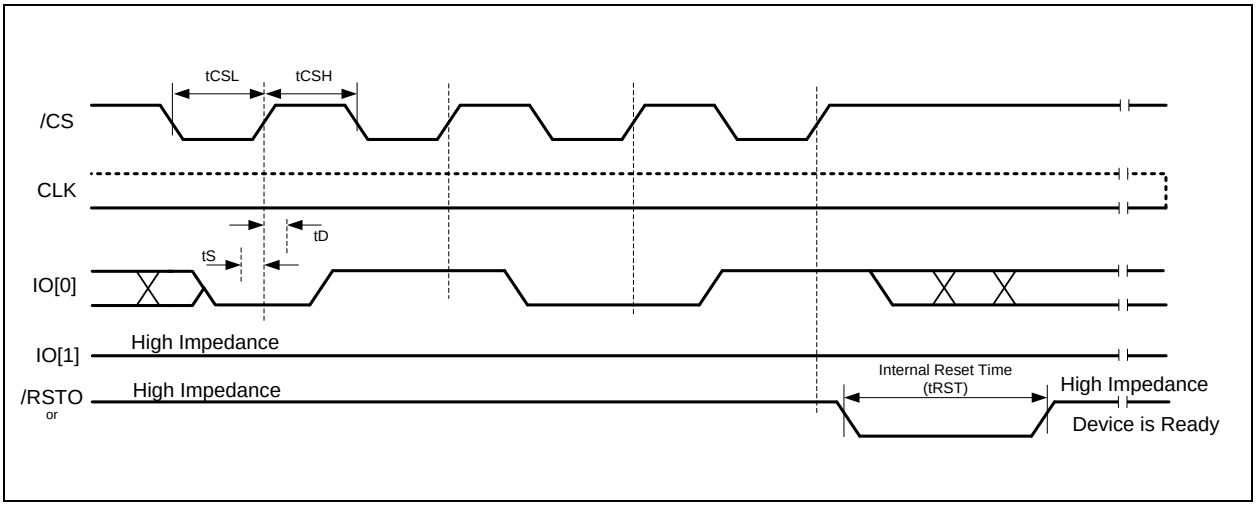
1. Values are guaranteed by characterization; not 100% tested.
2. The device reset is possible but not guaranteed if tRLRH < 50ns.
3. tRST:
   a. 40 ns minimum from reset to Standby mode after recovery from Standard/XIP Mode Reads or Volatile Writes.
4. 35 us minimum from reset to Standby mode after internal program, erase or non-volatile writes.



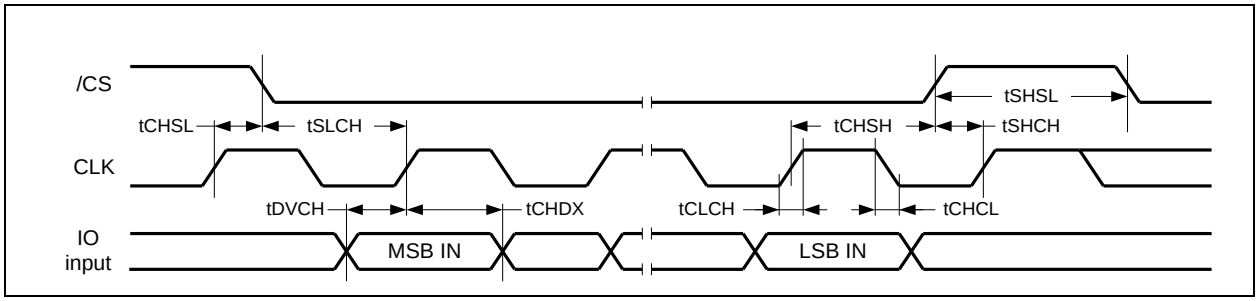
10.10 JEDEC Hardware Reset Protocol

The JEDEC Hardware Reset Signaling Protocol is based on JEDEC JESD252 Standard. It specifies the hardware resetting protocol of Serial Flash devices. The protocol can be used in the absence of or in addition to a dedicated RESET# pin on the device.

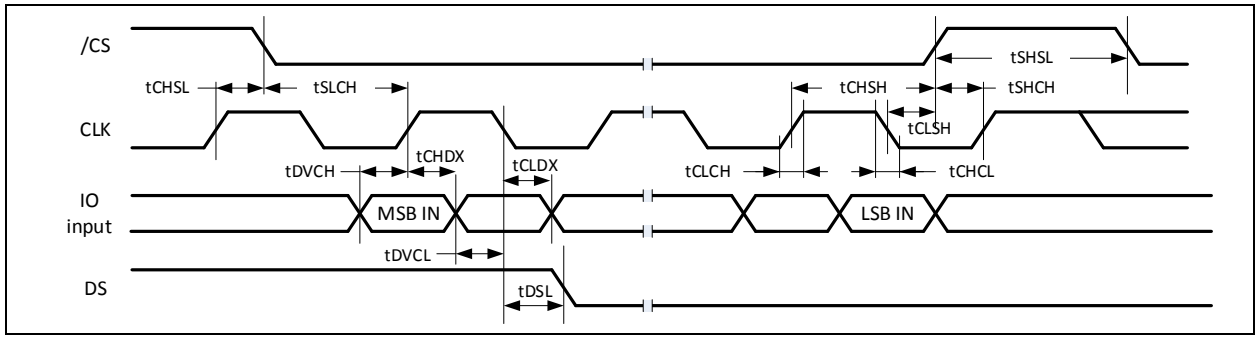
PARAMETER	SPEC		UNIT
	MIN	MAX	
/CS Low time (tCSL)	500		ns
/CS High time (tCSH)	500		ns
Setup Time (tS)	5		ns
Hold Time (tD)	5		ns



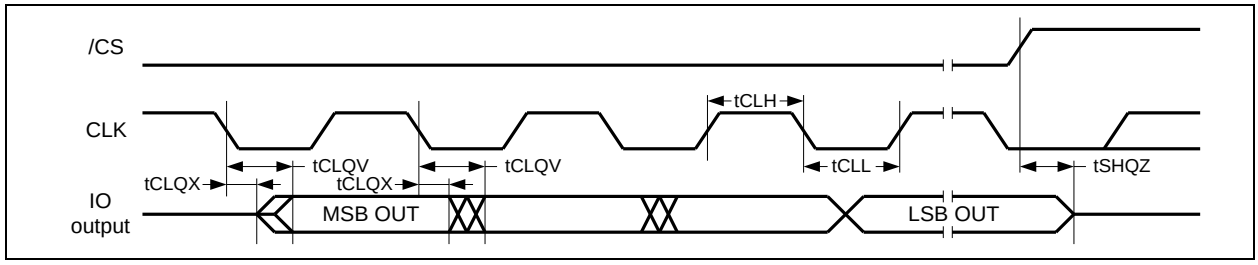
10.11 Serial Input Timing



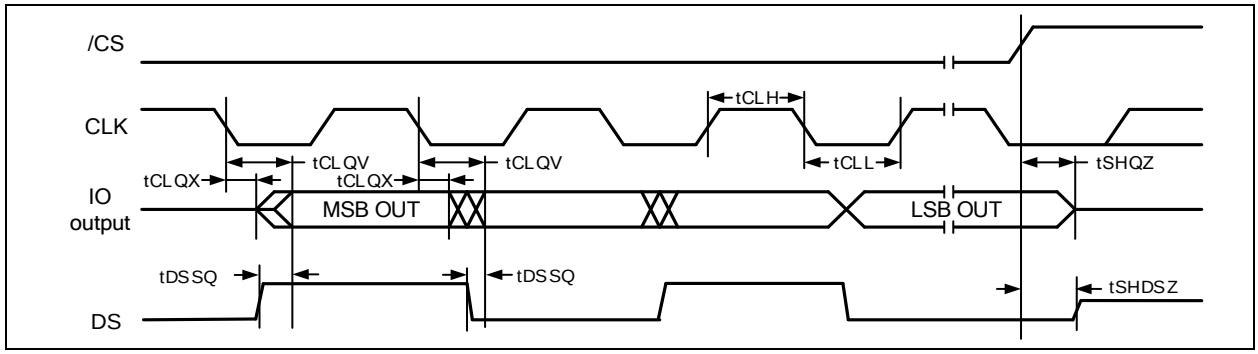
10.12 ODDR Serial Input Timing



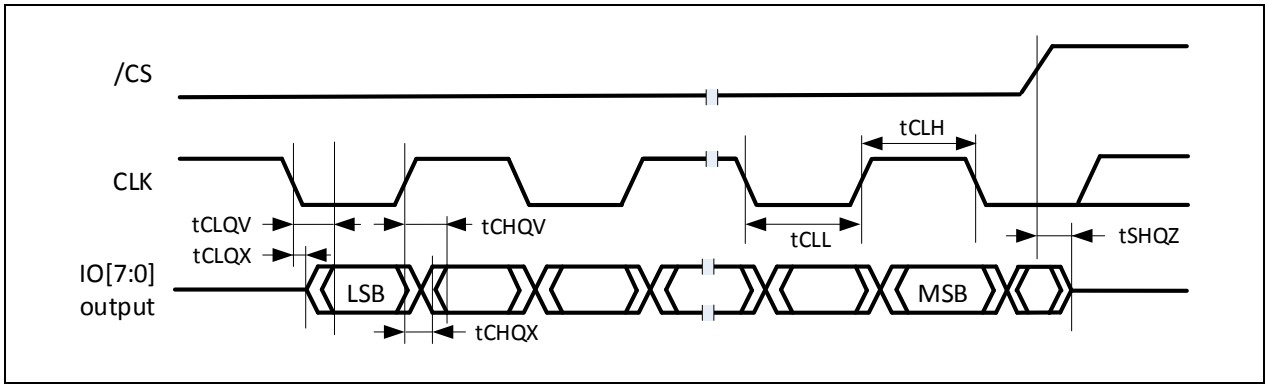
10.13 Serial Output Timing



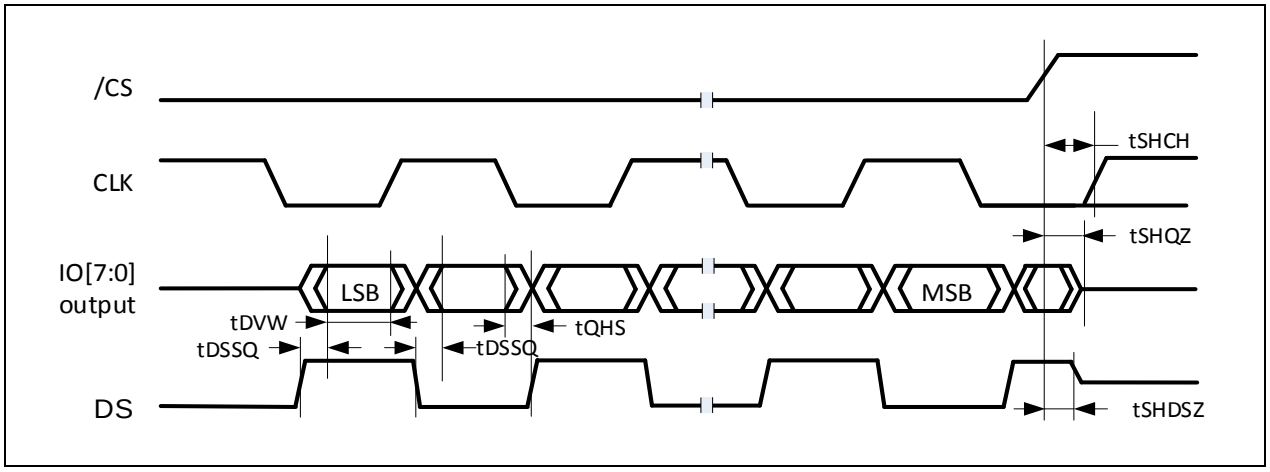
10.14 SDR Output Timing with Data Strobe



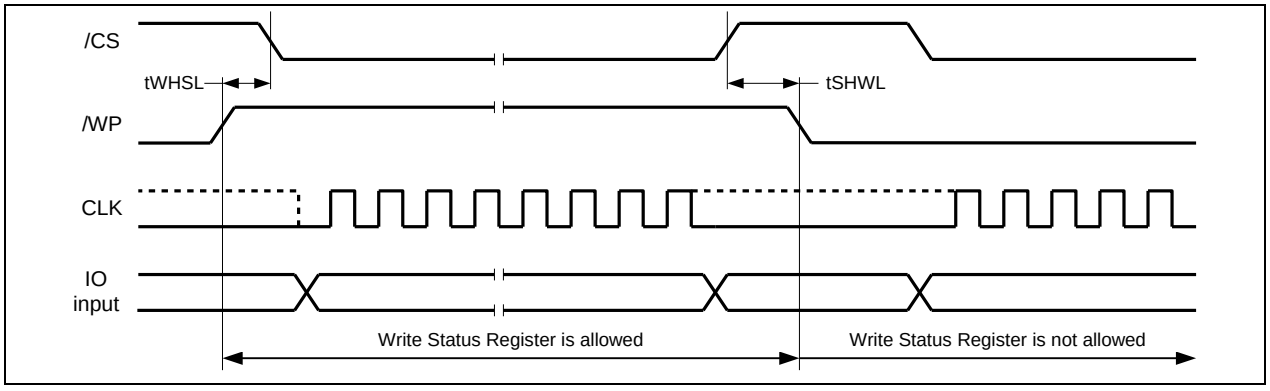
10.15 DDR Serial Output Timing



10.16 DDR Serial Output Timing with Data Strobe

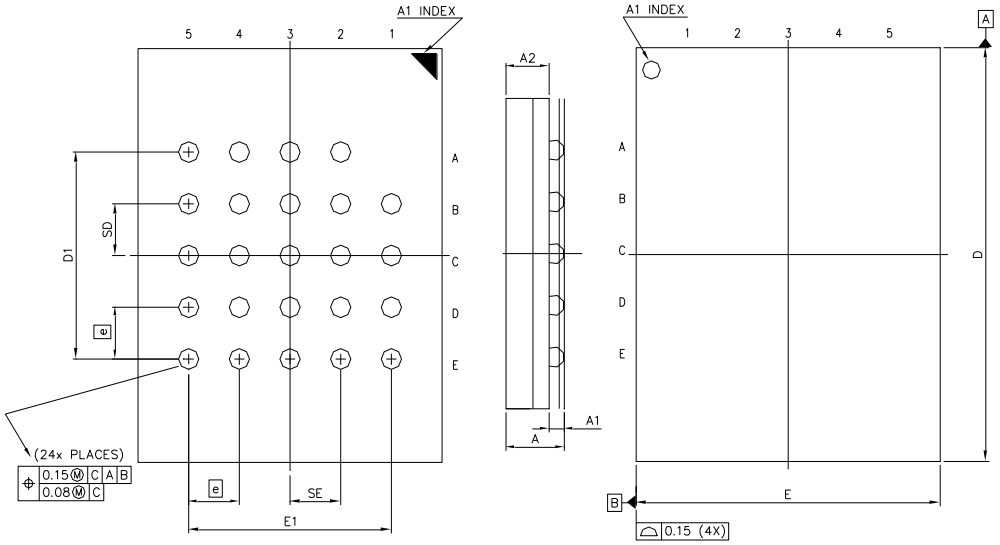


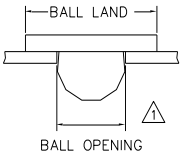
10.17 /WP Timing



11. PACKAGE SPECIFICATIONS

11.1 24-Ball TFBGA 8x6-mm (Package Code TB, 5x5-1 Ball Array)

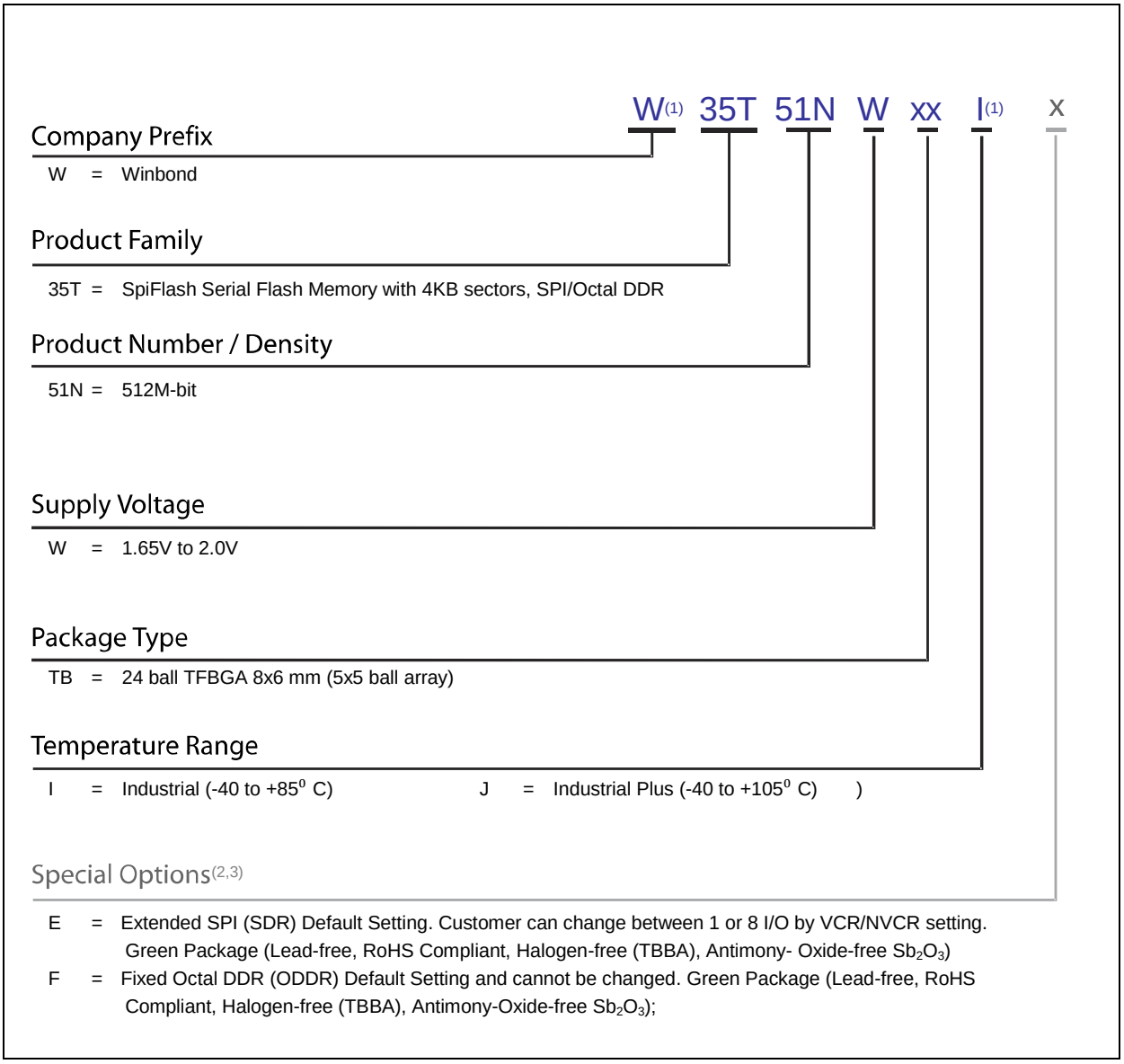




Note:
Ball land: 0.45mm. Ball Opening: 0.35mm
PCB ball land suggested <= 0.35mm

Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.20	---	---	0.047
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	---	0.85	---	---	0.033	---
b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	4.00 BSC			0.157 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	4.00 BSC			0.157 BSC		
SE	1.00 TYP			0.039 TYP		
SD	1.00 TYP			0.039 TYP		
e	1.00 BSC			0.039 BSC		

12. ORDERING INFORMATION



Notes:

1. The "W" prefix is not included on the part marking.
2. Standard bulk shipments are in Tube (shape E). Please specify alternate packing method, such as Tape and Reel (shape T) or Tray (shape S), when placing orders.
3. For shipments with special order options, please contact Winbond.

12.1 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the W35T51NW SpiFlash Memory. Please contact Winbond for specific availability by density and package type. Winbond SpiFlash memories use a 12-digit Product Number for ordering. However, due to limited space, the Top Side Marking on all packages uses an abbreviated 11-digit number.

12.1.1 W35T51NWxxxE Valid Part Numbers

Part Numbers for Industrial Grade:

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
TB TFBGA-24 8x6mm (5x5-1 Ball Array)	512M-bit	W35T51NWTBIE	35T51NWTBIE

Part Numbers for Industrial Plus Grade:

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
TB TFBGA-24 8x6mm (5x5-1 Ball Array)	512M-bit	W35T51NWTBJE	35T51NWTBJE

12.1.2 W35T51NWxxxF Valid Part Numbers

Part Numbers for Industrial Grade:

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
TB TFBGA-24 8x6mm (5x5-1 Ball Array)	512M-bit	W35T51NWTBIF	35T51NWTBIF

Part Numbers for Industrial Plus Grade:

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
TB TFBGA-24 8x6mm (5x5-1 Ball Array)	512M-bit	W35T51NWTBJF	35T51NWTBJF

13. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	03/13/2024		First release.
A2	06/17/2024	10 10,154,157,168 14 23,24 26,27,34,57-62, 65,127-130,143 37,38 44 49,50 55 66 159 161	Update Read current & Standby current values. Add Industrial Plus grade operating temperature. Remove “Available on Automotive Grade Part Numbers” from /INT output. Add note that only Mode 0 is supported. Add Advanced ECC Register description. Update Memory Protection description & table. Add footnote(4) for CMP bit. Change A8 & C4H:C7H values. Update CRC Register default values to 00h. Add SFDP footnote 4. Update tSHSL2 to 30ns, tDVCH/tDVCL tCHDX/tCLDX data setup/hold to 0.5ns, tCRC/tCRCF to 10ms/10s. Update typ tSE/tBE values.
A2.1	06/28/2024	13,14 64 115 137	Remove “Available on Automotive Grade Part Numbers from /RSTO & /INT pins Add footnote 4 on Read Serial Flash Discovery Parameter (SFDP) Modify RF & BUSY behavior after Erase/Program Resume. Correct CRC-At-Rest clock edge usage.
A2.2	07/08/2024	163	Fix typo.
B	11/10/2024	15 160 162 26-27,59-63,129-131	Merge VCC & VCCQ, VSS & VSSQ. Update AC parameters tDVCH, tDVCL, tCHDX, tCLDX, tSHDSZ. Update tSE(4KB), tSE(32KB), tSE(64KB). Add Advanced ECC Register.

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