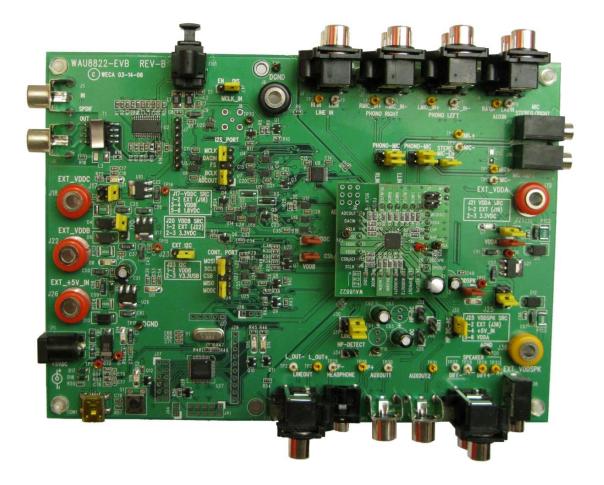
# Nuvoton Audio Codec Motherboard

# **Evaluation Board User's Guide**

(For Nuvoton CODEC series: 8812, 8814, 8810, 88C10, 8811, 8820, 8822, 8822L, 88C22, 8401, 8402, 8501, and 8502.)



#### Introduction

This system is a combination of hardware and software that enables fast and detailed evaluation of Nuvoton audio products. The hardware consists of a base evaluation board and a daughter card which contains the specific audio product to be evaluated. The daughter card system enables the use of the same base motherboard hardware and software to evaluate many different Nuvoton audio products. The software must be installed on a Windows based PC, and is compatible with most PC products and versions of the Windows operating system.

#### Summary Hardware Description

The motherboard includes a wide range of audio, power, and data input/output connectors that enable testing a very wide range of features and audio products. The motherboard kit includes a USB cable and the specific daughter card that was ordered with the system.

In most applications, the motherboard can be entirely powered via the included USB cable, and most testing can be done using only this cable as the power source. This system uses a large amount of USB power, and should NOT be used with longer or unknown quality USB cables. These can cause unreliable operation.

If additional daughter cards have been ordered with this system, it is strongly recommended to first install the software and test the system using the pre-installed daughter card. The motherboard and pre-installed daughter card have been carefully tested together, and it is best to fully verify the hardware/software system is working before changing to a different daughter card.

#### **Summary Software Description**

The supporting software includes many features that enable quick and thorough evaluation of the various supported Nuvoton audio products. The software includes easy-to-use predefined configurations, an intuitive GUI user interface, and also detailed register and bit manipulation controls to facilitate every technical level of device operation and evaluation.

Depending on how this system was ordered and delivered, software may either be provided on an included CD-ROM, or may be separately downloaded via the Internet. The software must be installed on a Windows based PC system. Downloaded versions of the software will require a Username and Password in order to start the installation process. Normally, this login information will have been provided in advance by a Nuvoton sales representative.

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## **1** Hardware Overview

All instructions in this guide require some familiarity with the physical layout of the motherboard and daughter cards. This information is introduced as needed, so it is not necessary at first to memorize or understand the complete layout and functions of the hardware.

There are various daughter card can be used for the same motherboard. They are NAU8812, NAU8814, NAU8810, NAU88C10, NAU8811, NAU8820, WAU8822, NAU8822L, NAU88C22, NAU8401, NAU8402, NAU8501, and NAU8502.

However, to get started, a few basic inputs and outputs must be noted. The USB connector and external audio inputs/outputs are highlighted in this section.

Control and power are supplied via the USB connector. When first learning how to use this system, it is recommended to choose a simple audio input and output combination. One example would be to input audio from a line level source such as a CD-audio player into the Aux inputs, and to listen to the output on the headphone connector.

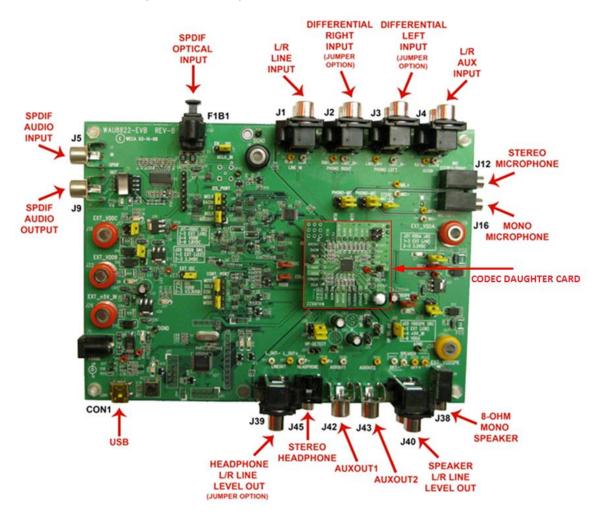


Figure 1: CODEC Motherboard SYSTEM

## 2 Software Installation and Set-Up

The software is installed using a standard PC installation software program that has been downloaded or supplied on a CD-ROM. The software installer is not an auto-start program, so it is necessary to locate the single executable (type .exe) file and run this program manually.

If the installation software has been downloaded, the installer program will request a Username and Password to complete the installation procedure. Normally, these will have been provided in advance by a Nuvoton sales representative. Using a downloaded version of the software will insure having the most recently released version of the program.

 If no version of this GUI Application has been previously installed on the PC, components will be added that enable the PC to recognize the Nuvoton USB audio hardware. Depending on the operating system and configuration, it may be necessary to reboot the PC after the first-time installation. If the installation program recommends rebooting the PC, it is best to do so. However, a requested reboot can usually be ignored, and all components will operate correctly.

The software installation procedure does not overwrite or replace older versions of the GUI Application software. In some cases, it may be desirable to keep older versions of the application available while learning to use a newer version.

If it is preferred to remove older versions of the application, the software should be removed BEFORE installing the new software. The reason is that the un-install process may remove common shared library components needed by the newer version of the application. An undesired version application can be removed (before installing a newer version) using the standard un-install feature included in Windows PC "Add or Remove Programs" control panel.

## **3 PC Configuration**

IMPORTANT INFORMATION: The GUI Application software installation and configuration is entirely automatic. However, because the EVB is registered with the PC as an "Audio Device," sound from inside the PC may automatically be routed to the Nuvoton EVB. The EVB is registered as a USB audio device, because it has the capability to receive an audio stream over the USB bus.

Thus, after plugging the EVB into a PC, audio inside the PC may appear to stop working or be changed in ways that are surprising. Managing the PC audio routing will be especially important if it is desired to use the PC as an audio source as part of the EVB evaluation process.

Therefore, it is important to understand how to manage and control the PC built-in software and hardware audio features. What happens automatically, and the details of how to manage audio inside the PC will vary depending on the Windows version and specific PC hardware. Further details may be different if other audio hardware and or software has been installed on the PC.

In all Windows systems, the management of audio is similar. This is typically done using the "Control Panel" option in the Start Menu, and then selecting the appropriate audio control icon or menu item. It may also be possible to access the PC audio control panel by clicking or rightclicking on the speaker icon in the Task Bar, normally at the bottom of the PC screen.

After activating the audio control panel, there will be various options. There will be an option for routing sound to and from the PC, and in this option there will be a list of possible audio devices. The Nuvoton EVB is registered as an "Audio Device." It is possible other audio devices attached to the PC may have the same or similar name. The Nuvoton EVB can be identified in this case by unplugging/replugging into the PC to see which item is changed in the list of audio devices.

Again depending on the Windows system and configuration, any selection made in the control panel may later be automatically changed by the PC system. Also, media player software may not immediately recognize that the PC audio path has been changed. It is best to quit and then restart any media player application after making a change to the audio routing using the PC control panel.

## 4 Running the GUI Application

After installation, and depending on the Windows operating system and installation options, an icon to start the application may have been added to either or both the Desktop and Start Menu locations. The program will always be available under the Run option in the Start Menu. The application name will always start with the word "Nuvoton."

The application may be started with or without the motherboard USB hardware attached. If the motherboard is not attached, the application will run in a "software demo" mode that enables becoming more familiar with the software.

After starting, the following start-up screen will be displayed.

The normal use of the application at this time is to click on the icon that matches the actual device that is on the installed hardware daughter card. Clicking on this icon will then configure the software to match the attached hardware, and after this, evaluation can begin immediately. The next window that opens will be the DEMO page that is explained below.



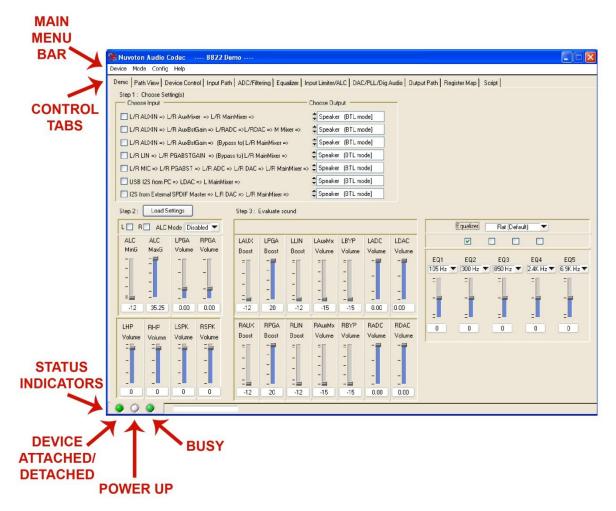
Figure 2: GUI APPLICATION START-UP SCREEN

## **5** Getting Started Using the GUI Application

After making the selection on the start-up screen to select the audio device to be evaluated, the GUI Application will open to the Demo Panel screen. All panels are structured similarly and include the Main Menu Bar, Control Tabs, and Status Indicators.

### 5.1 DEMO Panel Status Indicators

The Status Indicators are located in the lower left hand corner of every Control Tab screen. These indicators are especially important, as they provide the highest level of system status.





#### 5.1.1 Device Attached/Detached Indicator

The Status Indicator on the far left is the most important. This indicator will be Green when the motherboard hardware is attached to the PC, and signals that the PC has recognized the hardware and established communication with the hardware. If the indicator is white, then no interaction with the motherboard or daughter card is possible.

#### 5.1.2 Power Up Indicator

The middle status indicator is the Power Up Indicator. This will be Green after the software has powered up all elements on the motherboard necessary to interoperate with the daughter card. If the indicator is white, then the motherboard and communications between the motherboard and daughter card have not been set up, and no interaction with the daughter card is possible.

#### 5.1.3 Busy Indicator

The status indicator on the right-hand side indicates when the GUI Application is making changes to the motherboard and/or the daughter card. This will be Green when all changes are completed and the hardware is configured for operation. This indicator will be white when the GUI Application is busy making changes to the motherboard and/or the daughter card.

#### 5.2 Introduction to Main Menu Bar

The Main Menu Bar is included on the Demo Panel, the start-up screen, and all other views. This enables direct and quick access to some features common to all devices. Many of these features are for more experienced users, and this section can be studied as needed at a future time.

#### 5.2.1 Device

The Device menu allows changing the selected daughter card device without restarting the application. This can be useful if the wrong device was accidentally selected, or it can be used to switch daughter cards without restarting or powering down the hardware. However it is preferred to power-down the hardware and restart the application to change daughter cards This more conservative procedure will insure the greatest reliability for both the hardware and software.

#### 5.2.2 Mode

The Mode selection is normally automatic and the user should NOT change this. This menu item enables changing the hardware control bus protocol between the motherboard and the audio device being tested.

The Mode feature is included for instances when the motherboard or daughter card hardware has been custom modified to be hard-wired into a particular control bus configuration. Then, it is important to have a top-level menu control to change this selection. The control bus modes are explained in more detail in the section describing the Device Control menu tab functionality.

#### 5.2.3 Config

The Config menu enables Exporting or Importing settings from a standard file stored on the PC system. This feature saves only the settings for the audio device being tested, and not the configuration of the motherboard itself. So, the motherboard must already be initialized and set up in the desired mode before executing the Import function.

Export/Import is useful for saving configurations for future use, or for sharing configurations with other users. It is also a convenient way to copy/paste a set of desired register settings from the EVB environment directly into software used to control the device in the actual end product.

# nuvoTon

## 6 The Control Tabs

All of the main features and many options are selected by choosing one of the Control Tabs. This is the horizontal menu list immediately below the Main Menu. After the user selects the device, the application automatically opens into the Control Tab for the Demo Panel. It is best to first work with the Demo Panel to begin learning how to use this application and the other Control Tabs. The following sections describe the functions of each Control Tab in more detail.

#### 6.1 Demo Panel

The Demo Panel is important, because it enables complete, proven, and working examples of how to configure the device on the daughter card. This panel also will automatically initialize the EVB (if necessary) and do other initialization as may be needed to start up the device on the daughter card. The idea of this panel is to be able to use the EVB with almost no understanding of any other function of the EVB and its many options.

The Demo Panel breaks down operation of the EVB into three simple steps. These are grouped together visually on the PC screen, and each group is labeled as a numbered Step.

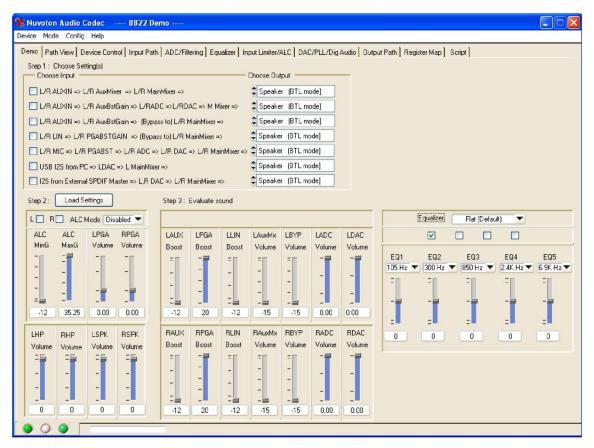


Figure 4: DEMO CONTROL PANEL

#### 6.1.1 Step 1: Choose Settings

The Choose Settings selection enables selection of the input, as well as the entire path for audio from the selected input, through all of the device options, and then to the output. The path descriptions are listed in an abbreviated form to fit within the GUI display.

The Choose Settings selection also enables choosing various possible outputs and output combinations that will work with the selected input. These selections may be scrolled one-at-a-time using the up/down arrows in the output selection area. They may also be selected directly by clicking on the text of the output path that is shown. This will open a pop up a window showing all of the possible output selections, and then the desired selection can be made directly.

#### 6.1.2 Step 2: Load Settings

Clicking on this button will cause all of the desired settings to be loaded into the audio device being tested. Additionally, any necessary changes to the EVB initialization or configuration will be performed automatically at this time.

While the settings are being loaded, the Status Indicators at the bottom left of the screen may change from Green to White. IMPORTANT: If the configuration was successfully completed, all three Status Indicators will be Green, and the configuration is now ready for evaluation.

#### 6.1.3 Step 3: Evaluate Sound

The bottom portion of the screen includes a few controls that enable experimentation with some of the settings that can be changed on the audio device being tested. These can be changed using the GUI, and the effect on the device will be immediate. Do NOT push the "Load Settings" button again while using this feature. This will cause all of the settings to revert to the original selected Demo configuration.

At this time, it may be useful to select any of the other Control Tabs. These make available many more controls and features that can be changed after the Demo selection has been loaded.

## 7 Demo Example for NAU8822

In this example, the goal is to pass audio from the left and right auxiliary inputs, into the ADC, from the ADC into the DAC, and then output to the headphones. This is accomplished by the following three steps:

Choose: "L/R AUXIN => L/R AuxBstGain => L/RADC => L/RDAC => M Mixer => Select for the output: Headphone Push the "Load Settings" button and verify all three Status Indicators change to Green

At this point, any line level audio input attached to the Aux inputs should be audible in a headphone attached to the headphone jack. A suitable line level audio source would be the output from a CD-audio player or other media player device.

#### 7.1 Path View Control Panel

This panel shows in a graphical form the internal structure of the device being tested as it related to the available input, output, and control pins on the device. This is a highly interactive panel, and most of the features and controls are "clickable." This means that on the GUI screen you can simply click on a functional block or path and change its settings. You can also use this panel to see some of the settings that are currently in use.

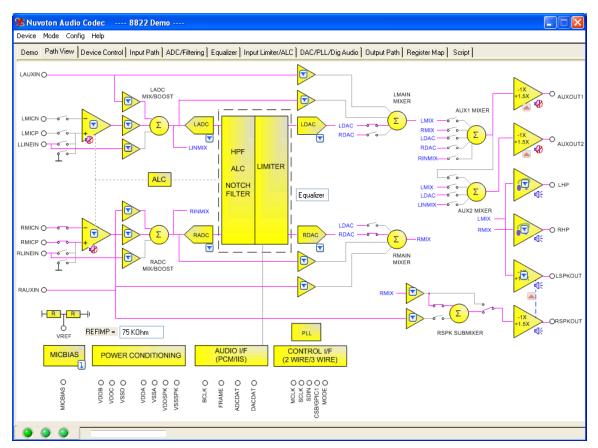


Figure 5: PATH VIEW

This panel is intended to be used after a full set of settings has already been loaded into the device. This panel is difficult or impossible to use without having done this first. The main reason for this is that power control features are in the "off" condition, and these are not all directly available on the Path View.

To simplify use of the Path View, the Demo settings have been set up with all of the power control features in the "on" condition. This makes the Path View simpler to use, because it may not be at all obvious that a particular path is not working because one of the elements in the path does not have power.

#### 7.1.1 Description of Special Icons in Path View

Here is a summary of the "language" that can be used in this graphical environment:

The active path over which audio is enabled, is indicated by red colored lines in the GUI. In some cases, the lines are clickable and the path can be enabled/disabled simply by clicking on the line. This includes on/off switches which are also clickable with the active path indicated in red.

A speaker icon indicates that an output or input block is enabled. The disabled state will show the speaker icon with the international red "crossed out" overlay.

Items for which a drop-down or pop-up menu will appear are marked with a small down-arrow icon. This can be used to either view the current setting or to change a setting.

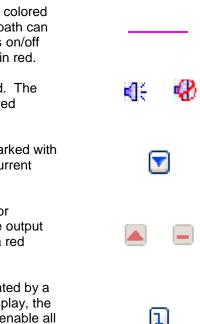
On NAU8822 devices, some of the outputs can be in a "boost" or "non-boost" gain configuration. This status is indicated near the output icon with a red up-arrow symbol to indicate the Boost state, or a red horizontal line symbol indicating the "Non-Boost" state.

Additionally, if a block is does not have power, this will be indicated by a right-angle down-arrow icon. To reduce visual clutter on the display, the "power-on" status is not shown. Because the Demo selections enable all power to all blocks, no power-down icons will normally be seen. However, if power is turned off using other Control Tabs, or the Path View is selected before loading any settings into the device, then the power-down icons will be visible.

#### 7.1.2 Path View Navigation Shortcuts

Clicking on blocks in the GUI view that have many functions will in some cases cause the display to switch to the Control Tab view appropriate for that block. This is a quick, powerful, and convenient way to change features in a block too complex to show in this Path View.

After clicking on a block that switches to a different Control Tab view, changes can be made in that view. When the changes are complete, simply right-click on the current Control Tab view, and the display will automatically switch back to the Path View. The Path View will automatically be updated to show any changes that were made in any of the other Control Tab panels.



#### 7.2 Device Control Panel

This panel modifies the basic configuration of both the motherboard and the audio device under test. In general, these features are for advanced users. Except for the "Initialize Board," "Initialize Device," and "Device Control" radio buttons, other settings in this panel should not be changed without a good understanding of the underlying functions.

The panel manages four basic groups of functions:

- 1) Radio button controls for motherboard and device management
- 2) Board Settings to select various motherboard hardware configuration options
- 3) Device Settings to select power options for high voltage NAU8822 outputs
- 4) Power Management features for the NAU8822 device

For less experienced users, the only Device Control radio buttons that should be used are the "Initialize Board" and "Initialize Device" buttons. These set up the motherboard and device, respectively, to basic starting conditions. These buttons may be most useful after having made many changes, and the state of the motherboard or device is unclear.

🛞 Nuvoton Audio Codec 📖 8822 Demo 📖 🔲 🗌 🔤 🔀			
Device Mode Config Help			
Device       Mode       Config       Help         Demc       Path View       Device Control       Input Path       ADC/Filtering       Equalizer       Input Limiter/ALC       DAC/PLL/Dig Audio       Output Path       Registe         Initialize Board       Initialize Device       Initialize Device       Device Settings       Device Settings         Command Interface       Speaker Power Supply       VDDSPK = 5V       (Output Boost = 1.5k)       VDDSPK = 5V       (Output Boost = -1.0)         VDDSPK = Read/Write       I2C CLK       500K       Device Control       Device Control         External Control       Set Mode Pin High       Power Up       Reset Device	r Map   Script   Power Management [ [DCBUFEN] [ [AUX1MXEN] [ [AUX1MXEN] [ [AUX2MXEN] [ [AUX2MXEN] [ [PLLEN] [ [MICDIASEN] Microphone Bias Enable [ [ABASEN] [ [IOBUFEN] [ REFIMP] 75 KDhm		
□ Digital Audio Reset         □ Digital Audio Reset         □ Digital Audio (125) Mode [Feed MCLK to device]         □ Audio Precision (125) Master Mode Interface Enable         □ Digital Audio (125) Master Mode Interface Enable         □ Digital Audio (125) Slave Mode Interface Enable         □ Digital Audio (125) Interface Header Enable         □ Digital Audio (125) Inter	IHHEN     IHHEN     IHHEN     IHHEN     ILHFEN     ILLFEN     ISLEEP     IGSTEN     RADC Mix/Boost stage Enable     ILBSTEN     LADC Mix/Boost stage Enable     ILBSTEN     ILADC Mix/Boost stage Enable     ILFGAEN     ILLFACEN     ILFT     ILFT     ILLFACEN     ILLFACEN		
	[LDACEN] Lett Channel DAC Enable		

Figure 6: DEVICE CONTROL OVERVIEW

#### 7.2.1 Device Settings

This changes the 5-volt or 3-volt settings of the NAU8822 outputs to match the actual voltage supplied on the VDDSPK pin. Management of the power options is explained in other sections of this document.

IMPORTANT: These settings should NOT be changed unless work is being done to change the internal or external VDDSPK voltage. For reliable operation, it is very important that these settings match the actual voltage on VDDSPK. The motherboard is set up by default to the 5-volt settings for VDDSPK, and this default software selection matches this default configuration.

The other Device Control radio buttons change various features as indicated by the text in the button. These change many different register values, and in many cases require a detailed understanding of information in the device data sheet and/or design guide.

- Reset: Writes to Register 0x00 of an NAU8822 device for its Reset condition
- PowerUp: Turns on basic registers to put an NAU8822 device into an "on" condition
- PowerDown: Sets an NAU8822 device into a low power "sleep" condition
- MuteAllOutputs: Enables only the Mute function on NAU8822 outputs
- EnableAllOutputs: Turns on power control bits for all outputs
- DisableAllOutputs: Turns off power control bits for all outputs
- LoadDefaultUpdateBits: Write to update bits to cause update feature to take place

Figure 7: DEVICE CONTROL PANEL - DEVICE SETTINGS

#### 7.2.2 Board Settings

These settings change the basic configuration of the motherboard communications with the device on the daughter card. These can affect the control bus mode, the I2S audio data stream, and also select external connectors as alternative sources and sinks for these signals.

IMPORTANT: Changes to this portion of the panel do NOT become effective until pushing the "Config Board" radio button. This button is located at the bottom of this grouping of controls.

🕦 Nuvoton Audio Codec 📖 8822 Demo 📖 🔲 🗌 🔀			
Device Made Config Help			
Device Mode Config Help Demo Path View Device Control Input Path ADC/Filtering Equalize Initialize Board Board Settings Command Interface 3 Wire SPI Mode - Write Only (4 Wire SPI when reading) 4 Wire SPI Mode - Read/Write 12C Mode - Read/Write 12C CLK 500K ▼ External Control Set Mode Pin High	Initialize Davice Device Settings Speaker Power Supply VDDSPK = 5V (Output boost = 1.5x) VDDSPK = 3.3V (Output Boost = -1.0) Device Control	ster Map   Script   Power Management [ [DCBUFEN] [ [AUX1MXEN] [ [AUX2MXEN] [ [PLLEN] [ [MICBIASEN] Microphone Bias Enable [ [ABIASEN] [ [BEJFEN] [ [BEFIMP] ] 75 KOhm	
I2S Signal Connection         Digital Audio Reset         I2S Master         Øn-Board USB (I2S) Mode [Feed MCLK to device]         Audio Precision (I2S) Master Mode Interface Enable         Digital Audio (I2S) Master Mode Interface Enable         I2S Slave         Audio Precision (I2S) Slave Mode Interface Enable         Digital Audio (I2S) Slave Mode Interface Enable         Digital Audio (I2S) Slave Mode Interface Enable         Digital Audio (I2S) Slave Mode Interface Enable	Power Up Reset Device Power Down Mute All Outputs Load Default Update Bits Enable All Outputs Disable All Outputs Power Management	[RHPEN]     [LHPEN]     [LHPEN]     [SLEEP]     [RBSTEN] R ADC Mix/Boost stage Enable     [LBSTEN] L ADC Mix/Boost stage Enable     [RPGAEN] Right Channel PGA Enable     [LPGAEN] Lett Channel PGA Enable     [RADCEN] Right Channel ADC Enable     [LADCEN] Lett Channel ADC Enable     [LADCEN] Lett Channel ADC Enable	
Direct Digital Audio ((25) Interface Header Enable Config Board	Image: Instance         Image: Imag	[AUXOUTTEN]     [AUXOUTZEN]     [JSFKEN]     [ISFKEN]     [BIASGEN]     [BIASGEN]     [RMMEN]     [MIXEN]     [MIXEN]     [RMACEN] Right Channel DAC Enable     [LDACEN] Left Channel DAC Enable	

Figure 8: DEVICE CONTROL PANEL – BOARD SETTINGS

#### 7.3 Command Interface

This selects options for the control bus to the daughter card device. Normally, this selection is automatic and these settings should not be changed unless there is a specific goal to work with the command interface.

The listed options set up the motherboard and device on the daughter card to work together in the indicated mode. Additionally, the speed of the I2C clock can be altered.

### 7.4 External Control

In addition to the built-in interfaces, an external command interface control can be selected. In this case, control to and from the daughter card is via the CONT. PORT, Connector J24. Bidirectional level shifters are used to connect the daughter card to this port instead of to the internal port provided on the motherboard.

Coupled with the External Control is the ability to set the MODE pin on the NAU8822 device to high or low. This feature is needed to set the control mode in the NAU8822 device as described in the NAU8822 device design guide.

When using the CONT. PORT interface, an additional option exists to set the voltage used by the level shifter. This is changed by the jumper on Connector J23. Pin #1 of this connector is indicated by a square symbol on the PCB silkscreen.

#### 7.5 I2S Signal Connection

The I2S path is the serial data path for audio the digital audio signal to and from the device on the daughter card. This feature is automatically handled, and should be changed only when specific work is being done with the I2S bus.

#### 7.5.1 Digital Audio Reset

A SPDIF controller chip is included on the motherboard for coupling audio to and from the device on the daughter card using I2S serial data. Selecting this option will reset the SPDIF controller.

#### 7.5.2 I2S Master

The motherboard can be configured as the I2S Master or I2S Slave, but not both at the same time. In most applications, the motherboard will be the I2S Master. There are several options for the signal source in I2S Master Mode.

#### 7.5.3 On-Board USB

When audio is streamed from the USB host (typically a PC computer), the USB controller device on the motherboard is configured by this selection to be the I2S Master. When selecting USB audio in the Demo Panel, this selection is made automatically.

It should be noted that the built-in USB controller supports only a monophonic data stream. In the Demo Panel configuration, this same audio stream is output to both the left and right channels. Also, the USB mode does NOT support streaming of audio from the daughter card to the PC.

#### 7.5.4 Audio Precision I2S Master

This control is for when I2S audio is streamed from an external master source connected to the I2S\_PORT, Connector J15. Bi-directional level shifters are selected by this option to connect the daughter card to this port instead of to the internal port provided on the motherboard. External equipment, such as an Audio Precision analyzer must be configured to be the I2S master.

#### 7.5.5 Digital Audio Master

This control is for when I2S audio is streamed from the SPDIF controller included on the motherboard. Bi-directional level shifters are selected by this option to connect the daughter card to the SPDIF controller, instead of to the USB I2S port also provided on the motherboard. When selecting SPDIF audio in the Demo Panel, this selection is made automatically.

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#### 7.5.6 I2S Slave

The motherboard can be configured as the I2S Master or I2S Slave, but not both at the same time. In most applications, the motherboard will be the I2S Master. This section controls options for the audio signal source in I2S slave mode.

#### 7.5.7 Audio Precision Slave Mode

This control is for when I2S audio is streamed to an external slave device connected to the I2S\_PORT, Connector J15. Bi-directional level shifters are selected by this option to connect the daughter card to this port instead of to the internal port provided on the motherboard. External equipment, such as an Audio Precision analyzer must be configured to be the I2S slave.

#### 7.5.8 Digital Audio Slave

This control is for when I2S audio is streamed to the SPDIF controller included on the motherboard. Bi-directional level shifters are selected by this option to connect the daughter card to the SPDIF controller, instead of to the USB I2S port also provided on the motherboard.

At the present time, the GUI Application software does not implement the ability for the SPDIF controller to stream audio out from SPDIF\_OUT, Connector J9.

#### 7.5.9 Direct Digital Audio Interface Header Enable

This control connects the I2S port on the daughter card device directly to the I2S\_PORT header Connector J15, but does not configure the daughter card device I2S direction. The daughter card device must be configured separately. Bi-directional level shifters are selected by this option to connect the daughter card to the J15 header connector, and not to any of the I2S devices on the motherboard.

## 8 Power Management

This panel of controls gives direct access to the various power management bits available in the NAU8822 device. Control of these bits is normally automatic. These bit controls are made available here for convenient manipulation and evaluation of the power control features.

The function of each of these control bits is explained in detail in the NAU8822 device Design Guide documentation. The names for each control in this panel match the names given to specific control bits in the NAU8822 control registers. The description and function for each of these bits can be found (most easily by doing a text string search) in the Details of Register Operation appendix portion of the NAU8822 device Design Guide.

Figure 9: DEVICE CONTROL PANEL – POWER MANAGEMENT

## 9 Input Path Control Panel

This Control Tab gives access to the various controls and settings for the analog audio input routing, power management, and gain blocks up to, but not including, the ADC converters. Control of these bits is normally automatic when using the Demo Panel. These bit controls are provided here for convenient manipulation and evaluation of the input path features and settings.

The function of each of these control bits is explained in detail in the NAU8822 device Design Guide documentation. The names for each control in this panel match the names given to specific control bits in the NAU8822 control registers. The description and function for each of these bits can be found (most easily by doing a text string search) in the Details of Register Operation appendix portion of the NAU8822 device Design Guide. It can also be helpful to switch to the Path View tab to better see how each of these controls affects the device settings and routing.

🛞 Nuvoton Audio Codec 🛛 8822 Demo			
Device Mode Config Help			
Demo   Path View   Device Control Input Path   ADC/Filter	ring   Equalizer   Input Limiter/ALC   DAC/PLL/Dig Audio   Output P	ath   Register Map   Script	
Power Management     [LPGAEN] Left Channel PGA Enable     [RPGAEN] Right Channel PGA Enable	Power Management	Power Management [ [LBSTEN] LADC Mix/Boost stage Enable [ [RBSTEN] R ADC Mix/Boost stage Enable	
Input Control [LMICPLPGA] LMICP to L PGA Positive Input [LMICNLPGA] LMICP to L PGA Negative Input [LLINLPGA] LLIN to L PGA Positive Input [IMICPRPGA] RMICP to R PGA Positive Input [RMICNRPGA] RMICN to R PGA Positive Input	MicroPhone Bias Volkage Control [MICBIASM] MIC BIAS Mode	Left ADC Boost [LPGABST] L PGA Boost (+20dB over 0dB) [LAUXBSTGAIN] LAUXIN Gain      ① 0.0dB [LPGABSTGAIN] LUN Gain      ⑦ Path Disable Right ADC Boost [RPGABST] R PGA Boost (+20dB over 0dB) [RAUXBSTGAIN] RAUXIN Gain      ⑦ 0.0dB	
Left Input PGA Gain [LPGAGAIN] L PGA Volume Setting ①0.0dB 「 [LPGAMT] L PGA Mute 「 [LPGAZC] L PGA Zero Cross 「 [LPGAU] PGA Volume Update bit Right Input PGA Gain [RPGAGAIN] R PGA Volume Setting ②0.0dB 「 [RPGAMT] R PGA Mute 「 [RPGAMT] R PGA Mute 「 [RPGAZC] R PGA Zero Cross 「 [RPGAU] PGA Volume Update bit	ALC Control [ALCEN] ALC Select ALC Off "When ALC is enabled, PGA volumes are controlled automatically, and L,RPGAGAIN bits should not be used. **	[RPGABSTGAIN] RLIN Gain 🗘 Path Disable	

Figure 10: INPUT PATH CONTROL PANEL

#### 9.1 Microphone Bias

This section also provides control over the microphone bias circuit. This function provides lownoise DC power from the MICBIAS output pin that is normally used to power one or more external microphones. The description and function for each of these bits can be found (most easily by doing a text string search) in the functional descriptions, and also, the Detailed Register Map in the NAU8822 device Design Guide.

## **10 ADC/Filtering Control Panel**

This Control Tab gives access to the various controls and settings in the ADC converter blocks. Controls are also included here for the digital high pass filter, digital notch filter, and gain options associated with the ADC function.

Control of these bits is normally automatic when using the Demo Panel. These controls are provided in this panel for convenient manipulation and evaluation of the ADC section features and signal processing settings.

The function of each of these control bits is explained in detail in the NAU8822 device Design Guide documentation. The names for each control in this panel match the names given to specific control bits in the NAU8822 control registers. The description and function for each of these bits can be found (most easily by doing a text string search) in the Details of Register Operation appendix portion of the NAU8822 device Design Guide. It can also be helpful to switch to the Path View tab to better see how each of these controls affects the device settings and routing.

🗱 Nuvoton Audio Codec 🛛				
Device Mode Config Help				
	Equalizer   Input Limiter/ALC   DAC/PLL/Dig Audio   Output Path   Register Map   Script   Digital ADC Volume Control [LADCGAIN] Left Ch. ADC Digital Volume 0.008 [RADVGAIN] Right Ch. ADC Digital Volume 0.008 [ LADC/U] Update: LADC immediate, RADC pending. [ RADC/U] Update: RADC immediate, LADC pending.			

Figure 11: ADC/FILTERING CONTROL PANEL

## **11 Equalizer Control Panel**

This Control Tab gives access to the various controls and settings for the Equalizer and 3-D Audio digital signal processing blocks. This pair of functions may be applied to either the ADC digital outputs, or to the DAC digital inputs, but not to both paths at the same time.

These features are explained in detail in the NAU8822 device Design Guide documentation. Also, the names for each control bit in this panel match the names given to specific control bits in the NAU8822 control registers as described in the detailed register map in the NAU8822 Design Guide. The description and function for each of these bits can be found (most easily by doing a text string search) in the Details of Register Operation appendix portion of the NAU8822 device Design Guide.

This panel provides both graphical equalizer style controls and control panel style controls to modify the Equalizer settings. A change in either type of control is reflected in both controls.

Additionally, a few Equalizer presets are provided in a scrolling window beneath the 3-D Audio controls. These presets give some examples of the many ways to configure the Equalizer. When a preset is applied, the settings for these are reflected in all of the control panels, and also, in the register map.

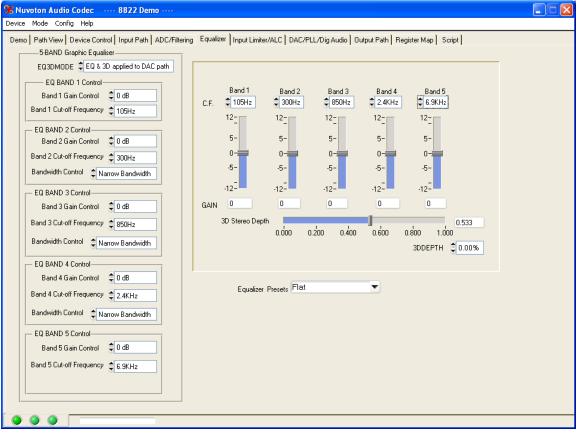


Figure 12: EQUALIZER CONTROL PANEL

## **12 Input Limiter and ALC Control Panel**

This Control Tab gives access to the various controls and settings for the Input Limiter and ALC signal control blocks.

The operation of each of these functions is explained in detail in the NAU8822 device Design Guide documentation. Also, the names for each control bit in this panel match the names given to specific control bits in the NAU8822 control registers as described in the detailed register map in the NAU8822 Design Guide. The description and function for each of these bits can be found (most easily by doing a text string search) in the Details of Register Operation appendix portion of the NAU8822 device Design Guide.

Additionally, a few Equalizer presets are provided in a scrolling window beneath the 3-D Audio controls. These presets give some examples of the many ways to configure the Equalizer. When a preset is applied, the settings for these are reflected in all of the control panels, and also, in the register map.

🗱 Nuvoton Audio Codec 📖 8822 Demo 📖 🔲 🔲 🔀			
Device Mode Config Help			
Demo   Path View   Device Control   Input Path   ADC/Filtering   Equalizer Input Limiter/ALC   DAC/PLL/Dig Audio   Output Path   Register Map   Script			
ALC Control 1 ALC Noise Gate Control			
[ALCMNGAIN] ALC Minimum Gain C-12dB [ALCNTH] ALC Noise gate threshold: C-39dB			
[ALCMXGAIN] ALC Maximum Gain (+35.25dB F (ALCTBLSEL) Target level table select (default 1)			
ALC Control 2			
[ALCSL] ALC target level at ADC output     -6dBFS       [ALCHT] Hold time before ALC gain     0 ms       Music -			
ALC Control 3			
[ALCM] ALC Mode     Limiter Mode operation       ALCM = Normal Mode     Speech-			
[ALCDCY] ALC Decay     4ms/step       [ALCATK] ALC Attack     500us/step			
ALCM = Limiter Mode			
[ALCDCY] ALC Decay C 1ms/step			
[ALCATK] ALC Attack 2124us/step			

Figure 13: INPUT LIMITER AND ALC CONTROL PANEL

## 13 DAC/PLL/Digital Audio Control Panel

This Control Tab manages three major functional groups: control of the DACs themselves, management of the PLL and voltage reference that support the DACs, and miscellaneous functions also related to operation of the DACs.

The operation of each of these functions is explained in detail in the NAU8822 device Design Guide documentation. Also, the names for each control bit in this panel match the names given to specific control bits in the NAU8822 control registers as described in the detailed register map in the NAU8822 Design Guide. The description and function for each of these bits can be found (most easily by doing a text string search) in the Details of Register Operation appendix portion of the NAU8822 device Design Guide.

The GUI Application performs a few additional services not described in the Design Guide. These are described in this section.

🔀 Nuvoton Audio Codec 🛛 8822 Demo			
Device Mode Config Help			
Device Mode Config Help	ing Equalizer Input Limiter/ALC DAC/PLL/Dig Audio Output Path PLL control [REFIMP] 75 KOhm ▼ ** To enable PLL, REFIMP can not be open Circuit. ▼ [PLLEN] Internal PLL Enable FS [Frame Synch] Default (48 KHz) Fixed ▼ [PLLMCLK] MCLK Prescaler Divide by 1 ▼ Auto ▼ [MCLKSEL] IMCLK Prescaler Divide by 2 ▼ Input MCLK (MHz) 12,00000 Desired Fs (KHz) 48,00000 Calculate ** IMCLK = 256° fs -> (in MHz) 12,288000 ** f2 = 4* MCLKSEL* IMCLK -> (in MHz) 12,288000 ** f2 = 4* MCLKSEL* IMCLK -> (in MHz) 98,304000 ** It is preferred to have f2 in range: 90MHz 100 MHz. PLLK 1 (23:18) © PLLN Integer © 08 PLLK 3 (8:0) © 09 Config PLL Jack Detect Bus Switching [ [JACDEN] Jack Detection Enable	Clock Generation Control  Clock Generation Control  CLKJOEN] Master mode: 88xx drives FS, BCLK  CLKJOEN] Master Clock select uses PLL output  BCLKSEL] Divide by 4  (SMPLR] Sample Rate 48KHz  SCEKEN] Slow Timer Clock Enable  Companding Control  (PASSTHRU] ADC Output Routed to DAC Input  ADCM] ADC companding mode off  (DACM] DAC companding mode off  (DACM] DAC companding mode off  (MON0] Choose Mono over Stereo  (ADCPHS) DAC Data Left Phase of Frame  (AIFMT] Audio Data Format DSP/PCM MC	
	[JACDEN] Jack Detection Enable	[AIFMT] Audio Data Format DSP/PCM Mc 💌	
[DACLIMBST] Max Auto Gain Q.0.0 dB [DACLIMTHL] Threshold Ratio 1.0 dB	GPI02  GPI02	[WLEN]     Word Length     16 Bits       [LRP]     Invert I2S data phase       [BCLKP]     Invert BCLK Polarity	

Figure 14: DAC/PLL/DIGITAL AUDIO PANEL OVERVIEW

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#### 13.1 DAC Control

As mentioned in the heading of this section, the details of all of the functions and bits are described in detail in the NAU8822 Design Guide and appendices. The bit names match this documentation, and using a text string search in the Design Guide is a good method to quickly locate specific information about a specific control bit function.

Device Mode Config Help         Demo Path View Device Control Input Path ADC/Filtering Equalizer Input Limiter/ALC DAC/PLL/Dig Audio Output Path Register Map Script         Power Management         F (LDACEN) Left Channel DAC Enable         F (RDACEN) Right Channel DAC Enable         DAC Control         LLDACPLJ Left DAC Duput Polarity Normal         ILDACOS] DAC Duput Polarity Normal         IRDACOS] DAC Duput Polarity Normal         Imput MCLK (MHz)         DAC Volume Control         F (SPTMT) Softmute Enable         F (SPTMT) Softmute Enable         F (DACGAIN) Left Ch DAC Gain \$0.08         PLL control         PLL control         F (BALGGAIN) Left Ch DAC Gain \$0.08         PLL (2318) \$0C         PLL NI Integer \$08	🛞 Nuvoton Audio Codec 📖 8822 Demo 📖 🔲 🗌 🔀			
Power Management       FLL control         Image: IpacExity in the image in the im	Device Made Config Help			
ILDACGAIN] Left Ch. DAC Gain       0.0dB         "It is preferred to have f2 in range: S0MHz - 100 MHz.       [ADCM] ADC companding mode       off         [IDACGAIN] Bitht Ch. DAC Gain       0.0dB       [IDACGAIN] Bitht Ch. DAC Gain       0.0dB	Device Mode Config Help Demo Path View Device Control Input Path ADC/Filteri Power Management [ [LDACEN] Left Channel DAC Enable [ [RDACEN] Right Channel DAC Enable DAC Control [LDACPL] Left DAC Ouput Polarity Normal [RDACPL] Right DAC Output Polarity Normal [DACOS] DAC Oversampling Rate 128X[Best Re] [ AUTOMT] Automute Enable	PLL control [REFIMP] 75 KDPm To enable PLL, REFIMP can not be open Circuit. [PLLEN] Internal PLL Enable FS [Frame Synch] Default (48 KHz) Fixed To [PLLMCLK] MCLK Prescaler Divide by 1 Auto To [MCLKSEL] IMCLK Prescaler Divide by 2 Input MCLK (MHz) 12 000000 Desired Fs (KHz) 48 0000000 Calculate	Clock Generation Control  CLKIDEN] Master mode: 88xx drives FS, BCLK  CLKM] Master Clock select uses PLL output (BCLKSEL] Divide by 4  (SMPLR) Sample Rate 49KH2  SCLKEN] Slow Timer Clock Enable  Companding Control	
Image: Control Contrector Control Control Control Control Contr	[LDACGAIN] Left Ch. DAC Gain <sup>1</sup> 0.0d8          [RDACGAIN] Right Ch. DAC Gain <sup>1</sup> 0.0d8          IF       LDACVU <sup>1</sup> RDACVU          DAC Limiter Control <sup>1</sup> [DACLIMEN] DAC Limiter Enable <sup>1</sup> DACLIMEN] DAC Limiter Enable          [DACLIMATK] Limiter Attack Time <sup>2</sup> 375.0 ue         [DACLIMDCY] Limiter Decay Time <sup>6</sup> 0.0 d8          [DACLIMBST] Max Auto Gain <sup>1</sup> 0.0 d8		[ADCM] ADC companding mode       off         [DACM] DAC companding mode       off         [DACM] DAC companding mode       off         [ICMB8] 8-bit Operation for Companding Mode         Audio Interface Control         [MDND] Choose Mono over Stereo         [ADCPHS] ADC Data Left Phase of Frame         [DACPHS] DAC Data Left Phase of Frame         [AICPHS] DAC Data Left Phase of Frame         [AIFMT] Audio Data Format         DSP/PCM Mc ▼         [WLEN] Word Length         [LRP] Invert I2S data phase	

Figure 15: DAC/PLL/DIGITAL AUDIO PANEL – DAC CONTROL

#### 13.2 Oversampling

DAC and ADC performance is optimized when both are operated at the same oversampling rate. An added feature of the GUI Application is that when either the ADC or DAC oversampling rate is changed, both are changed by the application. If it is desired to make the ADC and DAC operate at different oversampling rates, this can be done using the Register Map control tab.

#### 13.3 PLL Control

The PLL is one of the most powerful and also most difficult to understand features of NAU8822 devices. It is important to understand carefully the detailed information regarding the PLL that is included in the NAU8822 Design Guide.

As mentioned in the heading of this section, the details of all of the functions and bits are described in detail in the NAU8822 design guide and appendices. The bit names match this documentation, and using a text string search in the Design Guide is a good method to quickly locate specific information about a specific control bit function.

🍀 Nuvoton Audio Codec 🛛 8822 Demo		
Device Made Config Help		
	ring Equalizer Input Limiter/ALC DAC/PLL/Dig Audio Output P PLL control [REFIMP] 75 KDrm " To enable PLL, REFIMP can not be open Circuit. [PLLEN] Internal PLL Enable FS [Frame Synch] Default (48 KHz] Fixed T [PLLMCLK] MCLK Prescaler Divide by 1 T Auto T [PLLMCLK] MCLK Prescaler Divide by 2 T Input MCLK (MHz) 12,00000 Desired Fs [KHz] 48,000000 Calculate	Tath       Register Map       Script         Clock Generation Control       Clock Generation Control         Image: Clock Generation Control       Image: Clock Generation Control         Image: Clock Enable       Image: Clock Generation Control         Image: Clock Enable       Image: Clock Enable
[SOFTMT] Sotmute Enable  DAC Volume Control  [LDACGAIN] Left Ch. DAC Gain  0.0dB  [RDACGAIN] Right Ch. DAC Gain  0.0dB  [ LDACVU  DAC Limiter Control	Desired Ps (KP2)         48.000000         Calculate           "* IMCLK = 256" fs> (in MHz)         12.288000           "* f2 = 4" MCLKSEL" IMCLK> (in MHz)         98.304000           ** It is preferred to have f2 in range: S0MHz 100 MHz.           PLLK 1 (23:18)         k0C           PLLK 2 (17:9)         k033           PLLK 3 (8:0)         k0E9	Companding Control  (PASSTHRU) ADC Dutput Routed to DAC Input [ADCM] ADC companding mode off [DACM] DAC companding mode off [CMB8] 8-bit Operation for Companding Mode  Audo Interface Control [MON0] Choose Mono over Stereo
[DACLIMEN] DAC Limiter Enable     [DACLIMATK] Limiter Attack Time \$3750 us     [DACLIMATK] Limiter Attack Time \$6.0 ms     [DACLIMDCY] Limiter Decay Time \$6.0 ms     [DACLIMBST] Max Auto Gain \$0.0 dB     [DACLIMBST] Max Auto Gain \$1.0 dB	Jack Detect Bus Switching JACDEN] Jack Detection Enable GFI02  JACKDIO] Select Jack Detect Pin JACK_DET_1 JACK_UET_1	[MUNO] Choose Wohldows Steled         [ADCPHS] ADC Data Left Phase of Frame         [DACPHS] DAC Data Left Phase of Frame         [AIFMT] Audio Data Format         DSP/PCM Mc▼         [WLEN] Word Length         [LRP] Invert I2S data phase         [BCLKP] Invert BCLK Polarity

Figure 16: DAC/PLL/DIGITAL AUDIO PANEL – PLL CONTROL

#### 13.4 REFIMP

The PLL cannot be enabled unless the reference impedance is enabled. This is part of the power management functionality to help minimize power consumption when the device is put into a non-operating mode.

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#### 13.5 FS (Frame Sync)

This is the pin name and bit name for the Frame Sync function. The FS rate is normally the same as actual sampling rate intended for the device. However, FS is simply the rate at which samples are transmitted over the I2S or PCM digital audio bus. It is not inherent in the device that the ADC and DAC are actually also operating at the FS sample rate.

The FS rate can be left as Default, or selected to be Custom. In either case, this section of the PLL Control features will set up the PLL to operate the ADC and DAC at the desired sample rate. If the device is set to be the bus master, then FS will be exactly the specified sample rate.

If the device is in "slave" mode, best performance will be achieved when the FS signal is phase locked with the ADC and DAC and operating at the same exact sampling rate. The default configuration for the PLL is to convert a 12.000MHz external MCLK into an internal 12.288MHz signal for the internal IMCLK signal, which sets a 48.000kHz sample rate for both the ADC and DAC. The ADC and DAC always have the same sampling rate.

#### 13.6 Clock Prescalers

Choosing the optimum prescale values and PLL coefficients is a complex process linked to the details of the configuration and desired operation of the end-product system. As an aid to this process, the GUI Application can be asked to automatically determine the best PLL parameters.

However, this needs to be checked against the instructions in the Design Guide, because the automatic calculation may not guess correctly the entire desired configuration. As a further aid, the clock prescalers can be set to "Fixed" or "Auto." If set to "Auto," the Calculate function will make its best guess how to set the prescaler value. If set to "Fixed," the Calculate function will use the prescaler value set in this control panel.

## 13.7 Config PLL

This radio button causes all manually entered or automatically determined PLL parameters to be loaded into the PLL control registers. No change to the PLL control registers is made until the button is activated.

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## 13.8 Digital Audio Control

vice Mode Config Help		
emo   Path View   Device Control   Input Path   ADC/Filt - Power Management	eting   Equalizer   Input Limiter/ALC DAC/PLL/Dig Audio   Output PLL control (REFIMP) 75 KOhm " To enable PLL, REFIMP can not be open Circuit. [ PLLEN] Internal PLL Enable T FS (Frame Synch] Default (48 KHz)	Path   Register Map   Script   Clock Generation Control CLKIOEN   Master mode: 88xx drives FS, BCLK (CLKM] Master Clock select uses PLL output (BCLKSEL) Divide by 4
[LDACPL] Lett DAC Duput Polarity       Normal         [RDACPL] Right DAC Dutput Polarity       Normal         [DACOS] DAC Oversampling Rate       128K/Best Re         [IDACOS] Rate       128K/Best Re <td>Fixed         ·····         [PLLMCLK] MCLK Prescaler         Divide by 1         ✓           Auto         ·····         [MCLK SEL]         IMCLK Prescaler         Divide by 2         ✓           Input MCLK (MHz)         12.000000         Desired Fs (KHz)         48.000000         Calculate           ***         IMCLK = 256* fs →&gt; (in MHz)         12.288000         *** fz = 4* MCLKSEL* IMCLK →&gt; (in MHz)         98.304000           ***         It is preferred to have fz in range: 90MHz → 100 MHz         ***         100 MHz</td> <td>[SMPLR] Sample Rate 49KHz [SCLKEN] Slow Timer Clock Enable Companding Control [PASSTHRU] ADC Output Routed to DAC Input [ADCM] ADC companding mode off</td>	Fixed         ·····         [PLLMCLK] MCLK Prescaler         Divide by 1         ✓           Auto         ·····         [MCLK SEL]         IMCLK Prescaler         Divide by 2         ✓           Input MCLK (MHz)         12.000000         Desired Fs (KHz)         48.000000         Calculate           ***         IMCLK = 256* fs →> (in MHz)         12.288000         *** fz = 4* MCLKSEL* IMCLK →> (in MHz)         98.304000           ***         It is preferred to have fz in range: 90MHz → 100 MHz         ***         100 MHz	[SMPLR] Sample Rate 49KHz [SCLKEN] Slow Timer Clock Enable Companding Control [PASSTHRU] ADC Output Routed to DAC Input [ADCM] ADC companding mode off
[RDACGAIN] Right Ch. DAC Gain	PLLK 1 (23:18) <b>xOC</b> PLLN Integer <b>xO8</b> PLLK 2 (17:9) <b>xO33</b> PLLK 3 (8:0) <b>xOE9 Config PLL</b>	[DACM] DAC companding mode off     [CMB8] 8-bit Operation for Companding Mode     Audio Interface Control     [MOND] Choose Mono over Stereo     [ADCPHS] ADC Data Left Phase of Frame
[DACLIMATK] Limiter Attack Time ♥ 3750 us [DACLIMDCY] Limiter Decay Time ♥ 6.0 ms [DACLIMBST] Max Auto Gain ♥ 0.0 dB [DACLIMTHL] Threshold Ratio ♥ 1.0 dB	Jack Detect Bus Switching JACDEN] Jack Detection Enable GFI02	□ [DACPHS] DAC Data Left Phase of Frame         [AIFMT] Audio Data Format       □ SP/PCM Mc ▼         [WLEN] Word Length       16 Bits         □ [LRP] Invert I2S data phase         ☑ [BCLKP] Invert BCLK Polarity

Figure 17: DAC/PLL/DIGITAL AUDIO PANEL – DIGITAL AUDIO CONTROL

#### 13.9 Clock Generation Control

The Clock Generation Control block sets up the relationship of the ADC and DAC to the FS and BLCK digital audio data bus signals. It is important to understand carefully the detailed information regarding this, which is in the PLL description in the NAU8822 Design Guide.

As mentioned in the heading of this section, the details of all of the functions and bits are described in detail in the NAU8822 design guide and appendices. The bit names match this documentation, and using a text string search in the Design Guide is a good method to quickly locate specific information about a specific control bit function.

#### 13.10 CLKIOEN Master Mode

Selecting this control bit will cause NAU8822 device to drive the FS and BCLK pins as the master of the I2S or PCM digital audio data bus. If this is not selected, the NAU8822 device will be the slave of the digital audio data bus and the FS and BLCK pins will be used as inputs to the NAU8822 device.

#### 13.11 CLKM Master Clock

Selecting this control bit will cause the NAU8822 device to use the PLL output as the input to its Master Clock (IMCLK) Prescaler. If this is not selected, the IMCLK Prescaler will use the signal on the external MCLK pin as its input.

#### 13.12 BCLKSEL

This has an effect only if the NAU8822 device is the audio bus master. When the device is the audio bus master, the internal IMCLK rate will be divided by the factor set in this panel, and this will become the rate of the FS signal on the FS output pin.

#### 13.13 SMPLR Sample Rate

This control value does NOT change the sampling rate in any way. The SMPLR value exists because the digital signal processing algorithms have no information to know the actual physical sample rate. This is determined by the external MCLK frequency. The only function of the SMPLR value is to scale the ADC high pass filter coefficients to be compensated for the actual sample rate of the system. If SMPLR is set correctly, then the high pass filter cutoff frequency will be the desired value as listed in the NAU8822 Design Guide. The Equalizer cutoff frequencies have no such compensation. The nominal Equalizer cutoff frequencies in the design guide are for a 48kHz sample rate. For example, if the actual sample rate is 24kHz, then the Equalizer cutoff frequencies will be one half of the values listed for 48kHz in the Design Guide.

#### 13.14 Companding Control

Companding implements a non-linear compression/decompression of the audio signal as explained in the NAU8822 device Design Guide. Most applications for the NAU8822 will not use this feature.

#### 13.15 PASSTHRU

When enabled, the pass-through mode causes data from the left and right ADC outputs to flow directly into the digital signal processing chain for the DAC output section. In this mode, data on the DACIN pin are ignored and replaced with data from the corresponding ADCs. ADC data continues to be output on the ADCOUT pin.

#### 13.16 Audio Interface Control

These controls affect how audio data are formatted and input or output on the serial digital audio bus and are explained in the device Design Guide. The "MONO" control does not affect formatting. This feature may be useful when only the left ADC is being used, and it is important to guarantee that the right channel information is exactly zero.

#### 13.17 Jack Detect Bus Switching

These controls affect various options related to the jack detection feature as detailed in the device Design Guide. The idea of jack detection is that a logic level change can be sensed on one of the GPIO pins, and this change will then enable/disable specified outputs and power control blocks.

## 14 Output Path Control Panel

This Control Tab gives access to the various controls and settings for the analog outputs, and the analog mixers that work together with the analog outputs.

The operation of each of these functions is explained in detail in the NAU8822 device Design Guide documentation. Also, the names for each control bit in this panel match the names given to specific control bits in the NAU8822 control registers as described in the Design Guide detailed register map. The description and function for each of these bits can be found (most easily by doing a text string search) in the Details of Register Operation appendix portion of the NAU8822 device Design Guide.

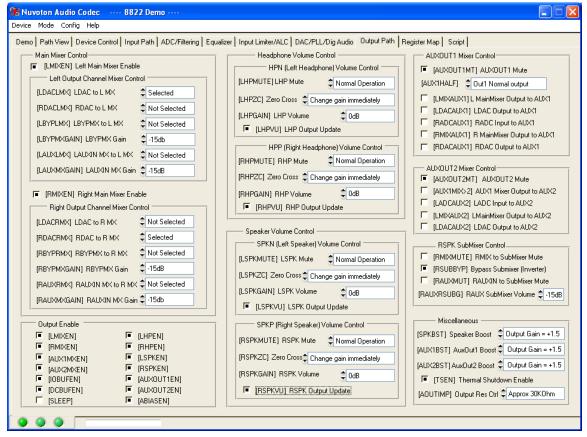


Figure 18: OUTPUT PATH CONTROL PANEL

## **15 Register Map Control Panel**

When the Register Map control tab is selected, all of the bits in all of the registers will be displayed corresponding to the current settings in the device. In the case of any write-only bits, or in the case when the control bus is write-only (register values cannot be read back by software), the values displayed are values that are remembered by software, and that should be the same as the actual values used by the device.

If there is ever any uncertainty whether or not the values in the display truly reflect the values in the physical device, and if the control bus allows reading from the device, the display values can be refreshed by selecting the "Read All and Update" radio button in the "Audio Codec Register Control" panel. This will read all of the registers from the device, and all bits values that can be read from the device will then be updated in the GUI display to be the same.

emo   Path View   Devi	ce Control	Input Path	ADC/Fi	iltering   E	qualizer	Input Limit	er/ALC   I	DAC/PLL/	'Dig Audio	Output F	Path Regi	ister Map   9	Script	]
			WA	U882	22 Re	giste	r Map	þ						Audio Codec Register Control
	Hex Addr	Dec Addr	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex Val		
Software_Reset	00	0	0	0	0	0	0	0	0	0	0	000		Address x00 Read
Power_Management_1	01	1	1	1	1	1	0	1	1	0	1	1ED		
Power_Management_2	02	2	1	1	0	1	1	1	1	1	1	1BF		Value ×000 Write
Power_Management_3	03	3	1	1	1	1	1	1	1	1	1	1FF		
Audio_Interface	04	4	1	0	0	0	1	1	0	0	0	118		Read All and Update
Companding	05	5	0	0	0	0	0	0	0	0	1	001		
Clock_Control_1	06	6	1	0	1	0	0	1	0	0	1	149		
Clock_Control_2	07	7	0	0	0	0	0	0	0	0	0	000		
GPIO	08	8	0	0	0	0	0	0	0	0	0	000		
Jack_Detect_1	09	9	0	0	0	0	0	0	0	0	0	000		
DAC_Control	QA	10	0	0	0	0	0	1	1	0	0	00C		
Left_DAC_Volume	OB	11	1	1	1	1	1	1	1	1	1	1FF		
Right_DAC_Volume	00	12	1	1	1	1	1	1	1	1	1	1FF		
Jack_Detect_2	0D	13	0	0	0	0	0	0	0	0	0	000		
ADC_Control	0E	14	1	0	0	0	0	1	0	0	0	108		
Left_ADC_Volume	OF	15	1	1	1	1	1	1	1	1	1	1FF		
Right_ADC_Volume	10	16	1	1	1	1	1	1	1	1	1	1FF		
EQ1-low_self	12	18	1	0	0	1	0	1	1	0	0	12C		
EQ2-peak_1	13	19	0	0	0	1	0	1	1	0	0	02C		
EQ3-peak_2	14	20	0	0	0	1	0	1	1	0	0	02C		
EQ4-peak_3	15	21	0	0	0	1	0	1	1	0	0	02C		
EQ5-high-self	16	22	0	0	0	1	0	1	1	0	0	02C		
DAC_Limiter_1	18	24	0	0	0	1	1	0	0	1	0	032		
DAC Limiter 2	19	25	Π	n	n	n	n	n	n	Π	n	000	1	

Figure 19: REGISTER MAP CONTROL PANEL OVERVIEW

#### 15.1 Register Map Bit Control

In this view, any bit can be selected and altered. The changed value will be written to the actual device control register by hitting the "enter" or "return" key on the PC keyboard, or by simply moving the cursor to a different bit field. When any of these completing actions is done, the hexadecimal value column entry for that register will also be updated.

In this view, hexadecimal values may also be directly changed in the "Hex Val" column. The changed value will be written to the actual device control register by hitting the "enter" or "return" key on the PC keyboard, or by simply moving the cursor to a different bit field.

#### 15.2 Register Map Update Bits (write-only bits)

The bits known as "update bits" are commands to the device that are not physically stored in the device control registers. These bits are displayed in the Register Map view as the present user preference. This preference may be altered at any time. When writing the device from the Register Map view, the displayed preferences for each update bit will be used when writing the respective register which contains that update bit.

			WA	U882	22 Re	giste	r Map	D						Audio Codec Register Control
	Hex Addr	Dec Addr	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex Val		
Software_Reset	00	0	0	0	0	0	0	0	0	0	0	000		Address ×00 Read
Power_Management_1	01	1	1	1	1	1	0	1	1	0	1	1ED		
Power_Management_2	02	2	1	1	0	1	1	1	1	1	1	1BF		Value x000 Write
Power_Management_3	03	3	1	1	1	1	1	1	1	1	1	1FF		
Audio_Interface	04	4	1	0	0	0	1	1	0	0	0	118		Read All and Update
Companding	05	5	0	0	0	0	0	0	0	0	1	001		
Clock_Control_1	06	6	1	0	1	0	0	1	0	0	1	149		
Clock_Control_2	07	7	0	0	0	0	0	0	0	0	0	000		
GPIO	08	8	0	0	0	0	0	0	0	0	0	000		
Jack_Detect_1	09	9	0	0	0	0	0	0	0	0	0	000	1	
DAC_Control	0A.	10	0	0	0	0	0	1	1	0	0	00C	1	
Left_DAC_Volume	0B	11	1	1	1	1	1	1	1	1	1	1FF	1	
Right_DAC_Volume	0C	12	1	1	1	1	1	1	1	1	1	1FF		
Jack_Detect_2	0D	13	0	0	0	0	0	0	0	0	0	000		
ADC_Control	0E	14	1	0	0	0	0	1	0	0	0	108		
Left_ADC_Volume	0F	15	1	1	1	1	1	1	1	1	1	1FF		
Right_ADC_Volume	10	16	1	1	1	1	1	1	1	1	1	1FF		
EQ1-low_self	12	18	1	0	0	1	0	1	1	0	0	12C		
EQ2-peak_1	13	19	0	0	0	1	0	1	1	0	0	02C		
EQ3-peak_2	14	20	0	0	0	1	0	1	1	0	0	02C		
EQ4-peak_3	15	21	0	0	0	1	0	1	1	0	0	02C		
EQ5-high-self	16	22	0	0	0	1	0	1	1	0	0	02C		
DAC_Limiter_1	18	24	0	0	0	1	1	0	0	1	0	032		
DAC Limiter 2	19	25	n	n	n	n	n	n	n	Π	Π	000		

Figure 20: REGISTER MAP CONTROL DETAILS

#### 15.3 Audio Codec Register Control

This panel gives simple hexadecimal read and write control to all of the registers in the device. Both the register address and register data are in hexadecimal format. If the control bus is set up in a write-only format, then reading the device is not possible, and attempts to read the device will result in an error message from the GUI Application software.

## **16 Script Control Panel**

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In all of the other Control Tabs, any time sequencing of operations to the device is automatic. This panel enables creating specific sequences of any specified register write operations. Only the commands in the script are executed, so the codec may already be configured using the other controls and panels. Then the script will modify what is already in the codec. This simplifies the script, because the script does not necessarily have to set up the entire codec.

#### 16.1 Script Panel Structure

The main body of this panel contains the script to be executed, and at the top of the panel are three the radio button controls. The "Run" command will cause the entire script to be executed at that time. The "Save" command will save the current script into short term system memory (but not as a file). The "Load" command will recall an existing script from short term memory.

🗱 Nuvoton Audio Codec 🛛 8822 Demo
Device Mode Config Help
Demo   Path View   Device Control   Input Path   ADC/Filtering   Equalizer   Input Limiter/ALC   DAC/PLL/Dig Audio   Output Path   Register Map Script
''0x-1 = mmm'' means Delay mmm msec run load save
This is a comment     This is a comment     This is a comment     Wait [1000ms]     Wait [1000ms]     Wait [1000ms]     Wait [1000ms]     Wait [1000ms]     Wait [1000ms]     Wait = 0x000  ; MCLK must be running for output register changes to be effective     Wait = 0x000  ; MCLK must be running for output register changes to be effective     Wait = 0x000  ; MCLK must be running for output register changes to be effective     Wait = 0x000  ; MCLK must be running for output register changes to be effective     Wait = 0x000  ; MCLK must be running for output register changes to be effective     Wait = 0x000  ; MCLK must be running for output register changes to be effective     Wait as long as possible to charge at the slow charging rate     ; thy to wait at least two seconds     Wert = 2000 ; wait at least two seconds for slow charging to partially finish     Port = 00000 ; where the wfit at least two seconds
0x31 = 0x002 ; change tie-off to 1k-ohm for faster charging ; this will make a click, however, ; the longer you wait before this time, the smaller the click 0x1 = 1000 ; wait at least one second for faster charging to begin working 0x01 = 0x007 ; set REFIMP = 3k for faster charging 0x1 = 1000 ; wait at least one second for faster charging to finish ; ; now turn on the line-to-aux output power control and analog paths
0x01 = 0x1CF       ; enable power Aux mixers, I/O buffers, and refimp=80k         0x02 = 0x030       ; enable power for input boost mixers         0x03 = 0x180       ; enable aux output amplifiers         0x2F = 0x050       ; set up left input boost mixer for LLIN=0.0dB gain, and boost=0dB         0x31 = 0x017       ; set up right input boost mixer for RLIN=0.0dB gain, and boost=0dB         0x31 = 0x017       ; set up right input boost mixer for RLIN=0.0dB gain, and boost=0dB         0x33 = 0x004       ; unmute Aux2 mixer output and enable path to left input boost mixer         0x38 = 0x004       ; unmute Aux1 mixer output and enable path to right input boost mixer

Figure 21: SCRIPT CONTROL PANEL

#### 16.2 Script Panel Syntax

The script panel has a simple syntax. Each line contains a register address in hexadecimal form, followed by an equals sign, then followed by another hexadecimal value to be written into that register. The hexadecimal values are the same 9-bit long values as are shown in the Register Map view and device register level documentation.

Lines are separated by carriage returns (new line or "enter" on the PC keyboard). Comments are limited to one line and are any text preceded by a semicolon. ηυνοτοη

A time delay can be inserted by using negative 1 (hexadecimal 0x-1) as the register address followed by an equal sign and then an integer decimal value. In this case, the script program will pause for the duration of the decimal value in milliseconds.

## 17 Daughter Card System

The daughter card is the small PCB mounted onto a socket connector on the main EVB motherboard, and this contains the device being evaluated. This arrangement enables a single EVB hardware and software system to support testing of a very wide range of Nuvoton audio products in a consistent, stable, and easy to use environment.

### 17.1 Changing Daughter Cards

If it is desired to use a different daughter card on the system, it is best to first completely remove all power connections to the EVB. Then, simply remove the existing daughter card and insert the new daughter card in the same location.

IMPORTANT: When inserting the new daughter card, make certain that the Pin #1 alignment matches the Pin #1 location indicated on the motherboard. Also, be careful to mount the daughter card so that all four rows of connectors are in fact connected. It is possible to offset the daughter card horizontally so that some rows are connected and other rows are not connected.

A good technique to insert a new daughter card is to hold the card at an angle so that it can be seen clearly visually that one row is completely and correctly aligned. After this first row begins to become connected, then in a rolling or rotating motion, swing the daughter card so that it is parallel with the motherboard and push to engage all of the other connectors.

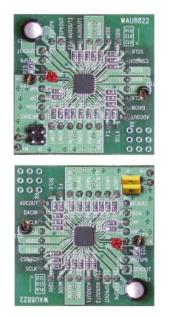
### 17.2 NAU8822 Daughter Card

The new style NAU8822 daughter card includes series resistors on all of the low-current analog and digital signal paths. Most are zero-ohm resistors, but some have a small value to optimize clock signal integrity. A schematic diagram of the daughter card is included for reference.

The series resistors make it easy to modify the daughter card for experimentation, eliminating the need to cut actual foil traces on the PCB. Additionally, test points are included for:

- \* digital ground (convenient for attaching test equipment)
- \* analog ground (important for precise analog performance measurement)
- \* Vref (AC and DC voltage reference used by the device)

A built-in microphone is also included on the new style daughter card. This can be connected by moving the two left microphone path jumpers, J11 and J14, from the normal location on the EVB onto the J1 and J2 pin-pairs on the daughter card as shown in the picture below. The Demo panel option for microphone input will now operate using the built-in microphone.



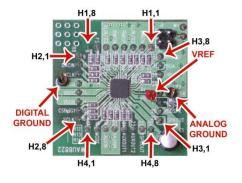


Figure 22: NAU8822 DAUGHTER CARD; AS ORIENTED ON EVB; WITH MIC ENABLED

## **18 Jumpers and Connectors**

The EVB motherboard has many jumpers and connectors for maximum flexibility. These enable various combinations of internal/external power, simplify power measurements, change audio paths, change external command and control paths, and enable external streaming of audio data to and from the device on the daughter card.

#### 18.1 Power Related Connectors and Options

The main power supply for the EVB and each regulated supply that supports the daughter card can be replaced with an external power supply connection. This makes it easy to test alternative power configurations.

WARNING: The EVB is carefully designed to keep built-in power supply combinations within safe limits for the device on the daughter card. When using external power supply sources, extreme care must be used to make certain that the maximum power supply limits and power supply combination voltages on the device under test are never exceeded. Excessive power or incorrect power combinations may destroy both the daughter card and the motherboard.

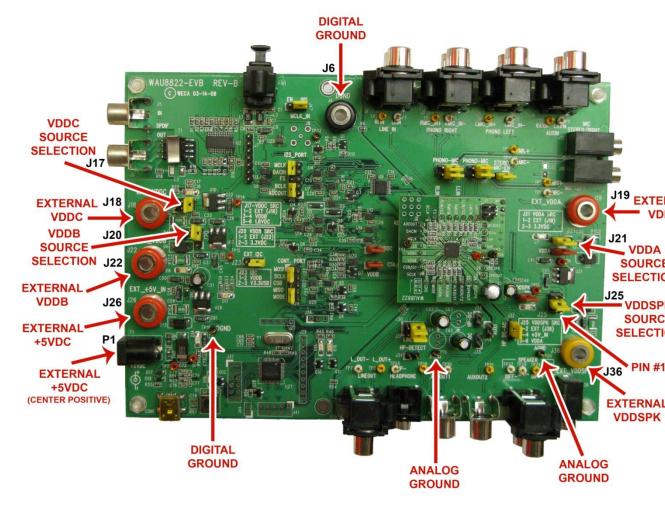


Figure 23: POWER RELATED CONNECTORS AND OPTIONS

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### **19.1** Summary of Power Options and Limits

IMPORTANT: Physical orientation of the various power selection jumpers is NOT the same. Each jumper must be examined carefully to determine its Pin #1 designator and orientation. The connector Pin #1 is marked with a white square in the silkscreen pattern on the PCB.

Connector Name	Signal Name	Supply Range and Limits	Option Jumper Name	Power optioning description Important: Note carefully the differing pin #1 positions on each jumper
CON1	USB	USB host limited	n/a	Power is normally supplied entirely from the USB host. Series diodes will substitute power from the greater of either P1 or from J26 if either source is greater than 5Vdc from the USB host.
P1	5vDC Center Pin = Positive (+V)	0.0Vdc to 5.5Vdc	n/a	Note: There is no jumper for this option. Series diodes pass power from P1 if this voltage is greater than 5Vdc coming from USB
J6	DGND	0V (digital ground)	n/a	n/a
J18	EXT_VDDC	1.6Vdc to 3.6Vdc	J17	Pin 1-2 shorted selects External VDDC via J18 Pin 3-4 shorted selects VDDC=VDDB Pin 5-6 shorted selects VDDC=1.8Vdc
J19	EX_VDDA	2.5V to 3.6V VDDA must be ≥ VDDC	J21	Pin 1-2 shorted selects external VDDA via J19 Pin 2-3 shorted selects VDDA = 3.3Vdc
J22	EXT_VDDB	1.8V to 3.6V VDDB must be ≥ VDDC	J20	Pin 1-2 shorted selects External VDDB via J22 Pin 2-3 shorted selects VDDB=3.3Vdc
J26	EXT_+5V_IN	0.0Vdc to 5.5Vdc	n/a	Note: There is no jumper for this option. Series diodes pass power from J26 if this voltage is greater than 5Vdc coming from USB
J36	EX_VDDSPK	2.5V to 5.0V	J25	Pin 1-2 shorted selects external VDDSPK via J36 Pin 3-4 shorted selects built-in 5.0Vdc Pin 5-6 shorted selects VDDSPK = VDDA

Default factory configuration highlighted in color

#### Table 1: POWER OPTIONS

#### 19.2 Main 5Vdc Power

All power is usually supplied to the NAU8822-EVB USB interface via the USB connector. It should be noted that the voltage supplied via USB is nominally 5Vdc. However, this voltage supplied by the external USB host may be significantly less, especially if driving a loudspeaker at high volume using the device on the daughter card.

With most USB host devices and USB cables, it is not possible to achieve the full rated 1-Watt of loudspeaker power using only USB as the power source. Additionally, long or poor quality USB cables can cause the EVB to operate unreliably. The USB cable used with the EVB should be a high quality product and not longer than 1-meter.

If the primary purpose to use alternative power is to drive the speaker output to the full rated power, it is preferred to simply substitute an external supply for VDDSPK via J36. EVB operation is simpler if the main 5Vdc power other than for VDDSPK is supplied from the USB host.

#### 19.3 Power LINK Jumpers

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Each power rail between the motherboard and the daughter card passes through a Link jumper. If this jumper is removed, the power connection is completely disconnected. These jumpers are useful as a point to measure power rail supply current, or to substitute external power directly to the device on the daughter card with no connection at all to any component on the motherboard.

Jumper	Supply Name	Jumper Selection
LINK2	VDDC	Removing jumper completely disconnects DC path for VDDC from motherboard
LINK3	VDDA	Removing jumper completely disconnects DC path for VDDA from motherboard
LINK4	VDDB	Removing jumper completely disconnects DC path for VDDB from motherboard
LINK5	VDDSPK	Removing jumper completely disconnects DC path for VDDSPK from motherboard

On newer revisions of the EVB motherboard, the LINK jumpers are a red color plastic.

#### Table 2: POWER LINK JUMPERS

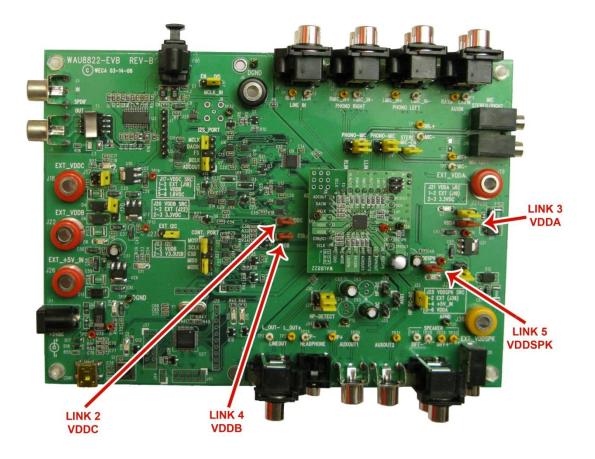


Figure 24: POWER LINK JUMPERS

## 20 Analog Inputs for NAU8822

The analog inputs connect via passive components to pins on the daughter card. All paths are AC coupled, and passive components are typically transparent (such as zero-ohm resistors and RF bypass capacitors) at audio frequencies. Some paths may also pass through a jumper selection as outlined in this documentation.

In most cases, the analog inputs may be used intuitively without the need to know further details of the actual path through the EVB. The EVB schematic is included and readily available if further detailed understanding is needed.

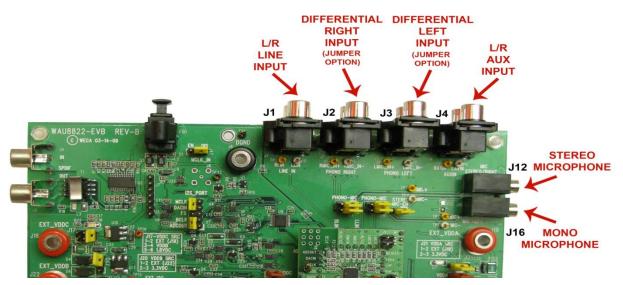


Figure 25: ANALOG INPUTS

Jack Name	Connector	Daughter card Pin	Jumper To Connect	Function and Signal Name / Device Pin Number on NAU8822
J1	RCA jack - top	H1,3	None	Left Line Level Input: LLIN: Pin #3
Line In	RCA jack - bottom	H1,6	None	Right Line Level Input: RLIN, Pin #6
J2	RCA jack - top	H1,5	J10: 2-3	Right Inverting Mic Input: RMICN, Pin #5
Phono Right	RCA jack - bottom	H1,4	J12: 2-3	Right non-Inverting Mic In: RMICP, Pin #4
J3	RCA jack - top	H1,2	J11: 2-3	Left Inverting Mic Input: LMICN, Pin #2
Phono Left	RCA jack - bottom	H1,1	J14: 2-3	Left non-Inverting Mic In: LMICP, Pin #1
J4	RCA jack - top	H4,3	None	Left Auxiliary Line Input: LAUXIN, Pin #19
Auxin	RCA jack - bottom	H4,4	None	Right Auxiliary Line Input: RAUXIN, Pin #20
J12	3.5mm jack - tip	H1,4	J13: 1-2	Right non-Inverting Mic In: RMICP, Pin #4
Stereo Mic /	3.5mm jack - ring	H1,1	Link1=on	Left non-Inverting Mic In: LMICP, Pin #1
Right Mic	3.5mm jack - sleeve	H1,5	J10: 1-2	Right Inverting Mic Input: RMICN, Pin #5
J16	3.5mm jack - tip	H1,1	J14: 1-2	Left non-Inverting Mic In: LMICP, Pin #1
Left Mic	3.5mm jack - ring	None	None	No connection
	3.5mm jack - sleeve	H1,2	J11: 1-2	Left Inverting Mic Input: LMICN, Pin #2

Default factory configuration highlighted in color

#### Table 3: ANALOG INPUTS

## 21 Analog Outputs for NAU8822

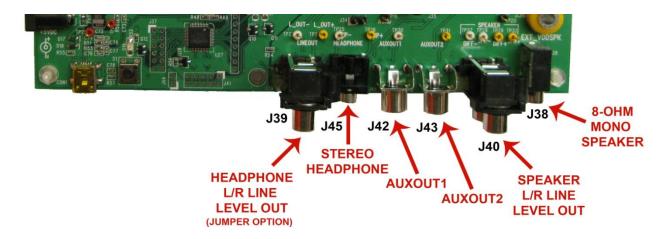
The analog outputs connect via passive components to pins on the daughter card. All paths are AC coupled, and passive components are typically transparent (such as zero-ohm resistors and RF bypass capacitors) at audio frequencies. Some paths may also pass through a jumper selection as outlined in this documentation.

In most cases, the analog outputs may be used intuitively without the need to know further details of the actual path through the EVB. The EVB schematic is included and readily available if further detailed understanding is needed.

Jack Name	Connector	Daughter card Pin	Jumper To Connect	Function and Signal Name / Device Pin Number on NAU8822
J39 Line Out	RCA jack - top RCA jack - bottom	H1,3 H1,6	J30: 1-2 J31: 1-2	Left Line Level Output: LHP: Pin #30 Right Line Level Output: RHP, Pin #29
J45 Headphone	3.5mm jack - tip 3.5mm jack - ring 3.5mm jack - sleeve	H1,5 H1,4 n/a	J30: 2-3 J12: 2-3 J32: 1-2	Left Headphone Output: LHP, Pin #30 Right Headphone Output: RHP, Pin #29 Sleeve connected to Analog Ground
J43 Auxout1	RCA jack (single)	H4,5	None	Auxiliary Output #1: AUXOUT1, Pin #21
J42 Auxout2	RCA jack (single)	H4,6	None	Auxiliary Output #2: AUXOUT2, Pin #22
J40 Spkr LineOut	RCA jack - top RCA jack - bottom	H3,1 H4,7	None None	Left Speaker line out: LSPKOUT, Pin #25 Right Speaker line out: RSPKOUT, Pin #23
J38 Speaker Out	3.5mm jack - tip 3.5mm jack - sleeve	H4,7 H3,1	None None	Mono-speaker right:RSPKOUT, Pin #23Mono-speaker left:LSPKOUT, Pin #25

Default factory configuration highlighted in color

Table 4: ANALOG OUTPUTS





### 21.1 Analog Output Options for NAU8822

Several functional feature options are available related to the analog outputs.

Jumper and Label on Motherboard	Jumper Selection
J34 HP-DETECT	Installing this jumper on the motherboard connects the LLIN/GPIO2 pin of the NAU8822 to a pullup resistor tied to VDDB, and shorted to a lower voltage by the headphone jack in the state when nothing is inserted in the headphone jack.
	Care should be taken to remove J34 if the headset detection function is not needed or being evaluated. This otherwise creates a large DC offset for the LLIN signal, and may give the appearance the LLIN input is malfunctioning.
J32	"AC" default position, connecting pins 1-2. Headphone is tied to analog ground and should be AC coupled (J33 and J35 not-installed on motherboard).
HP_DC-AC	"DC" position, connecting pins 2-3. Headphone is tied to AUXOUT2 which should be configured as a virtual ground, and in which case the headphone may be DC coupled.
J33 HP-DC	Installing J33 causes the left headphone connector output to be DC coupled to the LHP headphone output of the NAU8822.
J35 HP-DC	Installing J35 causes the left headphone connector output to be DC coupled to the LHP headphone output of the NAU8822.
H5 (header) AUX1	This is intended as the two-pin connection for an external ear speaker load, such as a telephony 150-ohm receiver transducer. This is not a jumper option location and no jumper should ever be installed at this location.
J30 LINE-HP	Position 1-2 Left Line_Out select and Position 2-3 selects Left HPOut (Left headphone out)
J31 LINE-HP	Position 1-2 Right Line_Out select and Position 2-3 selects Right HP+_Out (Right headphone out)

Default factory configuration highlighted in color

Table 5: ANALOG OUTPUT OPTIONS

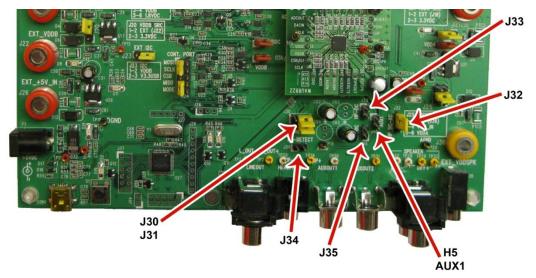


Figure 27: ANALOG OUTPUT OPTIONS

## 22 Headphone Detect

The NAU8822 can detect the presence of a headphone by sensing a logic level DC voltage change at its GPIO pins. On the motherboard, an option exists to connect the GPIO function of the Left Line input (LLIN/GPIO2) to a 33k-ohm pullup resistor to VDDB. This connection is made by inserting J34 onto the motherboard.

IMPORTANT: If jumper J34 is left inadvertently on the motherboard, the LLIN input will have a large DC offset voltage when no headphone is inserted into the headphone jack. This will cause this input to have a very limited voltage range and unexpected clipping owing to the large DC offset voltage. If it is desired to use the LLIN input as a signal input, J34 should be removed from the motherboard. Other GPIO pins can be selected for headphone jack detection in the same way by setting up the appropriate software configuration.

#### 22.1 Headphone Virtual Ground

The headphone is normally connected to analog ground in the default configuration. An alternative configuration is to use Auxout2 as a "virtual ground" for the headphone. This is done by moving jumper J32 to short the pin 2-3 position. In this mode of operation, the Auxout2 output is normally set to Mute, but enabled to output the same DC voltage output as the headphone output pins. When this is done, AC coupling of the headphone output drivers is not necessary.

IMPORTANT: If jumper J32 is left inadvertently in the pin 2-3 position, unexpected results will happen depending on how Auxout2 is being used. The most common unexpected result is for Auxout2 to be in the high impedance state (not powered). In this case, the headphones will have no ground. Stereo signals will partially cancel, and an unusual mix in the headphones will result.

### 22.2 DC Coupled Headphone Outputs

The headphone outputs may optionally be DC coupled by inserting a jumper on the motherboard. Inserting J33 will cause the left headphone output to be DC coupled, and inserting J35 will cause the right headphone output to be DC coupled.

### 22.3 Ear Speaker Mode

This mode is typically used in telephony applications when the ear speaker transducer (such as a standard 150-ohm impedance receiver transducer) is driven as a floating monaural load. For this application, the ear speaker transducer would be placed across the two pins of the H5 two-pin header on the motherboard.

## 23 Digital Audio Using the NAU8822

The NAU8822 supports digital audio input and output using I2S or PCM (DSP Mode) serial data communications. These various paths may be used directly, or as a convenience, the motherboard provides resources to convert these formats into commonly used external formats such as S/PDIF and USB audio. The connectors supporting these digital audio options are listed and discussed in this section.

### 23.1 NAU8822 Master Clock Requirement

The NAU8822 requires a high frequency master clock supplied via its MCLK pin to operate either the ADC or DAC blocks inside the NAU8822. For the best audio quality, the master clock should be phase locked in an integer ratio relationship with the sample clock (FS signal) of the external source. Further, the internal IMCLK signal clock rate to the ADC and DAC should be exactly 256 times the FS sample rate. This is explained in the Design Guide for the NAU8822.

### 23.2 Master Clock Selection

Many options are available for supplying a suitable MCLK under control of the W681308 microcontroller and using the extensive MCLK management resources provided by the NAU8822. The NAU8822 also includes a fractional-N PLL (phase locked loop) that can create a suitable internal MCLK signal using a wide range of available signals on its MCLK pin.

When using S/PDIF as an audio source, the S/PDIF transceiver provides a suitable MCLK.

When using USB, the W681308 provides the 12.000MHz USB clock as the MCLK signal.

An external MCLK clock may be supplied directly to the device on the daughter card via TP33. To select this option, the J47 jumper selector must be moved from the default Pin 2-3 position to the Pin 1-2 position. MCLK may also be supplied to J8, however, this SMB style connector is not populated on the motherboard.

### 23.3 Frame Sync (Sample Rate Clock)

The FS signal is synonymous with the sample rate of the digital audio data bus. This signal does NOT in any way determine the ADC and DAC sample rate. For best audio quality, the master clock inside the NAU8822 should be set up so that the ADC and DAC are running phase locked at exactly the same sample rate as the FS signal. The FS signal is provided by the audio bus master. The W681308 microcontroller determines which device is the bus master and sets up the NAU8822 clock subsystem accordingly.

### 23.4 Bit Clock (BLCK)

The bit clock is a medium speed clock that initiates transfer of each audio bit in the I2S or PCM audio data stream. This clock is synchronous with the Frame Sync and provided by the same bus master that supplies the Frame Sync signal. The only requirement for the bit clock is to have a sufficient number of clock-edge transitions to transfer all of the audio data bits in the audio sample before the next Frame Sync transition occurs.

# 24 Digital Audio Input

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There are three methods to stream digital audio from the motherboard or external devices into the NAU8822 audio data interface. These paths are set up using the appropriate connectors, and also, using the W681308 microcontroller managed by the GUI Application software to set up the paths accordingly.

### 24.1 Formatted Digital Audio

A serial audio transceiver that supports AES/EBU, UEC958, S/PDIF, EIAJ CP340/1201 serial digital audio formats is on the motherboard. Audio to the transceiver may be connected via either the S/PDIF optical coupler, S/PDIF RCA jack, or connected directly through the J7 header.

The transceiver and serial audio paths between the transceiver and the device on the daughter card are managed by the W681308 microcontroller. Level shifters are included on the motherboard to adjust signal levels appropriately for the voltages selected for the device on the daughter card.

### 24.2 USB Audio

Audio in mono format can be streamed from an external USB host through the W681308 microcontroller and output in I2S format to the device on the daughter card. USB audio is in a standard USB isochronous stream format. Level shifters are included on the motherboard to adjust signal levels appropriately for the voltages selected for the device on the daughter card.

### 24.3 Unformatted Audio

Bi-directional serial audio may be connected directly to a device on the daughter card via the J15 serial audio connector. Although J15 is labeled on the motherboard as an I2S port, this port may be used for either I2S or PCM (DSP mode) audio data modes as determined by the external device connected to the J15 header. The path to use the J15 header is managed by the W681308 microcontroller. Level shifters are included on the motherboard to adjust signal levels appropriately for the voltages selected for the device on the daughter card.

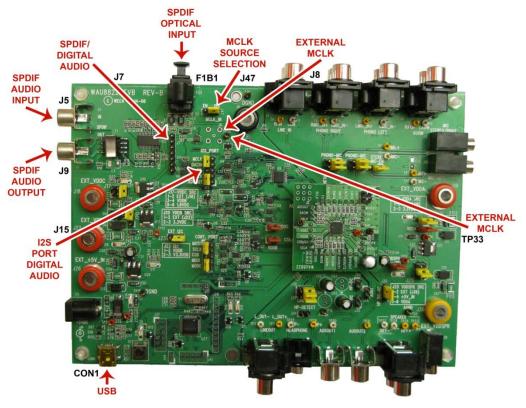


Figure 28: DIGITAL AUDIO INPUTS/OUTPUTS

## 25 Digital Audio Output

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There are three methods to stream digital audio from the NAU8822 audio data interface to the motherboard or external devices. These paths are set up using the appropriate connectors, and also, using the W681308 microcontroller managed by the GUI Application software to set up the paths accordingly.

#### 25.1 Formatted Digital Audio

A serial audio transceiver that supports AES/EBU, UEC958, S/PDIF, EIAJ CP340/1201 serial digital audio formats is included on the motherboard. Audio data from the NAU8822, and clock information to or from the NAU8822 may be routed to the transceiver under control of the W681308. The audio data from the NAU8822 ADC will then be available on the S/PDIF serial output from RCA jack, J9.

When the W681308 has configured the motherboard to use the S/PDIF transceiver, the I2S audio and clock signals to/from the NAU8822 are available on header J7.

#### 25.2 USB Audio

Audio data in mono format can be streamed from the NAU8822 ADC to the USB host through the W681308 microcontroller. USB audio is in a standard USB isochronous stream format.

#### 25.3 Unformatted Audio

Bi-directional serial audio may be connected directly to a device on the daughter card via the J15 serial audio connector. Although J15 is labeled on the motherboard as an I2S port, this port may be used for either I2S or PCM (DSP mode) audio data modes as determined by the external device connected to the J15 header. The path to use the J15 header is managed by the W681308 microcontroller. Level shifters are included on the motherboard to adjust signal levels appropriately for the voltages selected for the device on the daughter card.

## 25.4 Digital Audio Related Connector Options

Digital Audio Connector	Connector Type	Signal Name and Description
J5	RCA Jack (single)	SPDIF_IN digital audio from an external audio device
J9	RCA Jack (single)	SPDIF_OUT digital audio to an external audio device
TP33	Test Point	MCLK_IN external source for master clock
J8	SMB Connector	MCLK_IN external source for master clock (note: SMB connector not populated on PCB)
J7 pin1	Header	SPDIF_MCLK_OUT high speed clock generated by S/PDIF transceiver Passed to MCLK pin on daughter card if S/PDIF is set to be bus Master
J7 pin2	Header	SPDIF_ADCDAT_IN audio data from daughter card into S/PDIF transceiver This path is level shifted, but always enabled.
J7 pin3	Header	SPDIF_FRAME_IN frame sync from daughter card if provided by device on card
J7 pin4	Header	SPDIF_BCLK_IN bit clock from daughter card if provided by device on card
J7 pin5	Header	SPDIF_DACDAT_OUT serial audio data to daughter card
J7 pin6	Header	SPDIF_FRAME_OUT frame sync signal provided by S/PDIF transceiver
J7 pin7	Header	SPDIF_BLCK_OUT bit clock signal provided by the S/PDIF transceiver
J15 pin 1	Header	ADCOUT_AP audio data from daughter card if provided by device on card
J15 pin 3	Header	BCLK_AP bit clock to or from external device connected to J15
J15 pin 5	Header	FS_AP frame sync to or from external device connected to J15
J15 pin 7	Header	DACIN_AP audio data from external device
J15 pin 9	Header	MCLK_AP high speed MCLK signal to or from external device connected to J15
J47	Jumper	Pin 1-2 shorted to select external MCLK Pin 2-3 shorted to select internal MCLK on motherboard

Default factory configuration highlighted in color

#### Table 6: DIGITAL AUDIO CONNECTOR OPTIONS

## **26 USB and External Control CONNECTIONS**

The motherboard is connected to the USB host using a standard mini-USB type connector. USB V1.1 is supported, and in most cases, all power for the EVB is supplied via the USB cable.

Reference Designator	Connector Style	Pin Number	Signal Name			
		1	VCC			
	miniUSB Type B	2	USBD-			
		3	USBD+			
				-	4	NC
CON1		5	GND			
		6	SHIELD			
		7	7	SHIELD		
		8	SHIELD			
		9	SHIELD			

Table 7: USB CONNECTOR

#### 26.1 Special Connectors

The motherboard is connected to the USB host using a standard mini-USB type connector. USB V1.1 is supported, and in most cases, all power for the EVB is supplied via the USB cable.

Connector	Name	Description
J15	JTAG_ICE	JTAG ICE connector
J29, J37, J41	J29	For Nuvoton use to program the W681308 USB controller

Table 8: SPECIAL CONNECTORS

## 27 Jumpers

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All images of the motherboard show the jumpers in the standard configuration. This image may be used for reference to restore jumpers to the original factory-new positions.

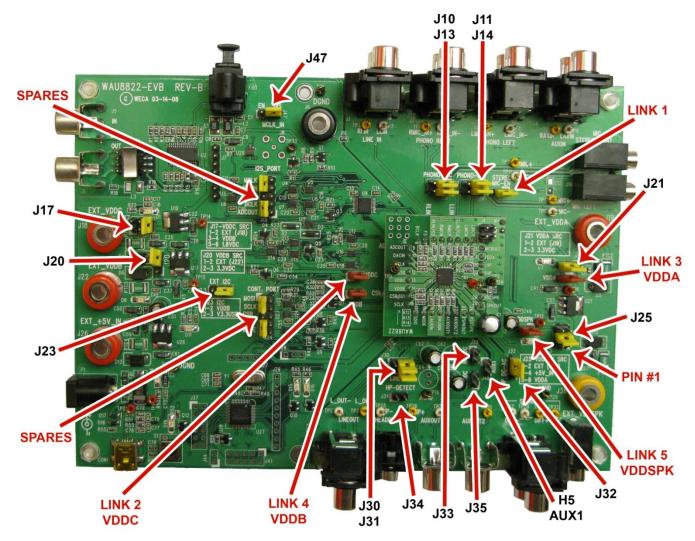


Figure 29: JUMPERS IN STANDARD CONFIGURATION

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# 27.1 Table of Jumper Options

Jumpers	Default Position	Description
J10	1-2 (short)	Position 1-2 selects Right MIC and Position 2-3 selects Right Phono
J11	1-2 (short)	Position 1-2 selects Left MIC and Position 2-3 selects Left Phono
J13	1-2 (short)	Position 1-2 selects Right MIC and Position 2-3 selects Right Phono
J14	1-2 (short)	Position 1-2 selects Left MIC and Position 2-3 selects Left Phono
J17	3-4(short)	The 3 position jumper selects the VDDC source. Position 1-2 Selects External VDD via J18, 3-4 Selects VDDB, and position 5-6 sects 1.8VDC
J20	2-3(short)	J20 Selects the VDDB source, position 1-2 selects external source via J22 position 2-3 selects 3.3VDC
J21	2-3(short)	J21 Selects the VDDA source, position 1-2 selects external source via J19 position 2-3 selects 3.3VDC
J23	2-3(short)	Install for external I2C at VDDB or I2C at 3.3V operation
J25	3-4 (short)	Speaker VDD selection jumper. Position 1-2 selects external source via (J36), position 3- 4 selects 5VDc and position 5-6 selects analog power (VDDA)
J28	Not on PCB	JTAG.connector for factory use with the W681308 USB controller
J30	2-3(short)	Position 1-2 Left Line_Out select and Position 2-3 selects Left HPOut (Left headphone out)
J31	2-3(short)	Position 1-2 Right Line_Out select and Position 2-3 selects right HP+_Out (Right headphone out)
J32	1-2 (short)	Position 1-2 selects Headphone cap-less mode and Position 2-3 selects AC coupled headphone output
J33	Open	Open position selects Headphone cap-less mode and Closed Position selects DC coupled headphone output (HP-) (Output for WAU8812, and WAU8814)
J34	Open	Headphone detect
J35	Open	Open position selects Headphone cap-less mode and Closed Position selects DC coupled headphone output (HP+)
J41	Not on PCB	Connector for JTAG ICE
J47	2-3(short)	Install this jumper for external MCLK Position 1-2 enables external MCLK and poison 2-3 disables the external MCLK.
AUX1	Open	H5 header on schematic. This is never a jumper. Two pin header for 150-ohm ear speaker load.
Link1	Closed	Set up 3.5mm stereo microphone for stereo operation.
Link2	Closed	Connects VDDC pin H2-5, on daughter card to VDDC supply voltage
Link3	Closed	Connects VDDA pin H3-7, on daughter card to VDDA supply voltage
Link4	Closed	Connects VDDB pin H2-6, on daughter card to VDDB supply voltage
Link5	Closed	Connects VDDSPK pin H3-2, on daughter card to VDDSPK supply voltage

#### Table 9: JUMPER OPTIONS

# 28 Test Points

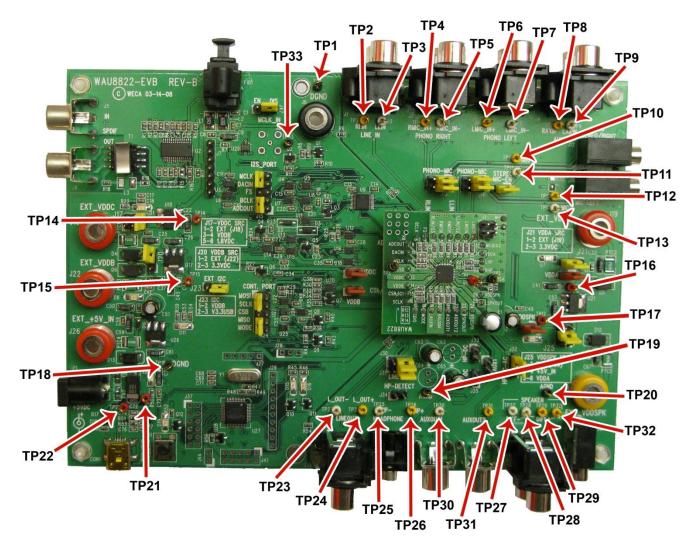


Figure 30: TEST POINTS

## 28.1 Table of Test Points

Reference Designator	Description	Signal Name
TP1	Digital Ground	DGND
TP2	Right Line_In	R_LIN
TP3	Left Line_In	L_LIN
TP4	Right Phono-In positive	RMIC_IN+
TP5	Right Phono-In Negative	RMIC_IN-
TP6	Left Phono-In positive	LMIC_IN+
TP7	Left Phono-In Negative	LMIC_IN-
TP8	Right Aux_IN	RAUXIN
TP9	Left Aux_IN	LAUXIN
TP10	Right Mic-In Positive	RMIC+
TP11	Right MIC-In Negative	RMIC-
TP12	Left MIC-In positive	LMIC+
TP13	Left MIC-In Negative	LMIC-
TP14	VDDC Source (J17)	J17-VDD-SRC
TP15	VDDB Source (J23)	J23 I2C
TP16	Analog Voltage test point	VDDA
TP17	Speaker VDD	VDDSPK
TP18	Digital Ground	DGND
TP19	Analog Ground	AGND
TP20	Analog Ground	AGND
TP21	External +5VDC P1	DC_EXT
TP22	Internal +5VDC Rail	+5V_IN
TP23	LINE OUT	L_OUT-
TP24	LINE OUT	L_OUT+
TP25	Headphone	HP-
TP26	Headphone	HP+
TP27	Differential Speaker Negative	DIFF-
TP28	Speaker Negative	SPK-
TP29	Differential Speaker Positive	DIFF+
TP332	Speaker positive	SPK+
TP31	AUXOU2	AUXOUT1
TP30	AUXOUT1	AUXOU2
TP33	External clock Input	MCLK_IN

Table 10: TEST POINTS

# 29 NAU8822-EVB Schematics (High Resolution Images)

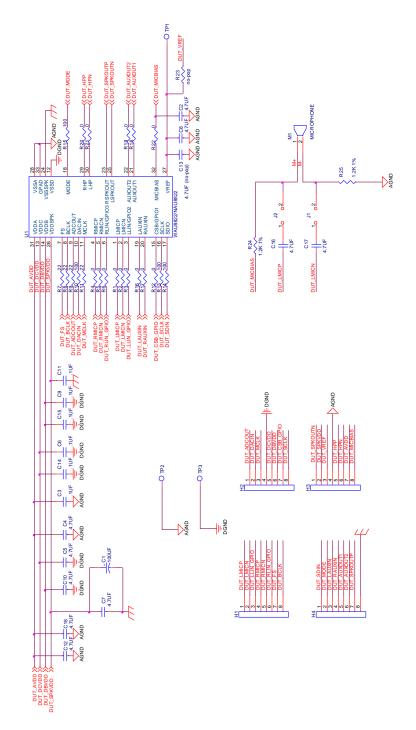




Figure 31: NAU8822 DAUGHTER CARD SCHEMATIC

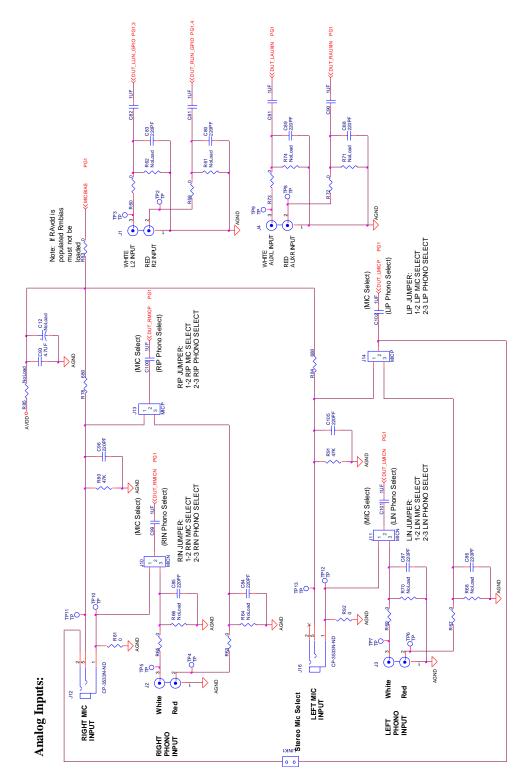


Figure 32: ANALOG INPUTS SCHEMATIC

# **CODEC** Motherboard

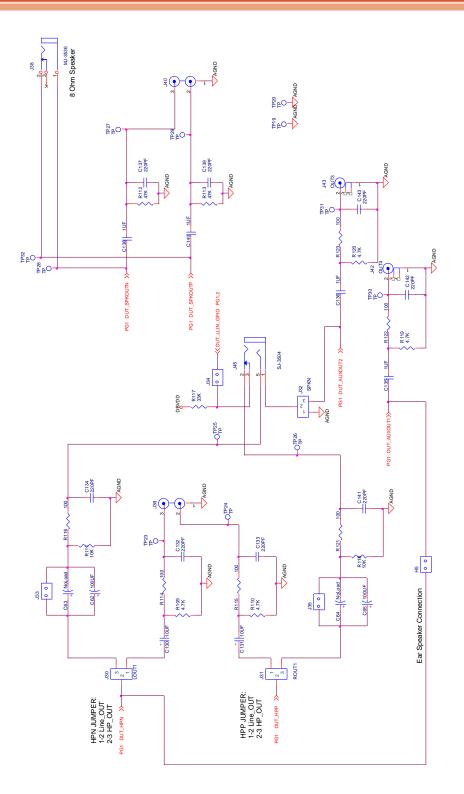


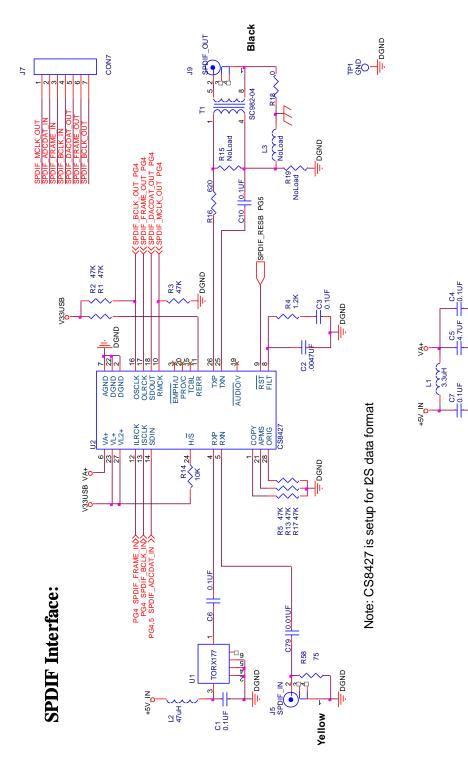
Figure 33: ANALOG OUTPUTS SCHEMATIC

# **CODEC** Motherboard

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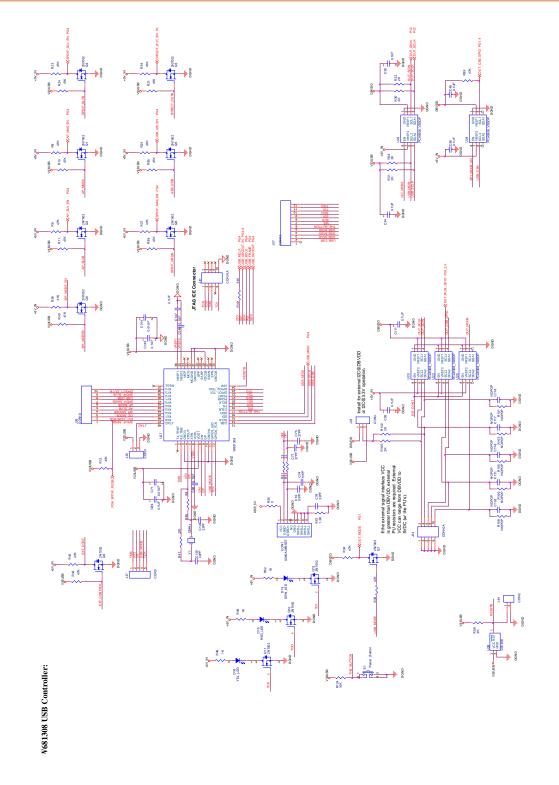
0.1UF

DGND



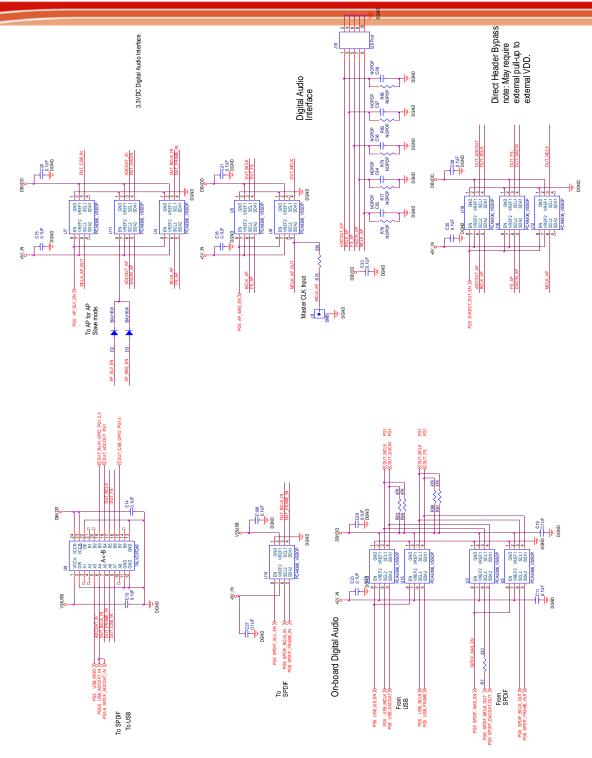


# **CODEC** Motherboard





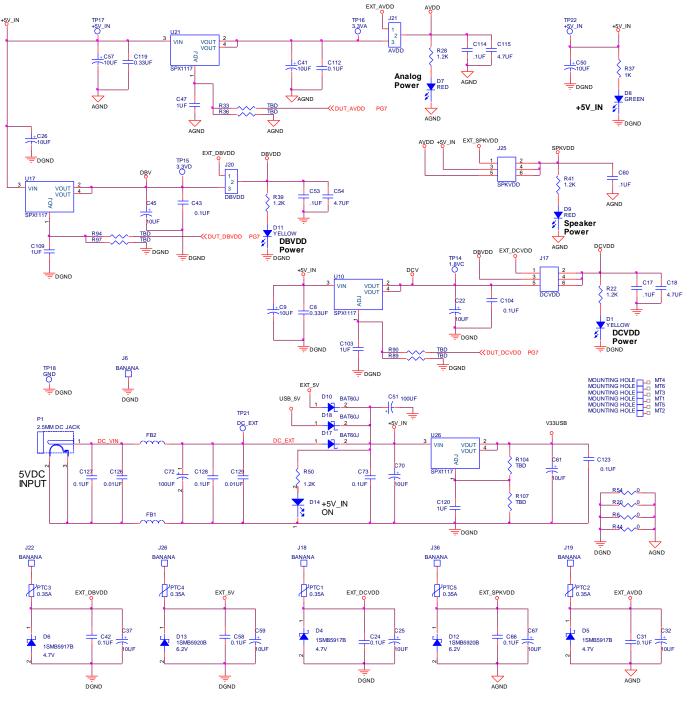
# **CODEC** Motherboard





# **CODEC** Motherboard







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#### **VERSION HISTORY**

VERSION	DATE	PAGE	DESCRIPTION
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0.2	June 17, 2008		Preliminary revision
0.3	June 17, 2008		Preliminary revision
0.5	July 24, 2008		Preliminary revision
0.6	December 24, 2008		Preliminary revision
0.7	January 12, 2009		Preliminary revision
1.0	February 04, 2010		General Revision
1.1	February 22,2013	9	Changed the GUI screen capture to reflect latest version
1.3	April 12, 2016	1 6	Changed Header & Title Replaced WAU8822 to NAU8822 Edit Fig.1 and first paragraph

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