NuMicro® Family

Arm® 32-bit Cortex®-M0 Microcontroller

M030G/M031G Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NuMicro® M030G/M031G 32-bit microcontroller series is designed for Optical Transceiver Module applications, both of the M030G and the M031G series have a built-in temperature sensor with ±1.6°C deviation from 0°C to 70°C and ±2°C deviation from -40°C to 105°C. Especially, the M031G series supports the "Pilot Tone Modulation" to realize the required OAM functions for the optical path network. Therefore, the M031G series is equipped with a high flexibility programmable Hardware Manchester Codec with CRC to encode and decode low-frequency dither signal and 1 set of DAC with "Auto Data Generation" function to generate the smooth sine waveform for the pilot tone modulation of optical path network up to 500kHz.

The M030G/M031G series is based on Arm® Cortex®-M0 core with 32-bit hardware multiplier/divider. It runs up to 48/72 MHz and features 32 Kbytes and 64 Kbytes Flash, 4 Kbytes and 8 Kbytes SRAM, 2.7V ~ 3.6V operating voltage, 5V I/O tolerant, and -40˚C to +105˚C operating temperature.

The M030G/M031G series provides plenty of peripherals including up to 6 sets of 32-bit timers, 1 set of UART with the RS485 and One-Wire mode, 1 set of SPI, 2 sets of I^2C supporting 1 MHz Slave Mode, and up to 7 channels of PDMA to offload CPU loading. Furthermore, both of these 2 series support I^2C bootloader for Optical Transceiver Module applications to program the application code into the M030/M031G series MCU through the I^2C interface.

The M030G/M031G series also provides rich analog peripherals including internal voltage reference that can output 2.5V, up to 16 channels of 1.4 MSPS 12-bit SAR ADC and 4 sets of 12-bit DAC. In addition, 1 set of DAC in the M031G series supports Auto Data Generation function.

In order to fit the small form factor requirement of the optical module, the M030G/M031G series provides the QFN 24-pin (3x3 mm) and QFN 33-pin (4x4 mm) small form factor package by pin-compatible across these 2 series to make the system design and change parts easily.

For the development system, Nuvoton provides the NuMaker evaluation board and Nuvoton Nu-Link debugger. The 3rd Party IDE such as Keil MDK, IAR EWARM, Eclippse IDE with GNU GCC compilers are also supported.

* 1 set of DAC with Auto Data Generation function

Product Line	UART	I^2C	SPI/ I^2S	Timer	BPWM	PDMA	ADC	DAC	Temp. Sensor	Internal V_{REF}	MANCH Codec	CRC
M030G	1	2	1	2	6	5	16	4	√	√		√
M031G	1	2	1	6	6	7	16	4*	√	√	√	√

Table 2.1-1 NuMicro M030G/M031G Series Key Features Support Table

2 FEATURES

2.1 M030G/M031G Features

Core and System	
Arm® Cortex®-M0	• Arm® Cortex®-M0 core, running up to 72 MHz • Built-in Nested Vectored Interrupt Controller (NVIC) • 24-bit system tick timer • Programmble and maskable interrupt • Low Power Sleep mode by WFI and WFE instructions
Brown-out Detector (BOD)	• Two-level BOD with brown-out interrupt and reset option (2.7V/2.5V)
Low Voltage Reset (LVR)	• LVR with 2.3V threshold voltage level
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID)
Memories	
Flash	• Up to 64/32 KB on-chip Application ROM (APROM) • Up to 2 KB on-chip Flash for user-defined loader (LDROM) • Up to 512 bytes non-readable Security Protection ROM (SPROM) • All on-chip Flash support 512 bytes page erase • Fast Flash programming verification with CRC-32 checksum calculation • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities • 2-wired ICP Flash updating through SWD/ICE interface
SRAM	• Up to 8 KB on-chip SRAM • Byte-, half-word- and word-access • PDMA operation
Cyclic Redundancy Calculation (CRC) - Configurable	• Supports 8-bits, 16-bits and 32-bits configurable polynomials • Programmable initial value and seed value • Programmable order reverse setting and one's complement setting for input data and CRC checksum • 8-bit, 16-bit, and 32-bit data width • 8-bit write mode with 1-AHB clock cycle operation • 16-bit write mode with 2-AHB clock cycle operation • 32-bit write mode with 4-AHB clock cycle operation

	• Uses DMA to write data with performing CRC operation
Cyclic Redundancy Calculation (CRC)	• Supports CRC-CCITT, CRC-8, CRC-16 and CRC-32 polynomials • Programmable initial value and seed value • Programmable order reverse setting and one's complement setting for input data and CRC checksum • 8-bit, 16-bit, and 32-bit data width • 8-bit write mode with 1-AHB clock cycle operation • 16-bit write mode with 2-AHB clock cycle operation • 32-bit write mode with 4-AHB clock cycle operation • Uses DMA to write data with performing CRC operation
Peripheral DMA (PDMA)	• Up to 7 independent and configurable channels for automatic data transfer between memories and peripherals • Basic and Scatter-Gather transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Fixed-priority and Round-robin priorities modes • Single and burst transfer types • Byte-, half-word- and word tranfer unit with count up to 65536 • Incremental or fixed source and destination address
Clocks	
Internal Clock Source	• 48 MHz High-speed Internal RC oscillator (HIRC) • 38.4 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wake-up operation • Up to 144 MHz on-chip PLL, allows CPU operation up to the maximim CPU frequency without the need for a high-frequency crystal
Timers	
32-bit Timer	• Up to 6 sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle and Continuous Counting operation modes • Supports event counting function to count the event from external pins • Supports external capture pin for interval measurement and resetting 24-bit up counter • Supports chip wake-up function, if a timer interrupt signal is generated
Basic PWM (BPWM)	• 16-bit counters with 12-bit clock pre-scale for 144 MHz PWM output channels • Up to 6 independent input capture channels with 16-bit resolution

	counter • Up, down or up-down PWM counter type • Mask function and tri-state output for each PWM channel • Able to trigger ADC to start conversion • Able to trigger DAC to start conversion
Watchdog	• 20-bit free running up counter for WDT time-out interval • Supports multiple clock sources from LIRC (default selection), HCLK/2048 with 9 selectable time-out period • Able to wake up system from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset
Window Watchdog	• Clock sourced from HCLK/2048 or LIRC; the window set by 6-bit counter with 11-bit prescale • Suspended in Idle/Power-down mode
Analog Interfaces	
Voltage Reference	• Internal built-in reference has 2.048V and 2.5V two voltage level selection for ADC, DAC or external devices • Supports ADC and DAC references voltage from internal built-in reference voltage, or external V_{REF} pin
ADC	• Analog input voltage range: 0 ~ AV_{DD} • One 12-bit, up to 1.4 MSPS SAR ADC with up to 16 single-ended input channels or 8 differential input pairs; 10-bit accuracy is guaranteed • Internal channels for band-gap V_{BG} input • Supports external V_{REF} pin or internal built-in reference voltage • Supports calibration capability • Four operation modes: Single mode, Burst mode, Single-cycle Scan mode and Continuous Scan mode • Analog-to-Digital conversion can be triggered by software (ADST), external pin (STADC), Timer 0~1 overflow pulse trigger, and BPWM1 trigger • Each conversion result is held in data register of each channel with valid and overrun indicators • Supports conversion result monitor by compare mode function • Configurable ADC external sampling time • PDMA operation • Supports floating detect function
DAC	• Analog input voltage range: 0 ~ AV_{DD}

	• Supports four 12-bit, 1 MSPS voltage type DAC • Supports 12- or 8-bit output mode • Supports external V_{REF} pin or internal built-in reference voltage • Digital-to-Analog conversion can be triggered by software (SWTRG), Timer 0~5 overflow pulse trigger, and BPWM1 trigger • Supports PDMA mode • Supports group mode of synchronized update capability for two DACs • Supports DAC output retention when system reset • 1 set of DAC Supports Auto Data Generation function in M031G series
Temperature Sensor	• Built-in calibrated temperature sensor • Supported temperature range: –40°C to 105°C • Precision: ±2 °C
Communication Interfaces	
Low-power UART	• Low-power UARTs with up to 7.2 MHz baud rate • Auto-Baud Rate measurement function • Supports low power UART (LPUART): baud rate clock from LIRC (38.4 kHz) with 9600bps in Power-down mode even system clock is stopped • 1-byte FIFOs with programmable level trigger • Auto flow control (nCTS and nRTS) • Supports IrDA (SIR) function • Supports RS-485 9-bit mode and direction control • Supports nCTS and incoming data wake-up function in idle mode • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • Supports wake-up function • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection functions • PDMA operation • Supports Single-wire function mode
I^2C	• Supports two sets of I^2C devices with Master/Slave mode • Supports Standard mode (100 kbps), Fast mode (400 kbps), Fast mode plus (1 Mbps) • Supports 7 bits mode • Programmable clocks allowing for versatile rate control

	• Supports multiple address recognition (four slave address with mask option) • Supports multi-address power-down wake-up function • PDMA operation • Supports receiving continuous data bytes in none stretch mode
SPI	• Up to 36 MHz in Master mode and up to 16 MHz in Slave mode at 2.7V~3.6V system voltage • Configurable bit length of a transfer word from 8 to 32-bit • Provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers • MSB first or LSB first transfer sequence • Byte reorder function • Supports Byte or Word Suspend mode • Supports one data channel half-duplex transfer • Supports receive-only mode • PDMA operation
GPIO	• Supports four I/O modes: Quasi bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode • Configured as interrupt source with edge/level trigger setting • Supports 5V-tolerance function except analog I/O (PA.0 ~ PA.3, PB.0~PB.15, PF0) • Enabling the pin interrupt function will also enable the wake-up function • Input schmitt trigger function • Supports independent pull-up control
Manchester Codec	• Supports encode/decode Manchester code • Supports different modulation signal format – Programmable Idle pattern – Programmable preamble style and its transmitted number – Programmable data size in a frame • Supports configurable Manchester bit rate • Supports selectable deglitch time function • Supports PDMA for receiving/transmitting • Supports Manchester encoded edge function to trigger Timer Controller

3 PARTS INFORMATION

3.1 Package Type

QFN24	QFN33
M030GGC1AE	M030GTC1AE
M030GGD1AE	M030GTD1AE
M031GGC2AE	M031GTC2AE
M031GGD2AE	M031GTD2AE

3.2 M030G/M031G Series Naming Rule

M0	30G	T	D	1	A	E
Core	**Line**	**Package**	**Flash**	**SRAM**	**Reserve**	**Temperature**
Cortex-M0	30: Base 31: with Manchester encode/decode	G: QFN24 (3x3x0.9 mm) T: QFN33 (4x4x0.8 mm)	C: 32 KB D: 64 KB	1: 4 KB 2: 8 KB		E:-40°C ~ 105°C

3.3 M030G/M031G Series Selection Guide

Part Number		M030G (Base)				M031G (Manchester)			
		GC1AE	GD1AE	TC1AE	TD1AE	GC2AE	GD2AE	TC2AE	TD2AE
Flash (KB)		32	64	32	64	32	64	32	64
SRAM (KB)		4				8			
LDROM (KB)		2				2			
SPROM (Bytes)		512				512			
System Frequency (MHz)		48				72			
PLL (MHz)		-				144			
I/O		19		28		19		28	
32-bit Timer		2				6			
Connectivity	UART	1				1			
	SPI/I²S	1				1			
	I²C/SMBus	2				2			
	Manchester	-				√			
BPWM		6				6			
PDMA		5				7			
CRC		√				-			
CRC- Configurable		-				√			
12-bit SAR ADC		11		16		11		16	
12-bit DAC		4				4*			
Temperature Sensor		√				√			
Internal Voltage Reference		√				√			
Package		QFN24		QFN33		QFN24		QFN33	

DAC*: 1 set supports Auto Data Generation function

4 PIN CONFIGURATION

Users can find pin configuration information in the M030G/M031G Multi-function Pin diagram sections or by using NuTool - PinConfigure. The NuTool - PinConfigure contains all NuMicro® Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1 Pin Configuration

4.1.1 M030G/M031G Series Pin Diagram

4.1.1.1 M030G/M031G Series QFN 24-Pin Diagram

Corresponding Part Number: M030GGC1AE, M030GGD1AE, M031GGD2AE, M031GGC2AE

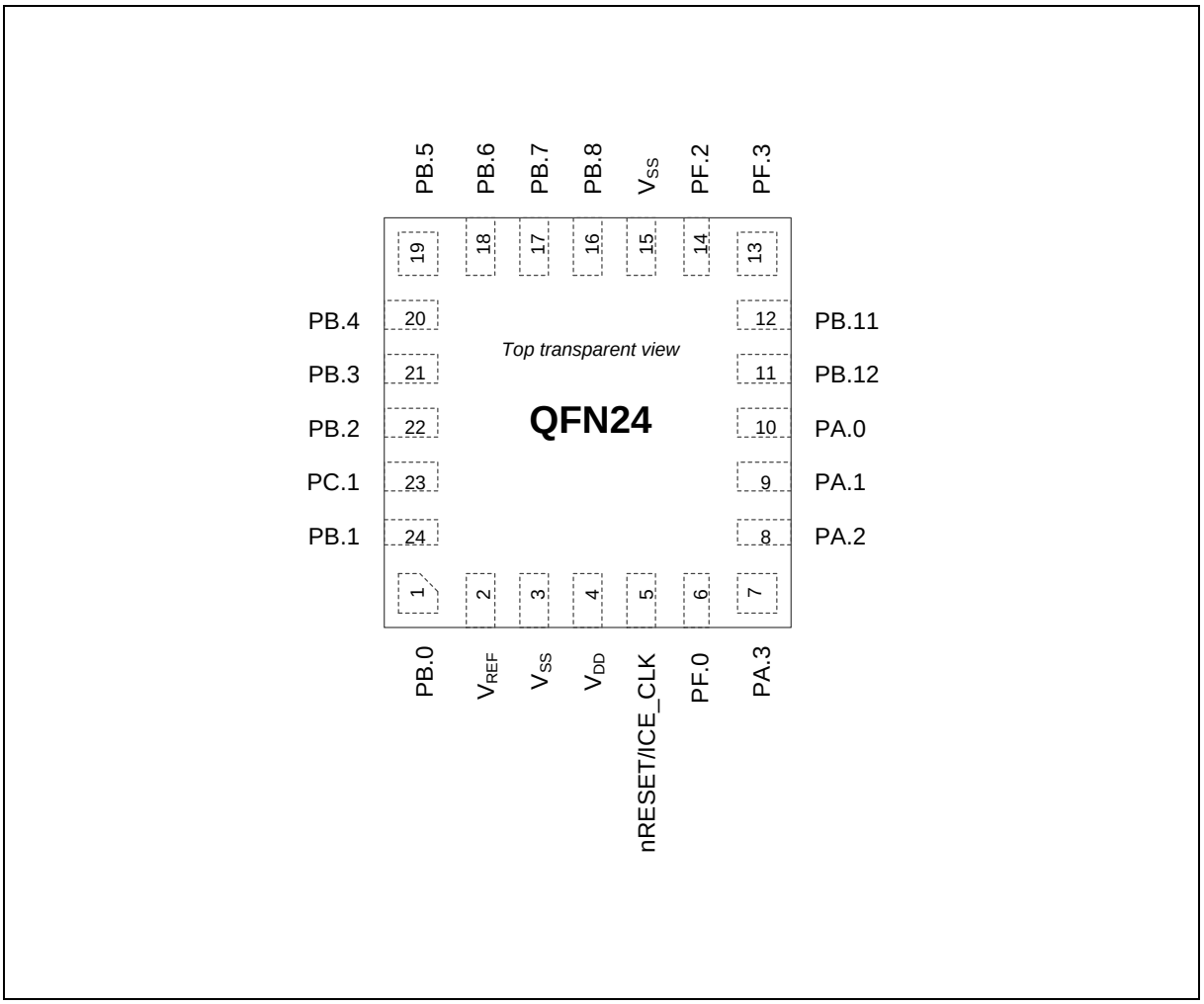


Figure 4.1-1 M030G/M031G Series QFN 24-pin Diagram

4.1.1.2 *M030G/M031G Series QFN 33-Pin Diagram*

Corresponding Part Number: M030GTC1AE, M030GTD1AE, M031GTD2AE, M031GTC2AE

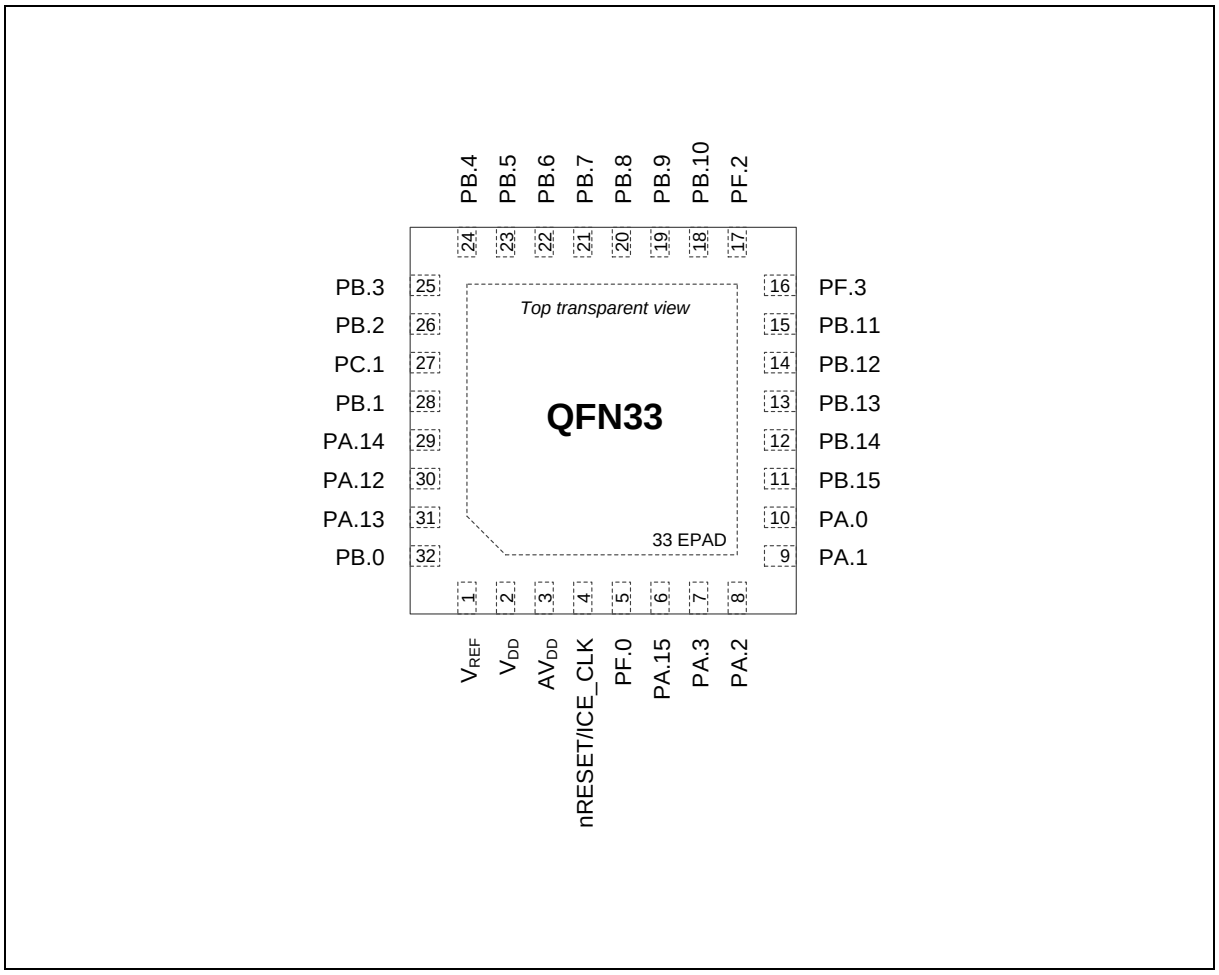


Figure 4.1-2 M030G/M031G Series QFN 33-pin Diagram

4.1.2 M030G Series Multi-function Pin Diagram

4.1.2.1 M030G Series QFN 24-Pin Multi-function Pin Diagram

Corresponding Part Number: M030GGC1AE, M030GGD1AE

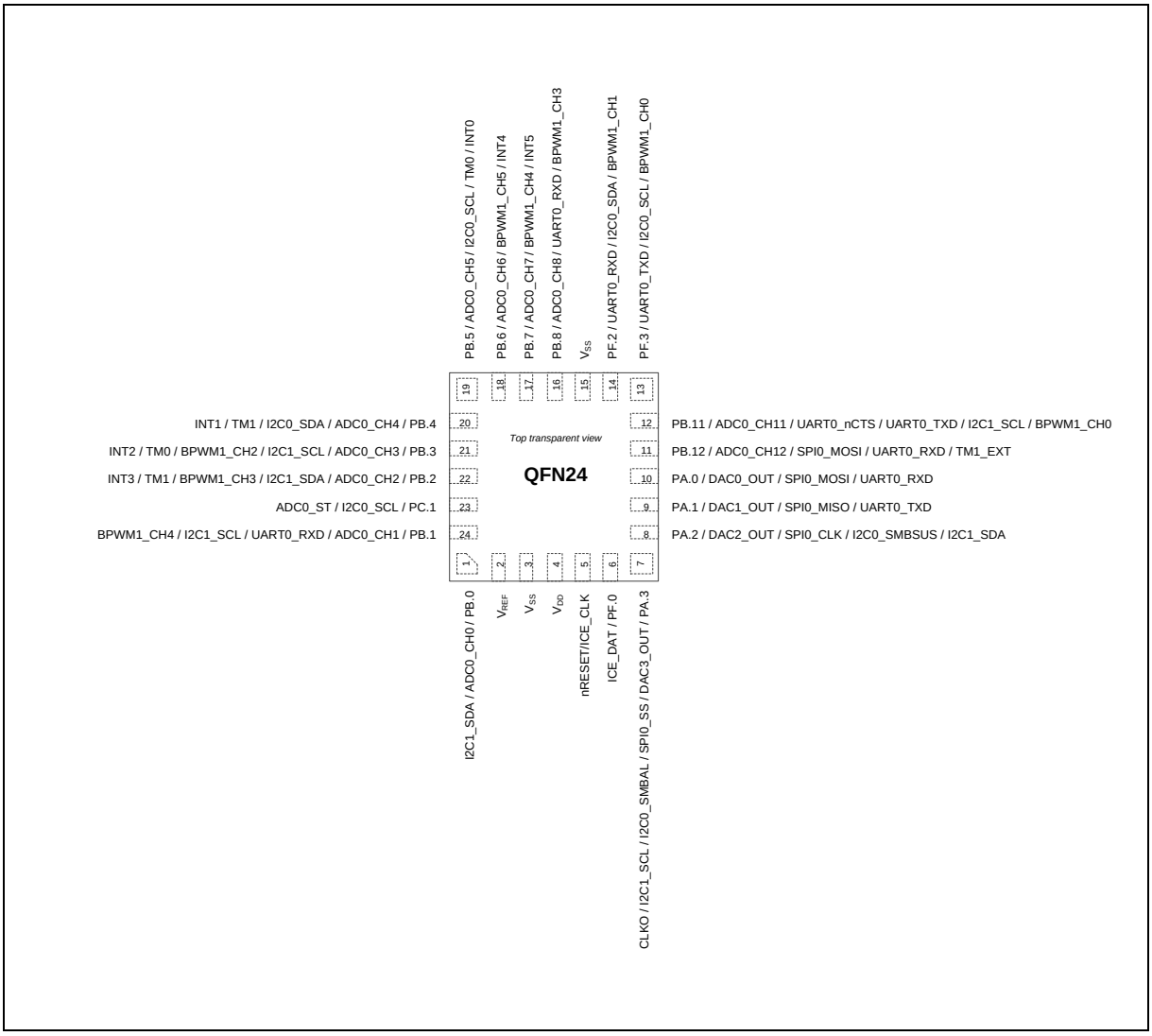


Figure 4.1-3 M030G Series QFN 24-pin Multi-function Pin Diagram

Pin	Pin Function
1	PB.0 / ADC0_CH0 / I2C1_SDA
2	V_{REF}
3	V_{SS}
4	V_{DD}
5	nRESET/ICE_CLK
6	PF.0 / ICE_DAT
7	PA.3 / DAC3_OUT / SPI0_SS / I2C0_SMBAL / I2C1_SCL / CLKO

Pin	Pin Function
8	PA.2 / DAC2_OUT / SPI0_CLK / I2C0_SMBSUS / I2C1_SDA
9	PA.1 / DAC1_OUT / SPI0_MISO / UART0_TXD
10	PA.0 / DAC0_OUT / SPI0_MOSI / UART0_RXD
11	PB.12 / ADC0_CH12 / SPI0_MOSI / UART0_RXD / TM1_EXT
12	PB.11 / ADC0_CH11 / UART0_nCTS / UART0_TXD / I2C1_SCL / BPWM1_CH0
13	PF.3 / UART0_TXD / I2C0_SCL / BPWM1_CH0
14	PF.2 / UART0_RXD / I2C0_SDA / BPWM1_CH1
15	V_{SS}
16	PB.8 / ADC0_CH8 / UART0_RXD / BPWM1_CH3
17	PB.7 / ADC0_CH7 / BPWM1_CH4 / INT5
18	PB.6 / ADC0_CH6 / BPWM1_CH5 / INT4
19	PB.5 / ADC0_CH5 / I2C0_SCL / TM0 / INT0
20	PB.4 / ADC0_CH4 / I2C0_SDA / TM1 / INT1
21	PB.3 / ADC0_CH3 / I2C1_SCL / BPWM1_CH2 / TM0 / INT2
22	PB.2 / ADC0_CH2 / I2C1_SDA / BPWM1_CH3 / TM1 / INT3
23	PC.1 / I2C0_SCL / ADC0_ST
24	PB.1 / ADC0_CH1 / UART0_RXD / I2C1_SCL / BPWM1_CH4

Table 4.1-1 M030GGC1AE and M030GGD1AE Multi-function Pin Table

4.1.2.2 M030G Series QFN 33-Pin Multi-function Pin Diagram

Corresponding Part Number: M030GTC1AE, M030GTD1AE

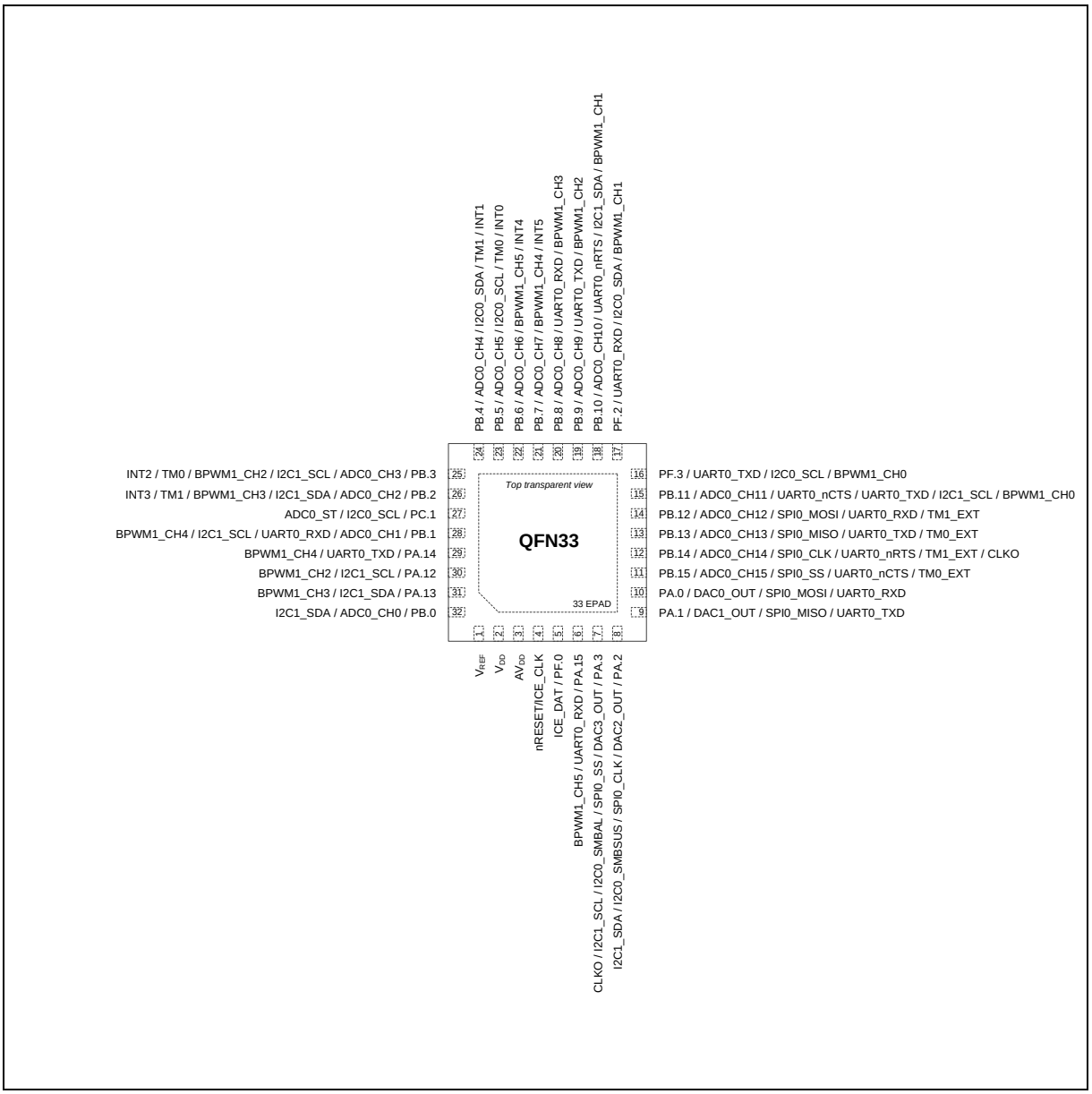


Figure 4.1-4 M030GTC1AE and M030GTD1AE Multi-function Pin Diagram

Pin	Pin Function
1	V_{REF}
2	V_{DD}
3	AV_{DD}
4	nRESET/ICE_CLK
5	PF.0 / ICE_DAT
6	PA.15 / UART0_RXD / BPWM1_CH5

Pin	Pin Function
7	PA.3 / DAC3_OUT / SPI0_SS / I2C0_SMBAL / I2C1_SCL / CLKO
8	PA.2 / DAC2_OUT / SPI0_CLK / I2C0_SMBSUS / I2C1_SDA
9	PA.1 / DAC1_OUT / SPI0_MISO / UART0_TXD
10	PA.0 / DAC0_OUT / SPI0_MOSI / UART0_RXD
11	PB.15 / ADC0_CH15 / SPI0_SS / UART0_nCTS / TM0_EXT
12	PB.14 / ADC0_CH14 / SPI0_CLK / UART0_nRTS / TM1_EXT / CLKO
13	PB.13 / ADC0_CH13 / SPI0_MISO / UART0_TXD / TM0_EXT
14	PB.12 / ADC0_CH12 / SPI0_MOSI / UART0_RXD / TM1_EXT
15	PB.11 / ADC0_CH11 / UART0_nCTS / UART0_TXD / I2C1_SCL / BPWM1_CH0
16	PF.3 / UART0_TXD / I2C0_SCL / BPWM1_CH0
17	PF.2 / UART0_RXD / I2C0_SDA / BPWM1_CH1
18	PB.10 / ADC0_CH10 / UART0_nRTS / I2C1_SDA / BPWM1_CH1
19	PB.9 / ADC0_CH9 / UART0_TXD / BPWM1_CH2
20	PB.8 / ADC0_CH8 / UART0_RXD / BPWM1_CH3
21	PB.7 / ADC0_CH7 / BPWM1_CH4 / INT5
22	PB.6 / ADC0_CH6 / BPWM1_CH5 / INT4
23	PB.5 / ADC0_CH5 / I2C0_SCL / TM0 / INT0
24	PB.4 / ADC0_CH4 / I2C0_SDA / TM1 / INT1
25	PB.3 / ADC0_CH3 / I2C1_SCL / BPWM1_CH2 / TM0 / INT2
26	PB.2 / ADC0_CH2 / I2C1_SDA / BPWM1_CH3 / TM1 / INT3
27	PC.1 / I2C0_SCL / ADC0_ST
28	PB.1 / ADC0_CH1 / UART0_RXD / I2C1_SCL / BPWM1_CH4
29	PA.14 / UART0_TXD / BPWM1_CH4
30	PA.12 / I2C1_SCL / BPWM1_CH2
31	PA.13 / I2C1_SDA / BPWM1_CH3
32	PB.0 / ADC0_CH0 / I2C1_SDA
33	EPAD

Table 4.1-2 M030GTC1AE and M030GTD1AE Pin Multi-function Pin Table

4.1.3 M031G Series Multi-function Pin Diagram

4.1.3.1 M031G Series QFN 24-Pin Multi-function Pin Diagram

Corresponding Part Number: M031GGD2AE, M031GGC2AE

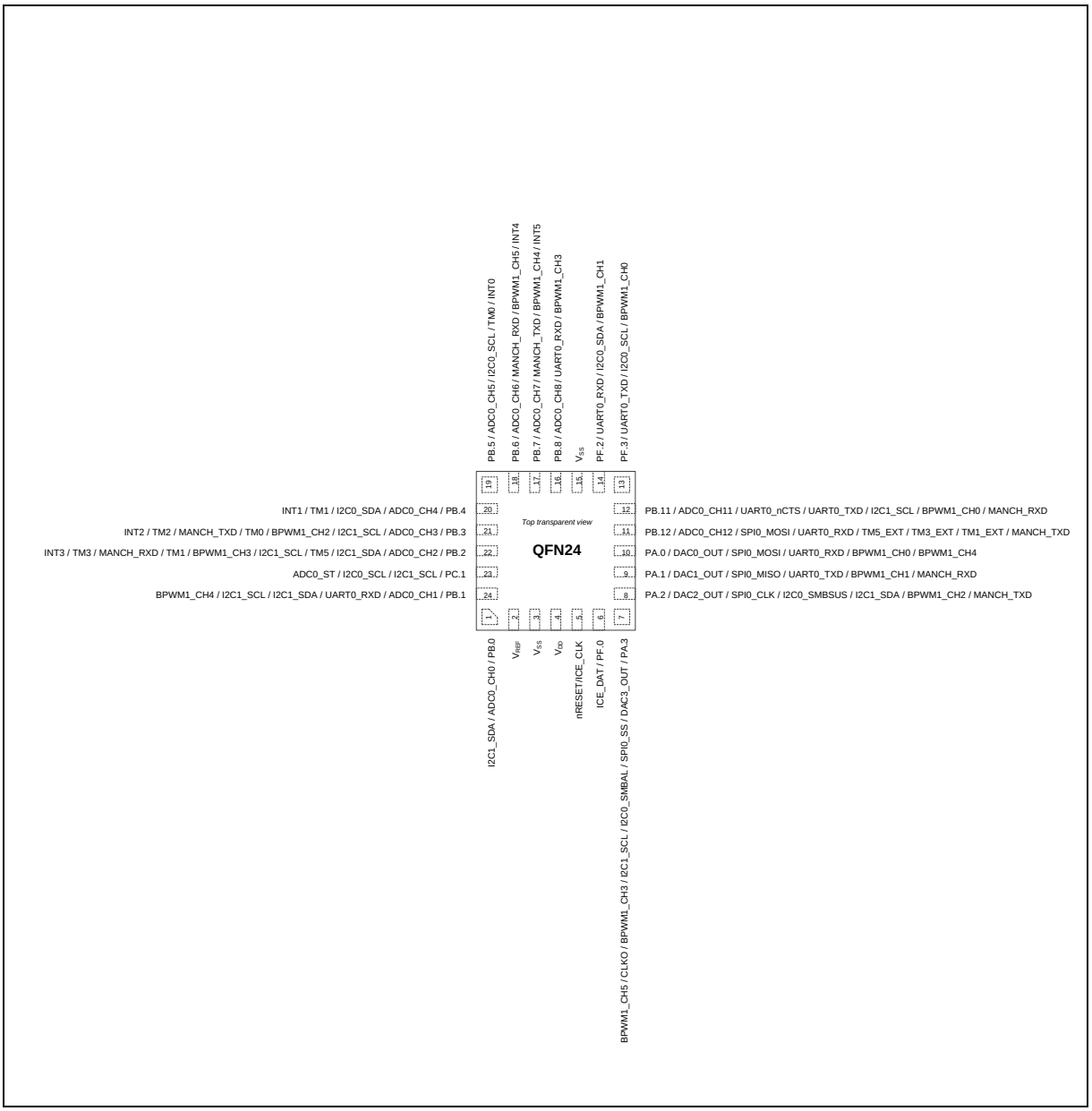


Figure 4.1-5 M031G Series QFN 24-pin Multi-function Pin Diagram

Pin	Pin Function
1	PB.0 / ADC0_CH0 / I2C1_SDA
2	V_{REF}
3	V_{SS}
4	V_{DD}

Pin	Pin Function
5	nRESET/ICE_CLK
6	PF.0 / ICE_DAT
7	PA.3 / DAC3_OUT / SPI0_SS / I2C0_SMBAL / I2C1_SCL / BPWM1_CH3 / CLKO / BPWM1_CH5
8	PA.2 / DAC2_OUT / SPI0_CLK / I2C0_SMBSUS / I2C1_SDA / BPWM1_CH2 / MANCH_TXD
9	PA.1 / DAC1_OUT / SPI0_MISO / UART0_TXD / BPWM1_CH1 / MANCH_RXD
10	PA.0 / DAC0_OUT / SPI0_MOSI / UART0_RXD / BPWM1_CH0 / BPWM1_CH4
11	PB.12 / ADC0_CH12 / SPI0_MOSI / UART0_RXD / TM5_EXT / TM3_EXT / TM1_EXT / MANCH_TXD
12	PB.11 / ADC0_CH11 / UART0_nCTS / UART0_TXD / I2C1_SCL / BPWM1_CH0 / MANCH_RXD
13	PF.3 / UART0_TXD / I2C0_SCL / BPWM1_CH0
14	PF.2 / UART0_RXD / I2C0_SDA / BPWM1_CH1
15	V_{SS}
16	PB.8 / ADC0_CH8 / UART0_RXD / BPWM1_CH3
17	PB.7 / ADC0_CH7 / MANCH_TXD / BPWM1_CH4 / INT5
18	PB.6 / ADC0_CH6 / MANCH_RXD / BPWM1_CH5 / INT4
19	PB.5 / ADC0_CH5 / I2C0_SCL / TM0 / INT0
20	PB.4 / ADC0_CH4 / I2C0_SDA / TM1 / INT1
21	PB.3 / ADC0_CH3 / I2C1_SCL / BPWM1_CH2 / TM0 / MANCH_TXD / TM2 / INT2
22	PB.2 / ADC0_CH2 / I2C1_SDA / TM5 / I2C1_SCL / BPWM1_CH3 / TM1 / MANCH_RXD / TM3 / INT3
23	PC.1 / I2C1_SCL / I2C0_SCL / ADC0_ST
24	PB.1 / ADC0_CH1 / UART0_RXD / I2C1_SDA / I2C1_SCL / BPWM1_CH4

Table 4.1-3 M031GGD2AE and M031GGC2AE Multi-function Pin Table

4.1.3.2 M031G Series QFN 33-Pin Multi-function Pin Diagram

Corresponding Part Number: M031GTD2AE, M031GTC2AE

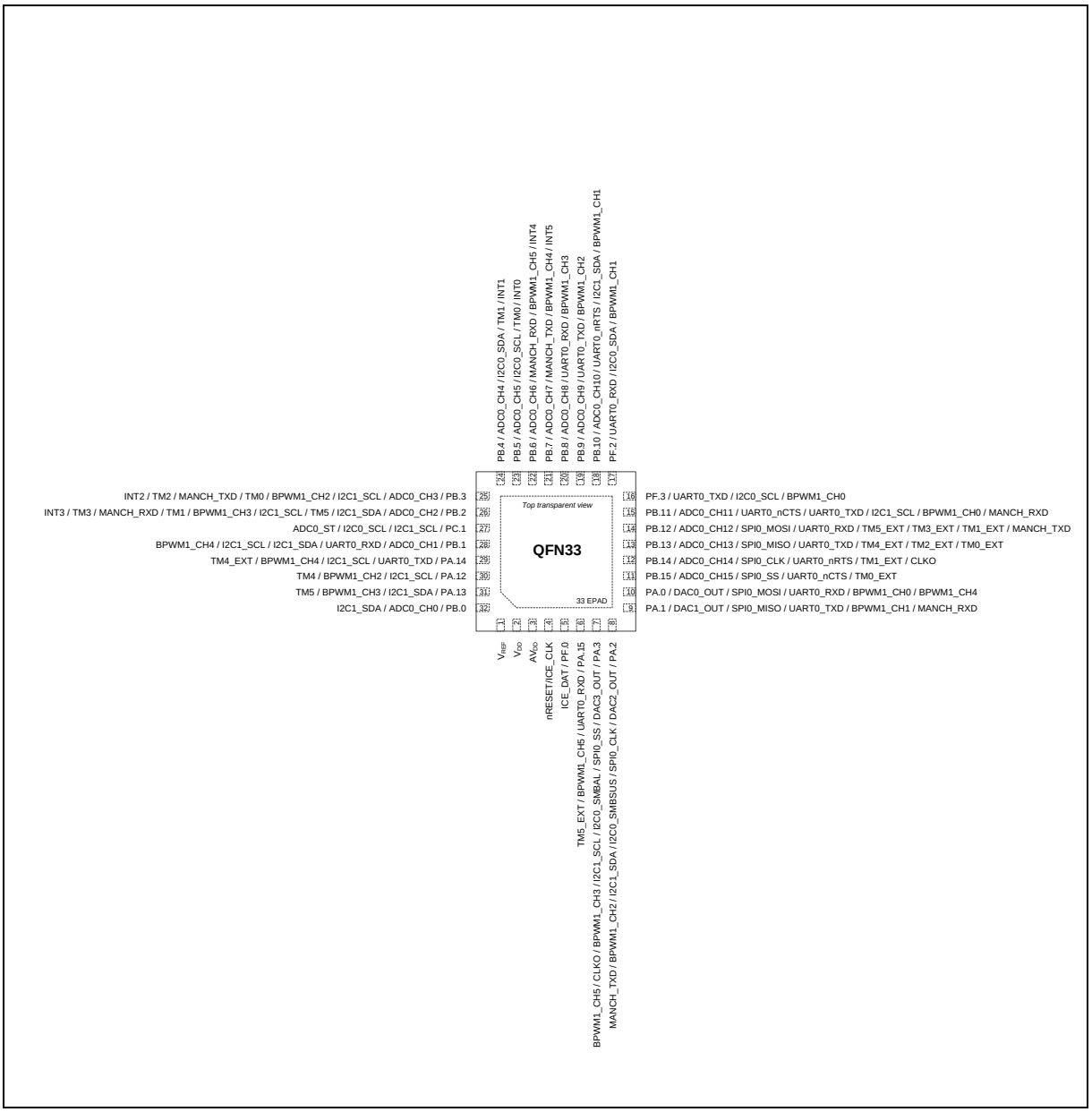


Figure 4.1-6 M031GTD2AE and M031GTC2AE Multi-function Pin Diagram

Pin	Pin Function
1	V_{REF}
2	V_{DD}
3	AV_{DD}
4	nRESET/ICE_CLK
5	PF.0 / ICE_DAT

Pin	Pin Function
6	PA.15 / UART0_RXD / BPWM1_CH5 / TM5_EXT
7	PA.3 / DAC3_OUT / SPI0_SS / I2C0_SMBAL / I2C1_SCL / BPWM1_CH3 / CLKO / BPWM1_CH5
8	PA.2 / DAC2_OUT / SPI0_CLK / I2C0_SMBSUS / I2C1_SDA / BPWM1_CH2 / MANCH_TXD
9	PA.1 / DAC1_OUT / SPI0_MISO / UART0_TXD / BPWM1_CH1 / MANCH_RXD
10	PA.0 / DAC0_OUT / SPI0_MOSI / UART0_RXD / BPWM1_CH0 / BPWM1_CH4
11	PB.15 / ADC0_CH15 / SPI0_SS / UART0_nCTS / TM0_EXT
12	PB.14 / ADC0_CH14 / SPI0_CLK / UART0_nRTS / TM1_EXT / CLKO
13	PB.13 / ADC0_CH13 / SPI0_MISO / UART0_TXD / TM4_EXT / TM2_EXT / TM0_EXT
14	PB.12 / ADC0_CH12 / SPI0_MOSI / UART0_RXD / TM5_EXT / TM3_EXT / TM1_EXT / MANCH_TXD
15	PB.11 / ADC0_CH11 / UART0_nCTS / UART0_TXD / I2C1_SCL / BPWM1_CH0 / MANCH_RXD
16	PF.3 / UART0_TXD / I2C0_SCL / BPWM1_CH0
17	PF.2 / UART0_RXD / I2C0_SDA / BPWM1_CH1
18	PB.10 / ADC0_CH10 / UART0_nRTS / I2C1_SDA / BPWM1_CH1
19	PB.9 / ADC0_CH9 / UART0_TXD / BPWM1_CH2
20	PB.8 / ADC0_CH8 / UART0_RXD / BPWM1_CH3
21	PB.7 / ADC0_CH7 / MANCH_TXD / BPWM1_CH4 / INT5
22	PB.6 / ADC0_CH6 / MANCH_RXD / BPWM1_CH5 / INT4
23	PB.5 / ADC0_CH5 / I2C0_SCL / TM0 / INT0
24	PB.4 / ADC0_CH4 / I2C0_SDA / TM1 / INT1
25	PB.3 / ADC0_CH3 / I2C1_SCL / BPWM1_CH2 / TM0 / MANCH_TXD / TM2 / INT2
26	PB.2 / ADC0_CH2 / I2C1_SDA / TM5 / I2C1_SCL / BPWM1_CH3 / TM1 / MANCH_RXD / TM3 / INT3
27	PC.1 / I2C1_SCL / I2C0_SCL / ADC0_ST
28	PB.1 / ADC0_CH1 / UART0_RXD / I2C1_SDA / I2C1_SCL / BPWM1_CH4
29	PA.14 / UART0_TXD / I2C1_SCL / BPWM1_CH4 / TM4_EXT
30	PA.12 / I2C1_SCL / BPWM1_CH2 / TM4
31	PA.13 / I2C1_SDA / BPWM1_CH3 / TM5
32	PB.0 / ADC0_CH0 / I2C1_SDA
33	EPAD

Table 4.1-4 M031GTD2AE and M031GTC2AE Pin Multi-function Pin Table

4.2 Pin Mapping

Different part number with same package might has different function. Please refer to the M030G/M031G Series Selection Guide, Pin Configuration section or NuTool - PinConfig.

Corresponding Part Number: M030GxC, M030GxD, M031GxC, M031GxD series.

	M030G/M031G Series	
Pin Name	24 Pin	33 Pin
V_{REF}	2	1
V_{SS}	3	
V_{DD}	4	2
A_{VDD}		3
nRESET/ICE_CLK	5	4
PF.0	6	5
PA.15		6
PA.3	7	7
PA.2	8	8
PA.1	9	9
PA.0	10	10
PB.15		11
PB.14		12
PB.13		13
PB.12	11	14
PB.11	12	15
PF.3	13	16
PF.2	14	17
PB.10		18
PB.9		19
V_{SS}	15	
PB.8	16	20
PB.7	17	21
PB.6	18	22
PB.5	19	23
PB.4	20	24
PB.3	21	25
PB.2	22	26
PC.1	23	27

PB.1	24	28
PA.14		29
PA.12		30
PA.13		31
PB.0	1	32
EPAD		33

4.3 Pin Functional Description

Corresponding Part Number: M030GxC, M030GxD, M031GxC, M031GxD series.

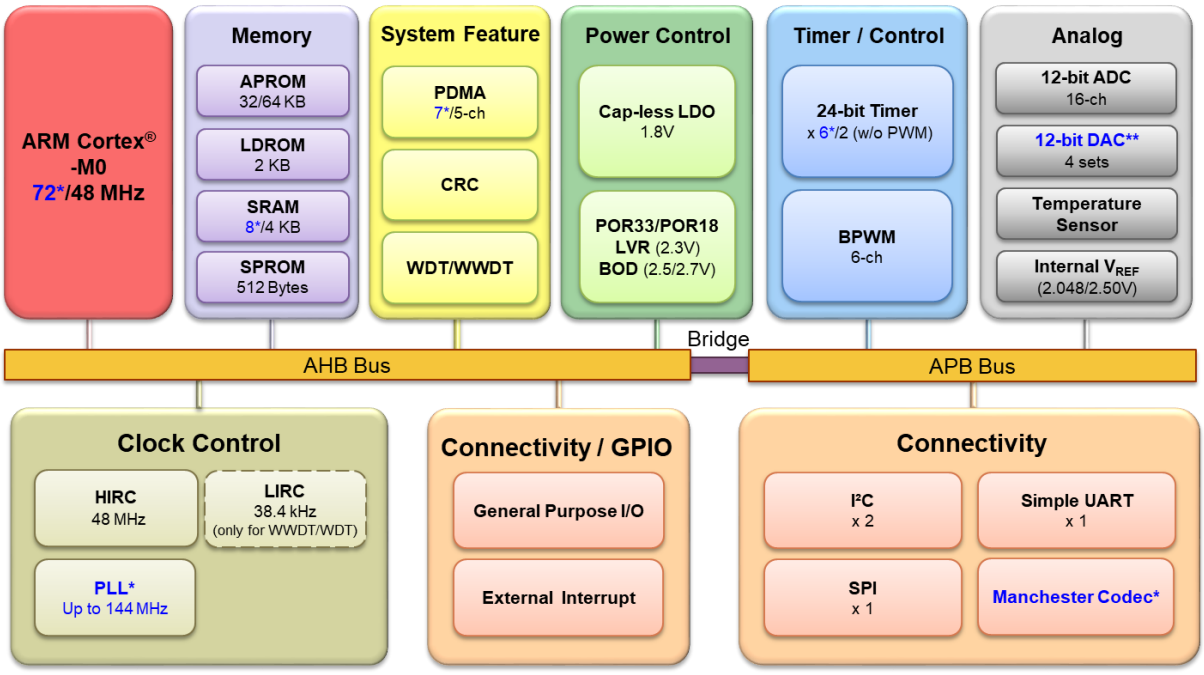
Group	Pin Name	Type	Description
ADC0	ADC0_CH0	A	ADC0 channel 0 analog input.
	ADC0_CH1	A	ADC0 channel 1 analog input.
	ADC0_CH2	A	ADC0 channel 2 analog input.
	ADC0_CH3	A	ADC0 channel 3 analog input.
	ADC0_CH4	A	ADC0 channel 4 analog input.
	ADC0_CH5	A	ADC0 channel 5 analog input.
	ADC0_CH6	A	ADC0 channel 6 analog input.
	ADC0_CH7	A	ADC0 channel 7 analog input.
	ADC0_CH8	A	ADC0 channel 8 analog input.
	ADC0_CH9	A	ADC0 channel 9 analog input.
	ADC0_CH10	A	ADC0 channel 10 analog input.
	ADC0_CH11	A	ADC0 channel 11 analog input.
	ADC0_CH12	A	ADC0 channel 12 analog input.
	ADC0_CH13	A	ADC0 channel 13 analog input.
	ADC0_CH14	A	ADC0 channel 14 analog input.
	ADC0_CH15	A	ADC0 channel 15 analog input.
	ADC0_ST	I	ADC0 external trigger input pin.
BPWM1	BPWM1_CH0	I/O	BPWM1 channel 0 output/capture input.
	BPWM1_CH1	I/O	BPWM1 channel 1 output/capture input.

Group	Pin Name	Type	Description
	BPWM1_CH2	I/O	BPWM1 channel 2 output/capture input.
	BPWM1_CH3	I/O	BPWM1 channel 3 output/capture input.
	BPWM1_CH4	I/O	BPWM1 channel 4 output/capture input.
	BPWM1_CH5	I/O	BPWM1 channel 5 output/capture input.
CLKO	CLKO	O	Clock Out
DAC0	DAC0_OUT	A	DAC0 channel analog output.
DAC1	DAC1_OUT	A	DAC1 channel analog output.
DAC2	DAC2_OUT	A	DAC2 channel analog output.
DAC3	DAC3_OUT	A	DAC3 channel analog output.
I2C0	I2C0_SCL	I/O	I2C0 clock pin.
	I2C0_SDA	I/O	I2C0 data input/output pin.
	I2C0_SMBAL	O	I2C0 SMBus SMBALTER pin
	I2C0_SMBSUS	O	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
I2C1	I2C1_SCL	I/O	I2C1 clock pin.
	I2C1_SDA	I/O	I2C1 data input/output pin.
ICE	ICE_CLK	I	Serial wired debugger clock pin **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin
	nRESET /ICE_DAT	I/O	nRESET : External reset input, active LOW with an internal pull-up. Set this pin low reset to initial state. ICE_DAT : Serial wired debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
INT0	INT0	I	External interrupt 0 input pin.
INT1	INT1	I	External interrupt 1 input pin.
INT2	INT2	I	External interrupt 2 input pin.

Group	Pin Name	Type	Description
INT3	INT3	I	External interrupt 3 input pin.
INT4	INT4	I	External interrupt 4 input pin.
INT5	INT5	I	External interrupt 5 input pin.
MANCH	MANCH_RXD	I	Manchester data receiver input pin.
	MANCH_TXD	O	Manchester data transmitter output pin.
Power	V_{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
	V_{SS}	P	Ground pin for digital circuit.
	AV_{DD}	P	Power supply for internal analog circuit.
	AV_{SS}	P	Ground pin for analog circuit.
	V_{REF}	A	ADC and DAC reference voltage input. **Note:** This pin needs to be connected with a 1uF capacitor.
	EPAD	P	Exposed pad served as ground pin (VSS).
SPI0	SPI0_CLK	I/O	SPI0 serial clock pin.
	SPI0_MISO	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_MOSI	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_SS	I/O	SPI0 slave select pin.
TM0	TM0	I/O	Timer0 event counter input/toggle output pin.
	TM0_EXT	I/O	Timer0 external capture input/toggle output pin.
TM1	TM1	I/O	Timer1 event counter input/toggle output pin.
	TM1_EXT	I/O	Timer1 external capture input/toggle output pin.
TM2	TM2	I/O	Timer2 event counter input/toggle output pin.
	TM2_EXT	I/O	Timer2 external capture input/toggle output pin.

Group	Pin Name	Type	Description
TM3	TM3	I/O	Timer3 event counter input/toggle output pin.
	TM3_EXT	I/O	Timer3 external capture input/toggle output pin.
TM4	TM4	I/O	Timer4 event counter input/toggle output pin.
	TM4_EXT	I/O	Timer4 external capture input/toggle output pin.
TM5	TM5	I/O	Timer5 event counter input/toggle output pin.
	TM5_EXT	I/O	Timer5 external capture input/toggle output pin.
UART0	UART0_RXD	I	UART0 data receiver input pin.
	UART0_TXD	O	UART0 data transmitter output pin.
	UART0_nCTS	I	UART0 clear to Send input pin.
	UART0_nRTS	O	UART0 request to Send output pin.

5 BLOCK DIAGRAM



* Only in M031G Series

** M031G Series is equipped with 1 set of DAC with Auto Data Generation function

Figure 5-1 NuMicro M030G/M031G Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Arm® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6.1-1 shows the functional controller of processor.

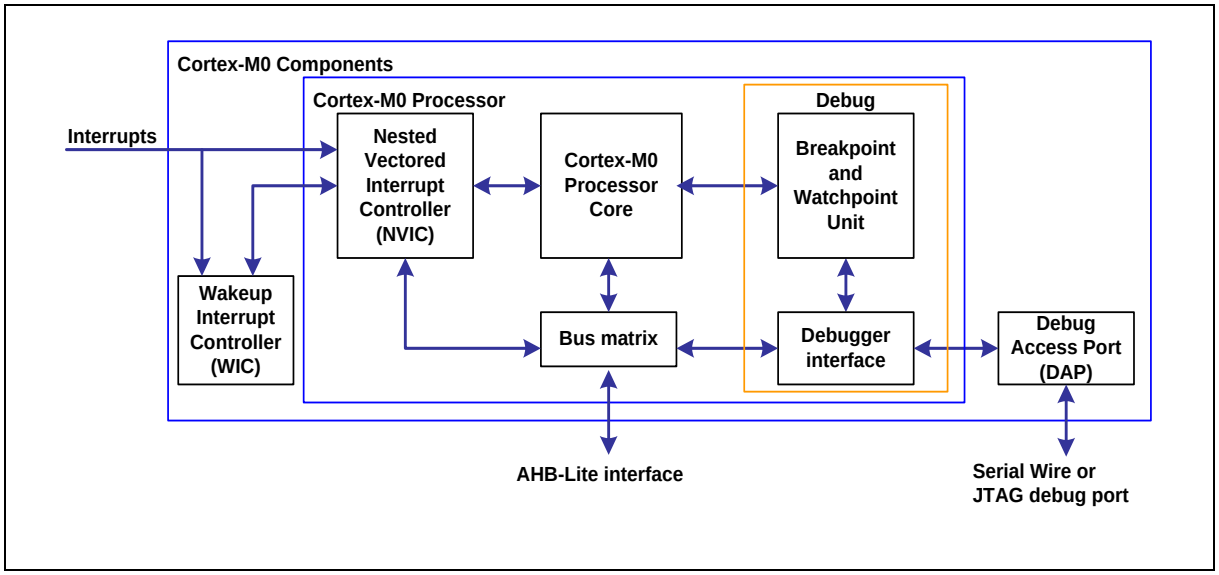


Figure 6.1-1 Functional Block Diagram

The implemented device provides:

- A low gate count processor:
  - Arm®6-M Thumb® instruction set
  - Thumb-2 technology
  - Arm®6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the Armv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature
- NVIC:
  - 32 external interrupt inputs, each with four levels of priority

- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode

- Debug support:
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Orginization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sources are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M0 core only by writing 1 to CPURST (SYS_IPRST0[1])

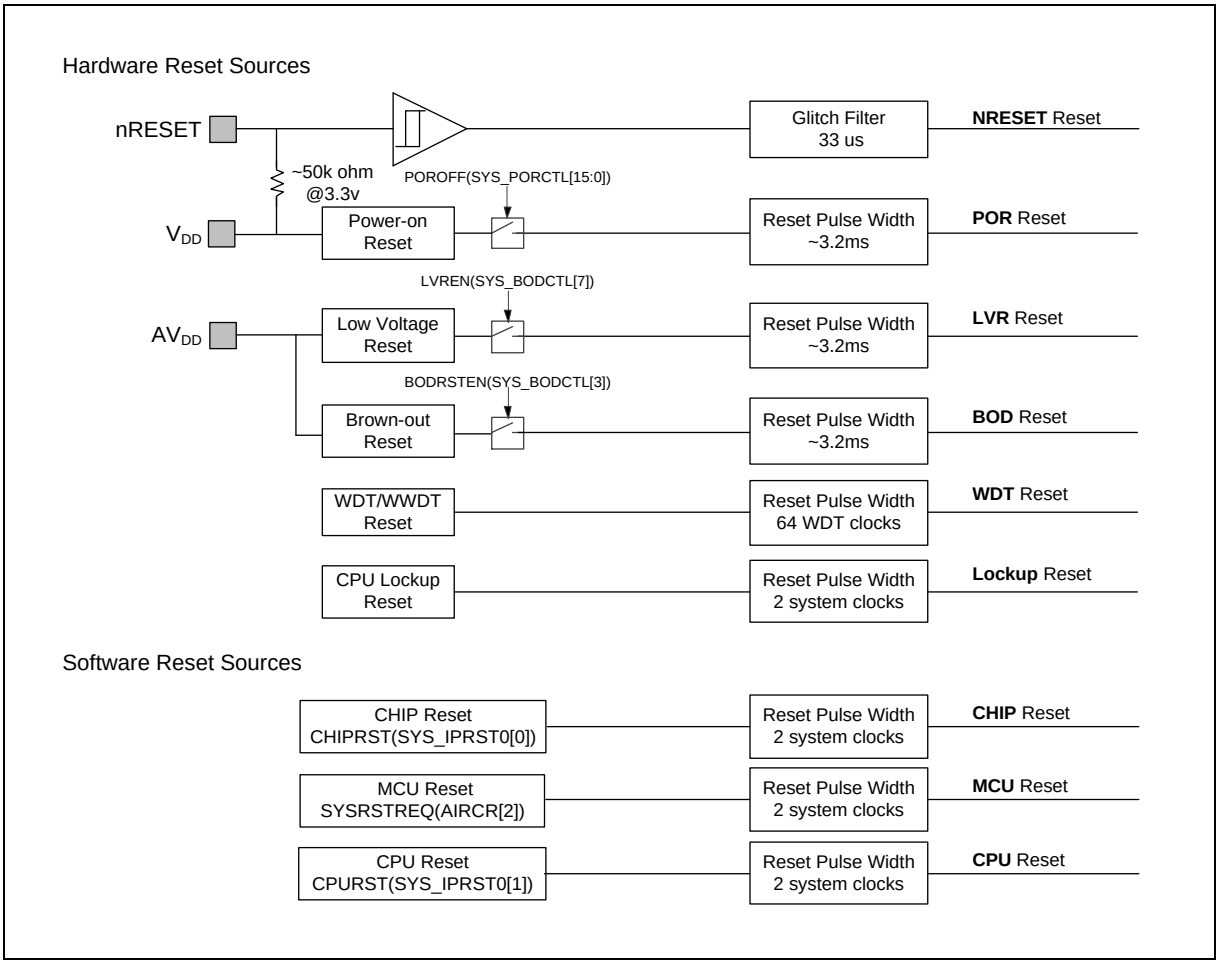


Figure 6.2-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M0 only; the other reset sources will reset Cortex®-M0 and all peripherals. However, there are some registers with particularly different reset sources. Table 6.2-1 lists these differences.

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
SYS_RSTSTS	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	0x0	0x1	0x1	0x1	-	0x1	0x1	0x1	-
BODVL (SYS_BODCTL[16])	0x0	0x0	0x0	0x0	-	0x0	0x0	0x0	-
BODRSTEN (SYS_BODCTL[3])	0x1	0x1	0x1	0x1	-	0x1	0x1	0x1	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
HCLKSEL	0x7	0x7	0x7	0x7	0x7	0x7	0x7	0x7	-

(CLK_CLKSEL0[2:0])									
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HIRCSTB (CLK_STATUS[4])	0x0	-	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1]) WDTEN (WDT_CTL[7])	Reload from CONFIG 0	Reload from CONFIG 0	Reload from CONFIG 0	Reload from CONFIG 0	Reload from CONFIG 0	-	Reload from CONFIG 0	-	-
WDT_CTL except bit 1 and bit 7.	0x0800	0x0800	0x0800	0x0800	0x0800	-	0x0800	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
BS (FMC_ISPCTL[1])	Reload from CONFIG 0	Reload from CONFIG 0	Reload from CONFIG 0	Reload from CONFIG 0	Reload from CONFIG 0	-	Reload from CONFIG 0	-	-
FMC_DFBA	Reload from CONFIG 1	Reload from CONFIG 1	Reload from CONFIG 1	Reload from CONFIG 1	Reload from CONFIG 1	-	Reload from CONFIG 1	-	-
CBS (FMC_ISPSTS[2:1))	Reload from CONFIG 0	Reload from CONFIG 0	Reload from CONFIG 0	Reload from CONFIG 0	Reload from CONFIG 0	-	Reload from CONFIG 0	-	-
VECMAP (FMC_ISPSTS[23:9])	Reload base on CONFIG 0	Reload base on CONFIG 0	Reload base on CONFIG 0	Reload base on CONFIG 0	Reload base on CONFIG 0	-	Reload base on CONFIG 0	-	-
DAC IP Registers (RETEN, DAC0_CTL[24]=1)	Refer to Table 6.2-2 for DAC Reset Retention source and reset value.								
DAC IP Registers (RETEN, DAC0_CTL[24]=0)	Reset Value								-
GPIO IP Registers (RETEN (GPIO_RET[0]) = 1)	Refer to Table 6.2-3 for GPIO Reset Retention source and reset value.								
GPIO IP Registers (RETEN (GPIO_RET[0]) = 0)	Reset Value								-
Other Peripheral Registers	Reset Value								-
FMC Registers	Reset Value								
Note: '-' means that the value of register keeps original setting.									

Table 6.2-1 Reset Value of Registers

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
DAC Registers	Reset Value	-	-	Reset Value	Reset Value	Reset Value	-	-	-
SCPDIS (SYS_VREFCTL[8])	0x0	-	-	0x0	0x0	0x0	-	-	-
PRELOADEN (SYS_VREFCTL[6])	0x0	-	-	0x0	0x0	0x0	-	-	-
VREFSEL (SYS_VREFCTL[1])	0x0	-	-	0x0	0x0	0x0	-	-	-
VREFEN (SYS_VREFCTL[0])	0x0	-	-	0x0	0x0	0x0	-	-	-
TSBGEN (SYS_TSCTL[1])	0x0	-	-	0x0	0x0	0x0	-	-	-

Table 6.2-2 DAC Reset Retention Value of Registers

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
GPIO Registers	Reset Value	-	-	Reset Value	Reset Value	Reset Value	-	-	-

Table 6.2-3 GPIO Reset Retention Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 33 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 33 us (glitch filter). The PINRF (SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.

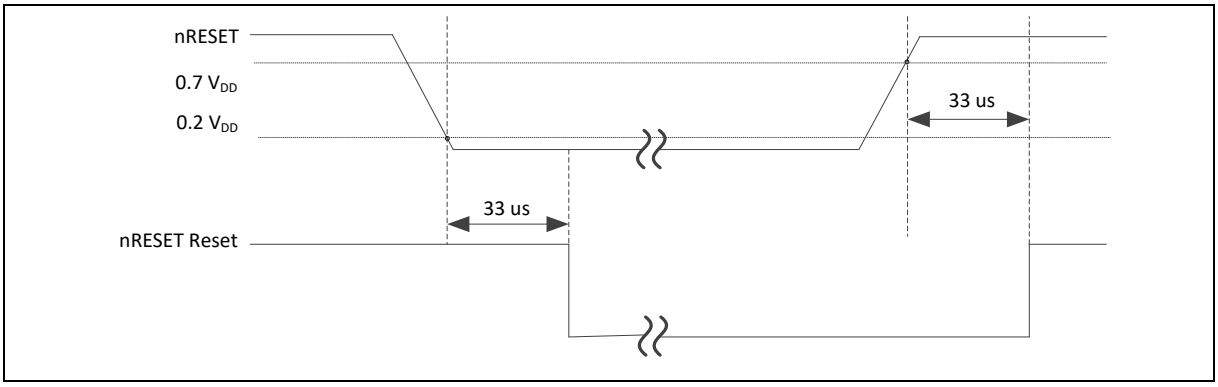


Figure 6.2-2 nRESET Reset Waveform

6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the power-on reset waveform.

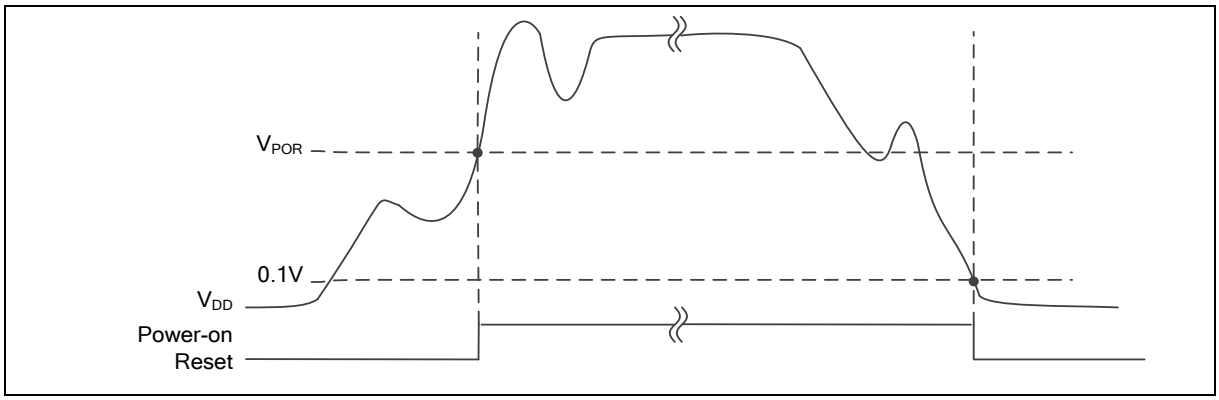


Figure 6.2-3 Power-on Reset (POR) Waveform

6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-4 shows the Low Voltage Reset waveform.

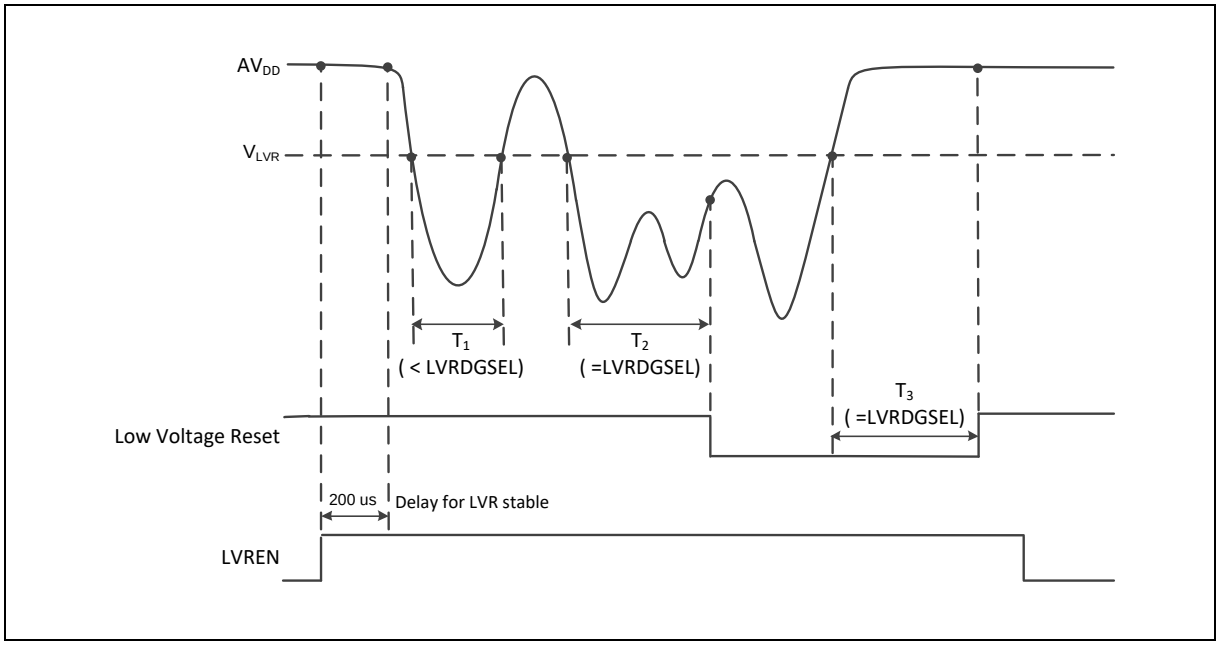


Figure 6.2-4 Low Voltage Reset (LVR) Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN and BODVL (SYS_BODCTL[16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. Figure 6.2-5 shows the Brown-out Detector waveform.

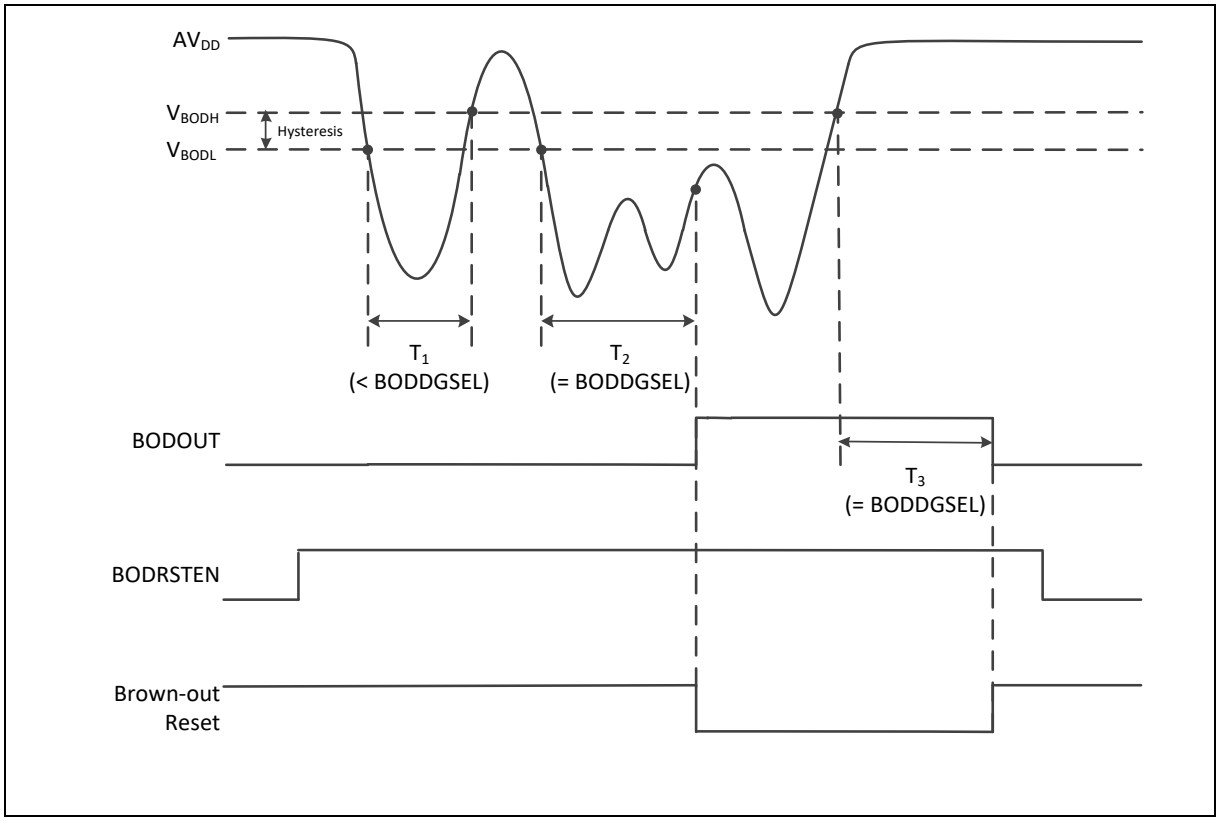


Figure 6.2-5 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M0 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[0]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 System Power Distribution

In this chip, power distribution is divided into three segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8V power for digital operation and I/O pins.
- M030G/M031G package connect AV_{SS} and V_{SS} together.

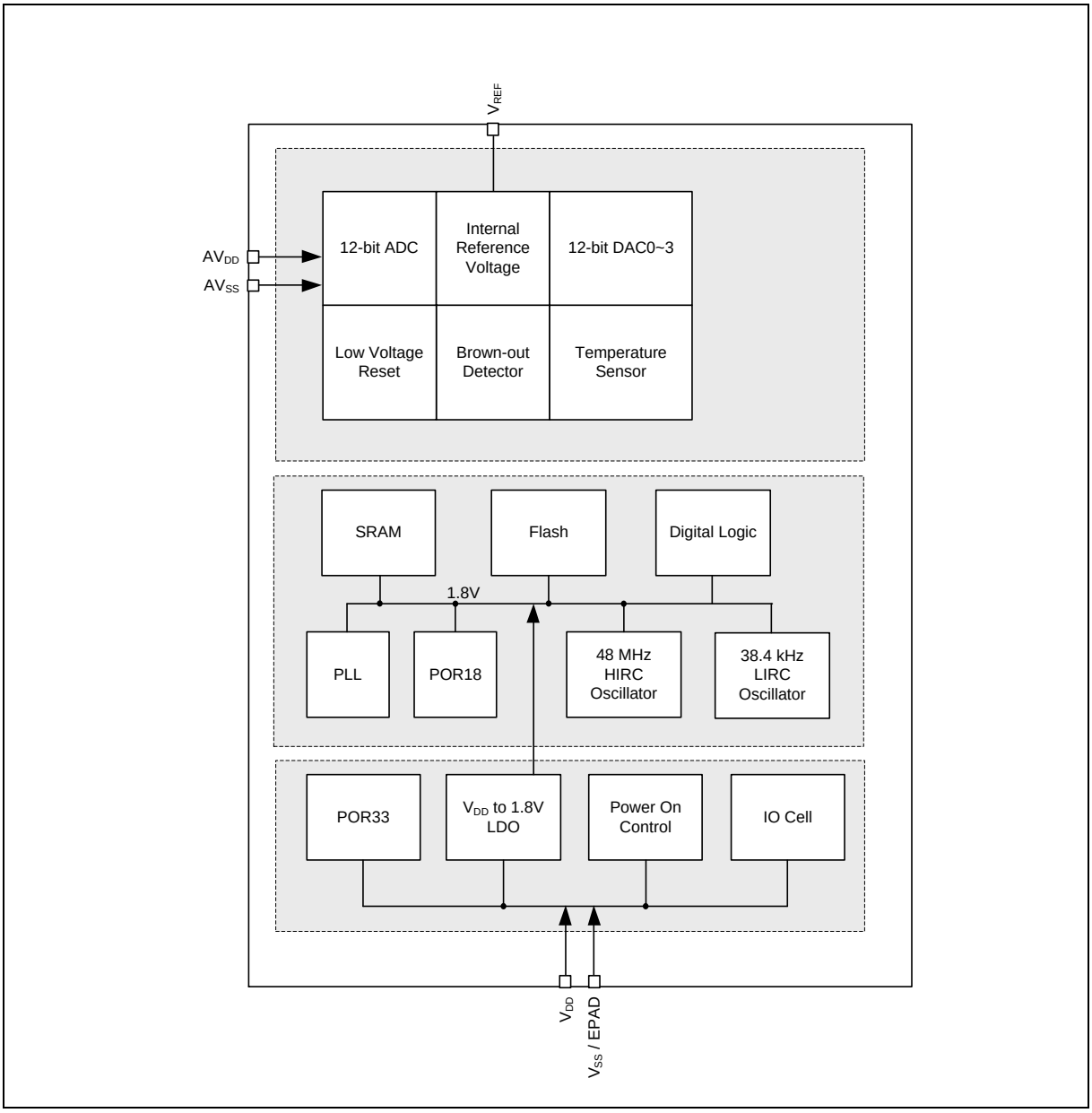


Figure 6.2-6 NuMicro® M030G/M031G Power Distribution Diagram

6.2.4 Power Modes and Wake-up Sources

This chip has a power manager unit to support several operating modes for saving power. Table 6.2-4 lists all power modes in the M030G/M031G series.

Mode	CPU Operating Maximum Speed (MHz)	LDO (V)	Clock Disable
Normal mode	72/48	1.8	All clocks are disabled by control register.
Idle mode	CPU enters Sleep mode	1.8	Only CPU clock is disabled.
Power-down mode	CPU enters Power-down mode	1.8	All clocks are disabled, except LIRC. And only WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC.

Table 6.2-4 Power Mode Table

There are different power mode entry settings and leaving condition for each power mode. Table 6.2-5 shows the entry setting for each power mode. When chip power-on, chip is running in normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCTL[7]) and execute WFI instruction.

Register/Instruction Mode	SLEEPDEEP (SCR[2])	PDEN (CLK_PWRCTL[7])	CPU Run WFI Instruction
Normal mode	0	0	NO
Idle mode (CPU enters Sleep mode)	0	0	YES
Power-down mode (CPU enters Deep Sleep mode)	1	1	YES

Table 6.2-5 Power Mode Entry Setting Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-6 lists the available clocks for each power mode.

	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	WDT, I²C, Timer, UART, BOD, GPIO and EINT
Available Clocks	All	All except CPU clock	LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-6 Power Mode Difference Table

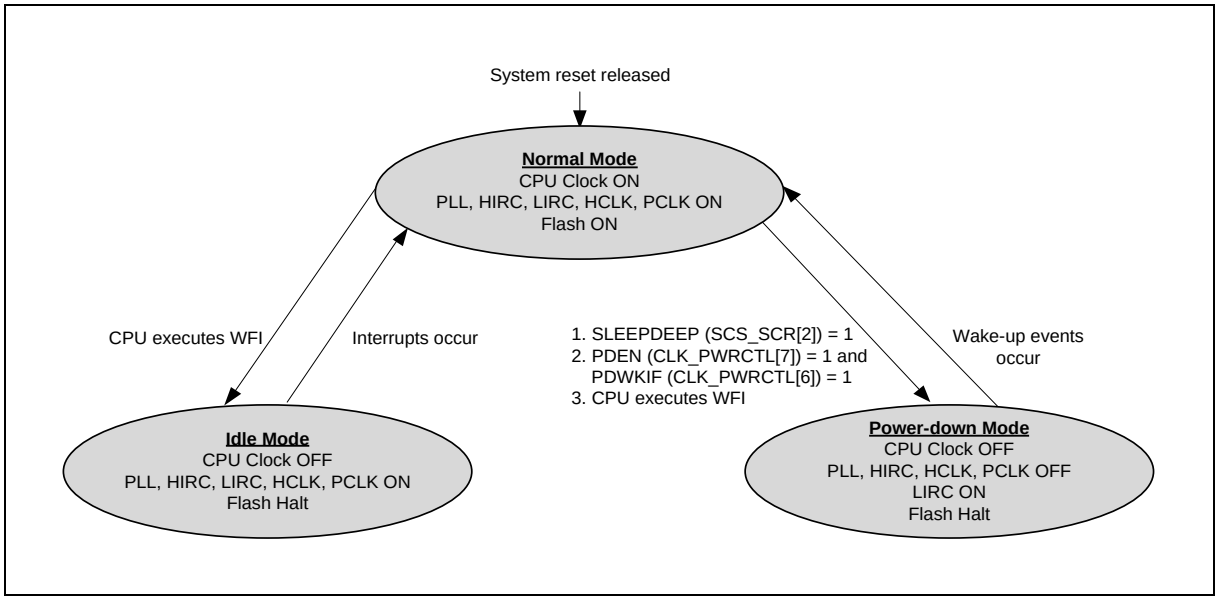


Figure 6.2-7 Power Mode State Machine

	Normal Mode	Idle Mode	Power-Down Mode
HIRC48 (48 MHz OSC)	ON	ON	Halt
LIRC (38.4 kHz OSC)	ON	ON	ON
PLL	ON	ON	Halt
HCLK/PCLK	ON	ON	Halt
CPU	ON	Halt	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON	Halt
TIMER	ON	ON	ON/OFF[1]
WDT	ON	ON	ON/OFF[2]
UART	ON	ON	ON/OFF[3]
Others	ON	ON	Halt

Table 6.2-7 Clocks in Power Modes

Note:

1. If TIMER clock source is selected as LIRC.
2. If WDT clock source is selected as LIRC.
3. If UART clock source is selected as LIRC.

Wake-up sources in Power-down mode:

WDT, I²C, Timer, UART, BOD and GPIO

After chip enters power down, the following wake-up sources can wake up chip to normal mode. Table 6.2-8 lists the condition about how to enter Power-down mode again for each peripheral.

User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	System Can Enter Power-Down Mode Again Condition
BOD	Brown-Out Detector Interrupt	After software writes 1 to clear BODIF (SYS_BODCTL[4]).
INT	External Interrupt	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO	GPIO Interrupt	After software write 1 to clear the Px_INTSRC[n] bit.
TIMER	Timer Interrupt	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
WDT	WDT Interrupt	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
UART	nCTS wake-up	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
I^2C	Address match	After software writes 1 to clear WKIF (I2C_WKSTS[0]).

Table 6.2-8 Condition of Entering Power-down Mode Again

6.2.5 System Memory Map

This chip provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-9. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The M030G/M031G series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0000_FFFF	FLASH_BA	FLASH Memory Space (64 Kbytes)
0x2000_0000 – 0x2000_1FFF	SRAM_BA	SRAM Memory Space (8 Kbytes)
Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers
0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_8000 – 0x4000_8FFF	PDMA_BA	Peripheral DMA Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers
APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_0FFF	WDT_BA	Watchdog Timer Control Registers
0x4004_3000 – 0x4004_3FFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
0x4004_7000 – 0x4004_7FFF	DAC01_BA	DAC01 Control Registers
0x4004_B000 – 0x400B_7FFF	DAC23_BA	DAC23 Control Registers
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers

0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_2000 – 0x4005_2FFF	TMR45_BA	Timer4/Timer5 Control Registers
0x4005_B000 – 0x4005_BFFF	BPWM1_BA	BPWM Control Registers
0x4006_1000 – 0x4006_1FFF	SPI0_BA	SPI0 Control Registers
0x4007_0000 – 0x4007_0FFF	UART_BA	UART0 Control Registers
0x4008_0000 – 0x4008_0FFF	I2C0_BA	I2C0 Control Registers
0x4008_1000 – 0x4008_1FFF	I2C1_BA	I2C1 Control Registers
0x400B_C000 – 0x400B_CFFF	MANCH_BA	Manchester Codec Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-9 Address Space Assignments for On-Chip Controllers

6.2.6 SRAM Memory Organization

This chip supports embedded 4/8 Kbytes size SRAM:

- Supports 4/8 Kbytes SRAM
- Supports byte / half word / word write
- Supports oversize response error

Figure 6.2-8 shows the M030G/M031G series SRAM organization. The address between 0x2000_2000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

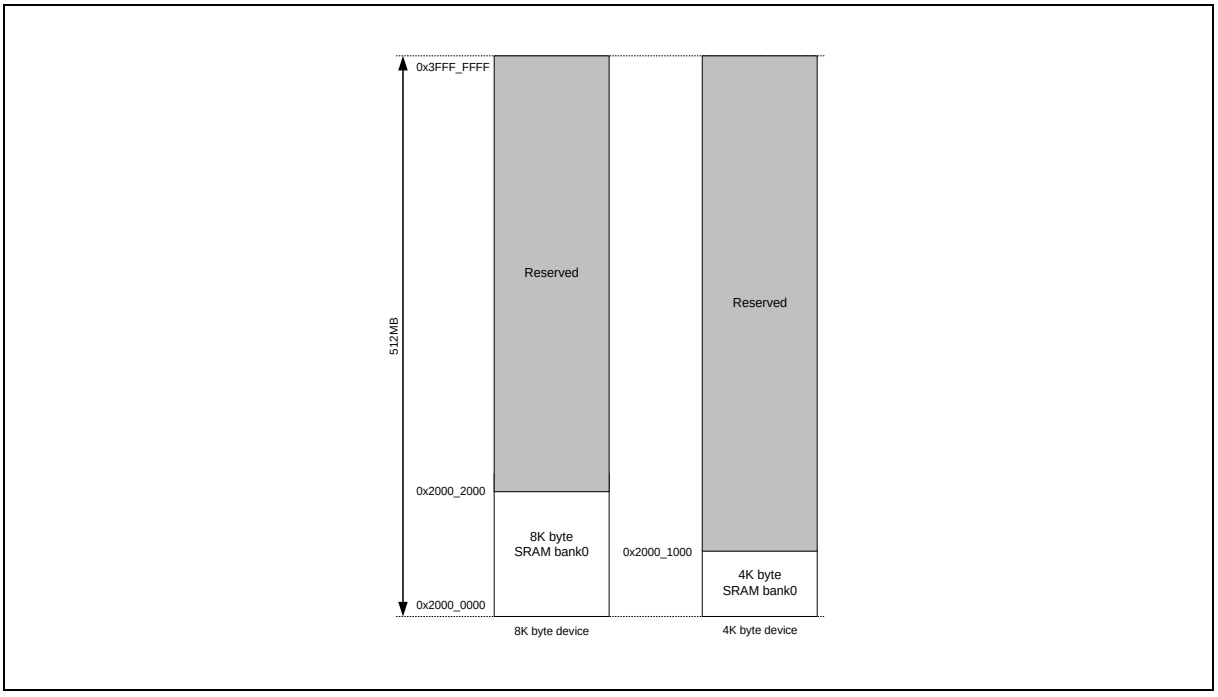


Figure 6.2-8 SRAM Memory Organization

6.2.7 Chip Bus Matrix

This chip supports Bus Matrix to manage the access arbitration between masters. The access arbitration uses round-robin algorithm as the bus priority.

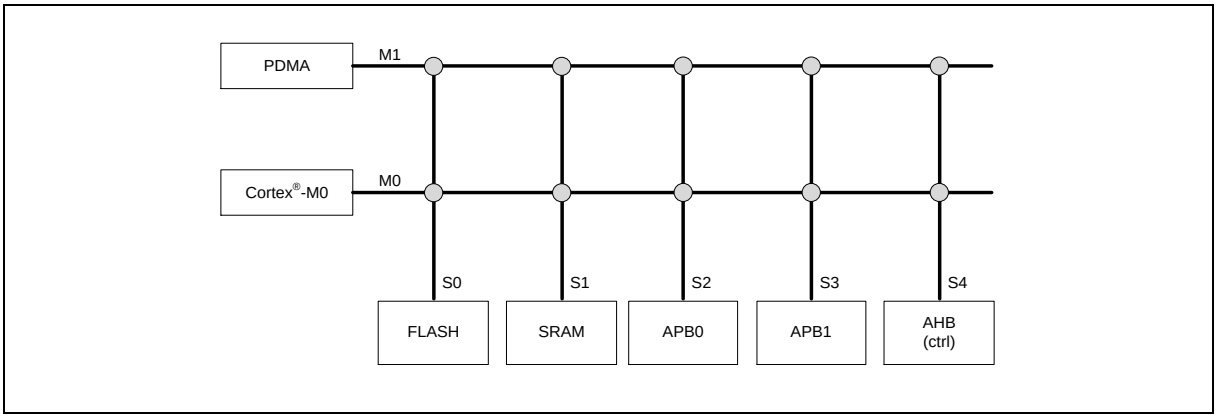


Figure 6.2-9 NuMicro® M030G/M031G Bus Matrix Diagram

6.2.8 Temperature Sensor

This chip is equipped with an on-chip temperature sensor. Temperature sensor control registers are located in SYS_TSCTL and SYS_TSDATA.

User should set both TSEN(SYS_TSCTL[0]) and TSBGEN(SYS_TSCTL[1]) bits to 1 to enable the temperature sensor. User needs to wait 200us for temperatre sensor to be stable, and then set TSST(SYS_TSCTL[2]) bit to 1 to start temperature sensor conversion.

After temperature sensor conversion is finished, TSEOC(SYS_TSDATA[0]) bit will be set to 1 automatically, and TSDATA(SYS_TSDATA[27:16]) will present the temperature sensor data. Figure 6.2-10 shows the timing waveform of temperature sensor conversion.

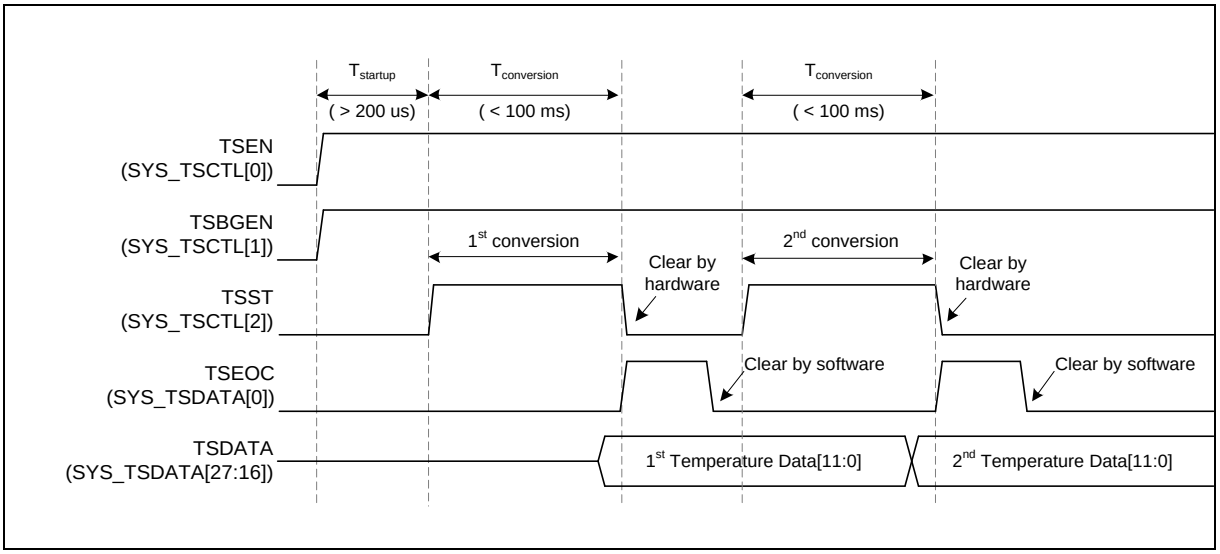


Figure 6.2-10 Temperature Sensor Conversion Waveform

Table 6.2-10 is a reference table for the relationship between temperature and TSDATA. Negative temperature is represented in TSDATA(SYS_TSDATA[27:16]) by twos complement format, and per LSB difference is equivalent to 0.0625 ° C.

Temperature (°C)	Temperature Data (TSDATA)
128	0x7FF
127.9375	0x7FF
100	0x640
80	0x500
75	0x4B0
50	0x320
25	0x190
0.25	0x004
0	0x000
-0.25	0xFFC
-25	0xE70
-55	0xC90

Table 6.2-10 Temperature Data Truth Table

6.2.9 Internal Voltage Reference (INT_VREF)

This chip supports internal voltage reference (INT_VREF) to provide the voltage reference for ADC and DACs. The INT_VREF routes to V_{REF} pin. User can set VREFEN(SYS_VREFCTL[0]) to select ADC and DACs reference voltage sourcing from external V_{REF} pin supply or internal INT_VREF. If using external V_{REF} source, VREFEN needs to be set to 0, and INT_VREF will output floating.

When VREFEN is set to 1, INT_VREF will be enabled. In addition, user can select INT_VREF output voltage level 2.048V or 2.5V by VREFSEL(SYS_VREFCTL[1]). However, VREFSEL must be decided before VREFEN is set to 1.

When VREFEN is set to 1, PRELOADEN(SYS_VREFCTL[6]) will be set automatically to shorten V_{REF} discharge and stable time. User needs to disable PRELOADEN function after stable time, otherwise it will affect the maximum load current that INT_VREF can provide.

6.2.10 MANCH_TXD Modulation with BPWM1

This chip supports MANCH_TXD to modulate with BPWM1_CH0 ~ BPWM1_CH5. User can set MANCHMODEN (SYS_MODCTL[21:16]) to enable modulation function with each BPWM1 channel and set MANCHMODL (SYS_MODCTL[29:24]) to select MANCH_TXD data high or low to modulate with

BPWM1 channels. The Manchester modulation example waveform is shown in Figure 6.2-11.

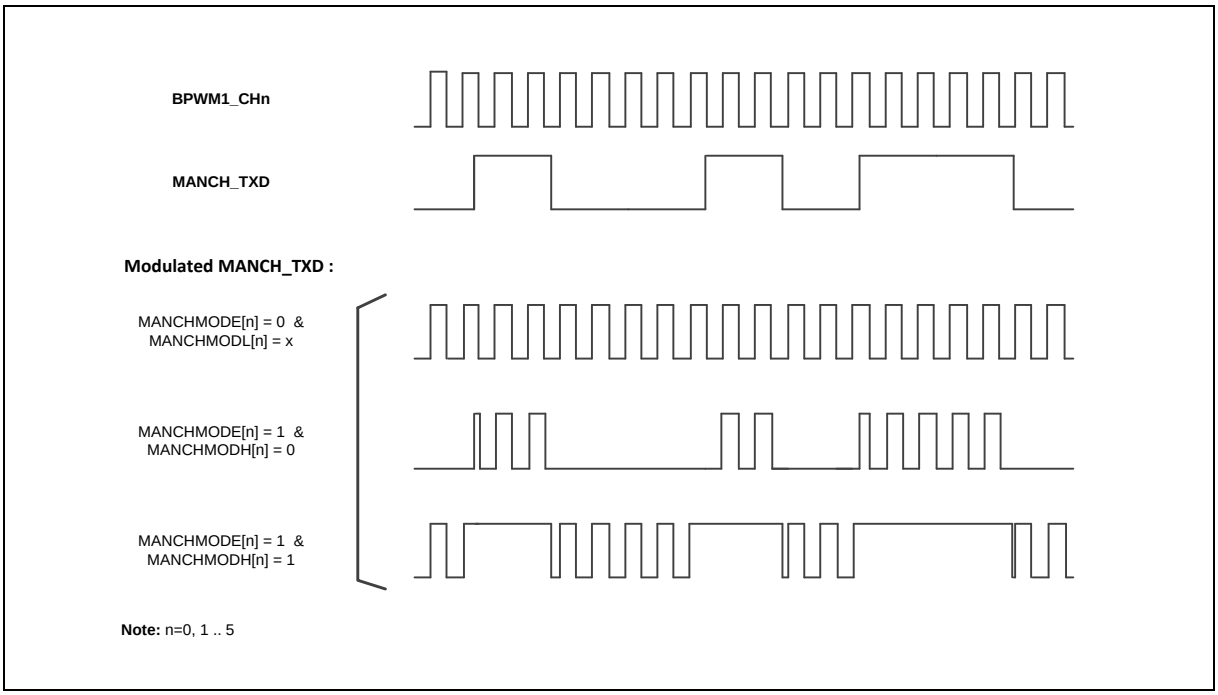


Figure 6.2-11 MANCH_TXD Modulated with BPWM1_CHn

6.2.11 Register Lock Control

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x4000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence. All proteced control registers are noted “(Write Protect)” and add an note “**Note:** This bit is write protected. Refer to the SYS_REGLCTL register “ in register description field.

6.2.12 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “Arm® Cortex®-M0 Technical Reference Manual” and “Arm® v6-M Architecture Reference Manual”.

6.2.13 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)", which is closely coupled to the processor core and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "*Arm® Cortex®-M0 Technical Reference Manual*" and "*Arm® v6-M Architecture Reference Manual*".

6.2.13.1 Exception Model and System Interrupt Map

Table 6.2-11 lists the exception model supported by the M030G/M031G series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as "0" and the lowest priority is denoted as "3". The default priority of all the user-configurable interrupts is "0". Note that priority "0" is treated as the fourth priority on the system, after three system exceptions "Reset", "NMI" and "Hard Fault".

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6.2-11 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BODOUT	Brown-Out low voltage detected interrupt
17	1	WDT_INT	Watchdog Timer interrupt
18	2	EINT024	External interrupt fromEINT0,2,4.
19	3	EINT135	External interrupt fromEINT1.3.5
20	4	GPAB_INT	External interrupt from PA, PB pin
21	5	GPCF_INT	External interrupt from PC, PF pin
22	6	TMR4_INT	Timer 4 interrupt
23	7	TMR5_INT	Timer 5 interrupt
24	8	TMR0_INT	Timer 0 interrupt
25	9	TMR1_INT	Timer 1 interrupt
26	10	TMR2_INT	Timer 2 interrupt
27	11	TMR3_INT	Timer 3 interrupt
28	12	UART0_INT	UART0 interrupt
29	13	Reserved	Reserved
30	14	SPI0_INT	SPI0 interrupt
31	15	Reserved	Reserved
32	16	Reserved	Reserved

33	17	MANCH_INT	Manchester Codec interrupt
34	18	I2C0_INT	I2C0 interrupt
35	19	I2C1_INT	I2C1 interrupt
36	20	Reserved	Reserved
37	21	BPWM_INT	BPWM interrupt
38	22	Reserved	Reserved
39	23	DAC01_INT	DAC0/1 device interrupt
40	24	DAC23_INT	DAC2/3 device interrupt
41	25	TEMP_INT	TEMP interrupt
42	26	PDMA_INT	PDMA interrupt
43	27	Reserved	Reserved
44	28	PWRWU_INT	Clock controller interrupt for chip wake-up from power-down state
45	29	ADC_INT	ADC interrupt
46	30	Reserved	Reserved
47	31	Reserved	Reserved

Table 6.2-12 Interrupt Number Table

6.2.13.2 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For Armv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 6.2-13 Vector Figure Format

6.2.13.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not be activated. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution

status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M0 core executes the WFI instruction. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 48 MHz internal high speed RC oscillator (HIRC) and Programmable PLL output clock frequency (PLLFOUT) to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.

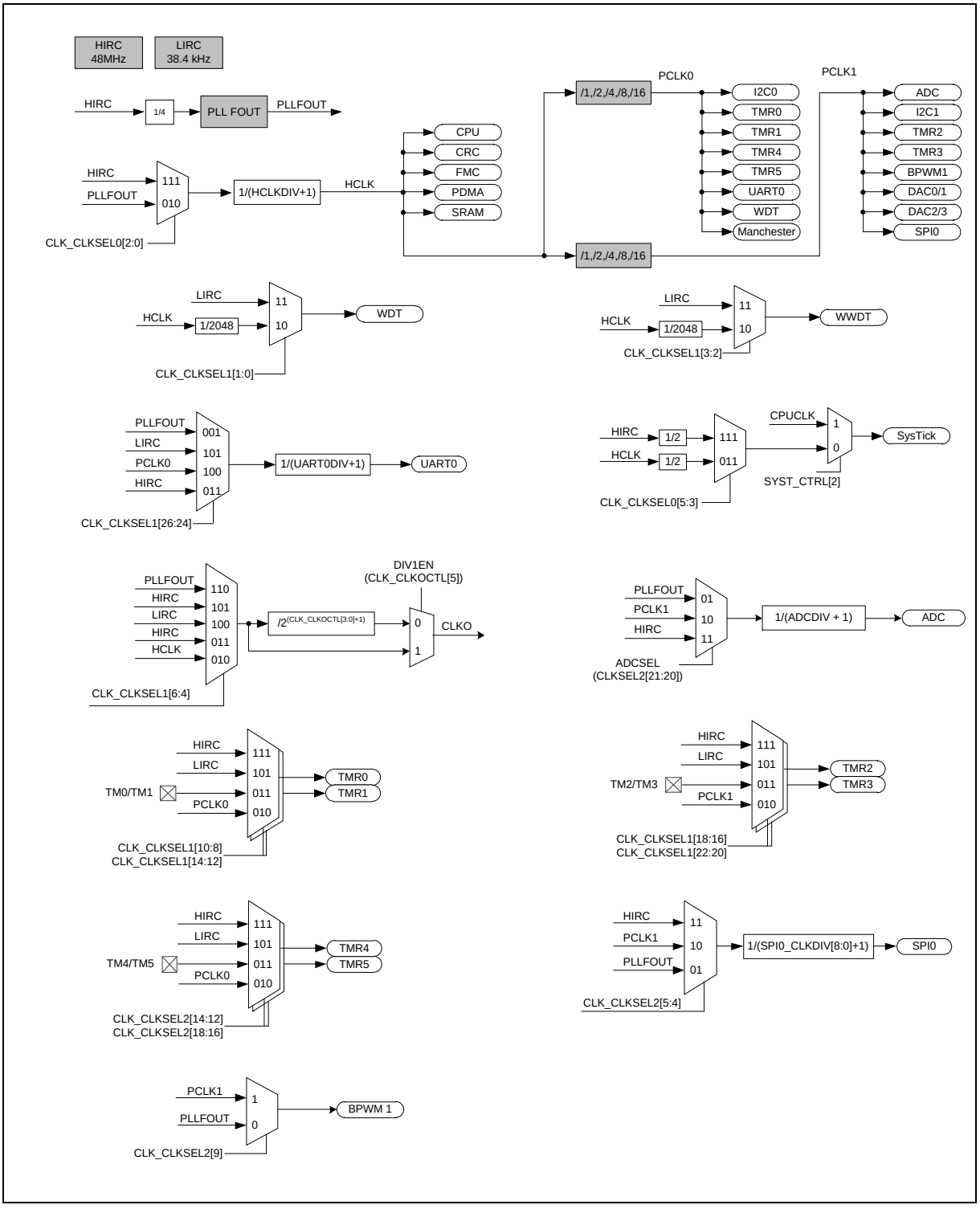


Figure 6.3-1 Clock Generator Global View Diagram

6.3.2 Clock Generator

The clock generator consists of 2 clock sources, which are listed below:

- 48 MHz internal high speed RC oscillator (HIRC)
- Programmable PLL output clock frequency (PLLFOUT) – PLL source is selected from 48 MHz internal high speed oscillator (HIRC/4)
-

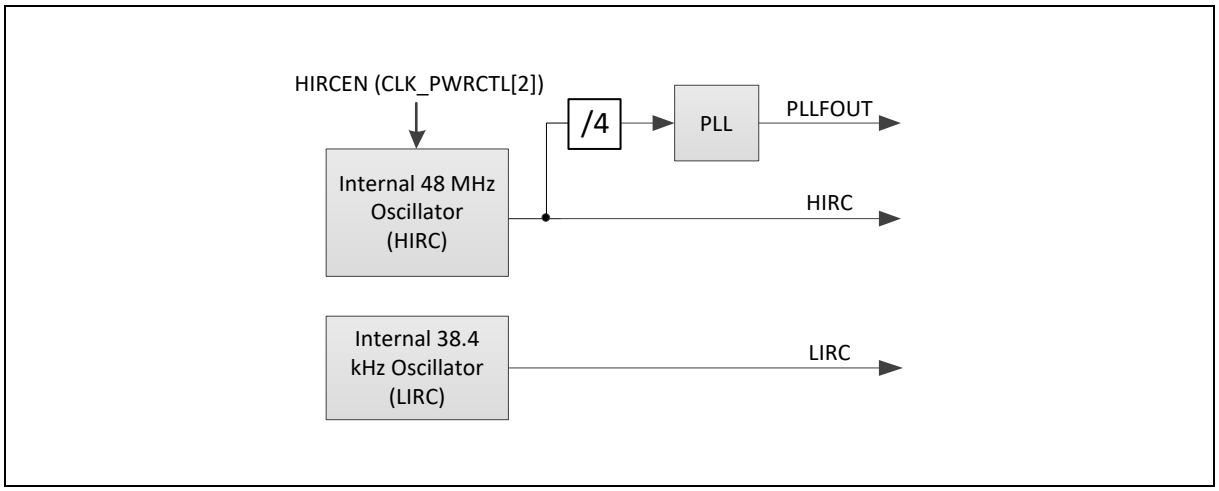


Figure 6.3-2 Clock Generator Block Diagram

6.3.3 System Clock and SysTick Clock

The system clock has 2 clock sources generated from clock generator block The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-3.

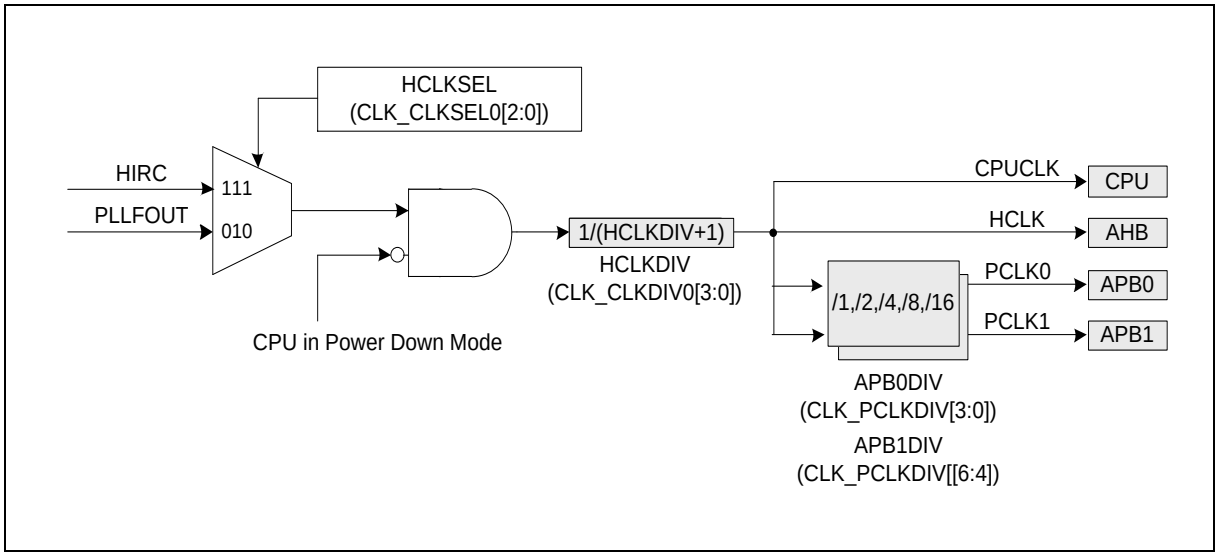


Figure 6.3-3 System Clock Block Diagram

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 2 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-4.

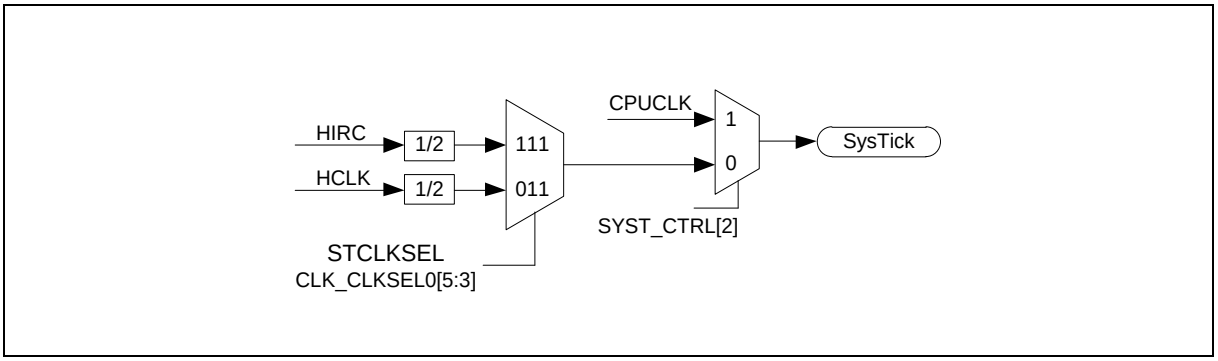


Figure 6.3-4 SysTick Clock Control Block Diagram

6.3.4 Peripherals Clock

The peripherals clock has different clock source switch setting, which depends on the different peripheral. Please refer to the CLK_CLKSELx register description.

6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

The clock that is still kept active is listed below:

- Peripherals Clock (when the modules adopt LIRC as clock source)

6.3.6 Clock Output

This device is equipped with a power-of-2 frequency divider composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore, there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

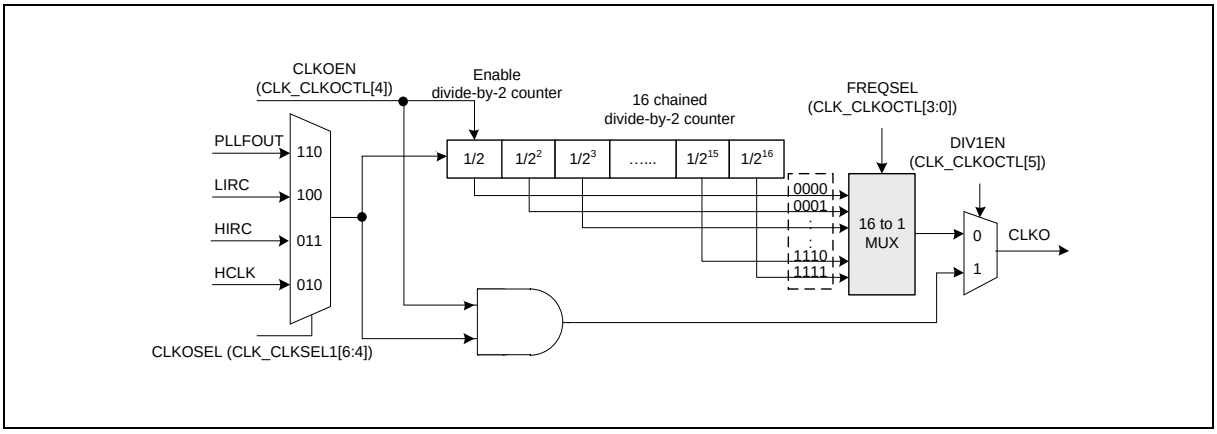


Figure 6.3-5 Clock Output Block Diagram

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

This chip is equipped with 32/64 Kbytes on-chip embedded Flash. A User Configuration block is provided for system initialization. A loader ROM (LDROM) is used for In-System-Programming (ISP) function. A security protection ROM (SPROM) can conceal user program. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without the chip reset after the embedded Flash is updated.

6.4.2 Features

- Supports 32/64 Kbytes application ROM (APROM).
- Supports 512 bytes page size for 32/64 Kbytes Flash.
- Supports 2 Kbytes loader ROM (LDROM).
- Supports configurable Data Flash size to share with APROM.
- Supports 512 bytes security protection ROM (SPROM) to conceal user program.
- Supports 12 bytes User Configuration block to control system initialization.
- Supports 512 bytes page erase for all embedded Flash.
- Supports CRC-32 checksum calculation function.
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory.

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

This chip has up to 28 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 28 pins are arranged in 4 ports named as PA, PB, PC, PF. PA has 8 pins on port. PB has 16 pins on port. PC has 1 pin on port. PF has 3 pins on port. Each of the 28 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are dependent on CIOINI (CONFIG0[10]).

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- I/O pin can be configured as interrupt source with edge/level setting
- Input schmitt trigger function
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in input mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Supports independent pull-up control
- Enabling the pin interrupt function will also enable the wake-up function
- Supports 5V-tolerance function except analog I/O (PA0~PA3, PB0~15, PF0)
- GPIO output can be configured to retention when system reset

6.6 PDMA Controller (PDMA)

6.6.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 7 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.6.2 Features

- Supports 7 independently configurable channels
- Selectable 2 level of priorities (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size to be byte, half-word, word or no increment
- Supports software and I^2C, SPI, UART, ADC, DAC, MANCH and TIMER request
- Supports Scatter-Gather mode to implement complex transmission by using descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on channel 0 and channel1

6.7 Timer Controller (TMR)

6.7.1 Overview

The timer controller includes up to six 32-bit timers, Timer0 ~ Timer5, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.7.2 Features

6.7.2.1 *Timer Function Features*

- Up to six sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports internal capture triggered while LIRC transition
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer5 time-out interrupt signal or capture interrupt signal to trigger ADC, DAC, PDMA, BPWM function
- Supports Inter-Timer trigger mode

6.8 Watchdog Timer (WDT)

6.8.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer also supports the function to wake up system from Idle/Power-down mode.

6.8.2 Features

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{20}) and the time-out interval is 416us ~ 27.3 s if WDT_CLK = 38.4 kHz (LIRC)
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC

6.9 Window Watchdog Timer (WWDT)

6.9.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.9.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.10 Basic PWM Generator and Capture Timer (BPWM)

6.10.1 Overview

This chip provides one BPWM generator (BPWM1). BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for ADC, DAC to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.10.2 Features

6.10.2.1 BPWM Function Features

- Supports maximum clock frequency up to 144 MHz
- Supports one BPWM modules and provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter, the module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger DAC
- Supports trigger ADC in the following events:
  - BPWM counter matches 0, period value or compared value

6.10.2.2 Capture Function Features

- Supports up to 6 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.11 UART Interface Controller (UART)

6.11.1 Overview

The chip provides one channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs serial-to-parallel conversion on data received from the peripheral and parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller supports flow control function. The UART controller also supports IrDA SIR, RS-485, and Single-wire function modes and auto-baud rate measuring function.

6.11.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 1/1 byte entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS and incoming data wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT[15:8])
- Supports Auto-Baud Rate measurement function
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function
- Support Single-wire function mode

UART Feature		UART0	
FIFO		1 Bytes	
Auto Flow Control (CTS/RTS)		√	
IrDA		√	
LIN		-	
RS-485 Function Mode		√	
nCTS Wake-up		√	
Incoming Data Wake-up		√	
Received Data FIFO reached threshold Wake-up		-	
RS-485 Address Match (AAD mode) Wake-up		-	
Auto-Baud Rate Measurement		√	
STOP Bit Length		1, 1.5, 2 bit	
Word Length		5, 6, 7, 8 bits	
Even / Odd Parity		√	
Stick Bit		√	

Table 6.11-1 NuMicro® M030G/M031G Series UART Features

6.12 Serial Peripheral Interface (SPI)

6.12.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains one set of SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer.

6.12.2 Features

- SPI Mode
  - Supports one set of SPI controller
  - Supports Master or Slave mode operation
  - Configurable bit length of a transaction word from 8 to 32-bit
  - Provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers which depends on SPI setting of data width
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Master mode up to 24 MHz and Slave mode up to 16 MHz (when chip works at V_{DD} = 1.8~3.6V)
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
  - Supports PDMA transfer

6.13 I²C Serial Interface Controller (I²C)

6.13.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are two sets of I²C controllers that support Power-down wake-up function.

6.13.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to two I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports two-level buffer function (only supported in slave mode)
- Supports setup/hold time programmable

6.14 CRC Controller (CRC)

6.14.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

6.14.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

6.15 CRC Controller (CRC) - Configurable

6.15.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with 8-bits, 16-bits and 32-bits configurable polynomials.

6.15.2 Features

- Supports 8-bits, 16-bits and 32-bits configurable polynomials
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

6.16 Manchester Controller (MANCH)

6.16.1 Overview

The Manchester code is used to transmit a plenty of continuous data in a single bus without synchronous clock. In each encoded data bit, there is an edge transition in the middle to synchronize the internal clock. Hence, the clock deviation between receiver and transmitter will not affect the communication.

The Manchester Controller supports encode and decode function with at least 2 modulation signal formats (Mode 1 and Mode 2). The Manchester Controller also supports programmable format. The format of the preamble of the data packet and the idle pattern of bus can be defined. The Manchester Controller supports three 4-level FIFO for transmit, encoded and decoded data. To read/write the data from/into FIFO, PDMA can be used and combined with other peripherals. The Manchester encoded edge function can also trigger Timer Controller and interconnect with PDMA and DAC.

6.16.2 Features

- Supports encode/decode Manchester code
- Supports different modulation signal format
  - Mode 1
  - Mode 2
  - Programmable format
    - Programmable Idle pattern
    - Programmable preamble style and its transmitted number
    - Programmable data size in a frame
- Supports configurable Manchester bit rate
- Supports selectable deglitch time function
- Supports three 4-level FIFO for transmit, encoded and decoded data
- Supports PDMA for data receiving/transmitting individually
- Supports Manchester encoded edge function to trigger Timer Controller
- Supports bit detect error, receive FIFO overflow, receive frame done and transmit frame done interrupt

6.17 Analog-to-Digital Converter (ADC)

6.17.1 Overview

The ADC contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with 16 input channels. The A/D converter supports four operation modes: Single, Burst, Single-cycle Scan and Continuous Scan mode. The A/D converter can be started by software, external pin (STADC), timer0~timer5 overflow pulse trigger or BPWM trigger.

6.17.2 Features

- Operating voltage: 1.8V~3.6V.
- Analog input voltage: 0 ~ AV_{DD}.
- Supports external reference voltage from V_{REF} pin.
- 12-bit resolution and 10-bit accuracy is guaranteed.
- Up to 16 single-end analog input channels or 8 differential analog input channels.
- Maximum ADC peripheral clock frequency is 34 MHz.
- Up to 1.4 MSPS sampling rate.
- Scan on enabled channels
- Threshold voltage detection
- Four operation modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO.
  - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software Write 1 to ADST bit
  - External pin (STADC)
  - Timer 0~timer5 overflow pulse trigger
  - BPWM trigger
- Each conversion result is held in data register of each channel with valid and overrun indicators.
- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.
- Supports extend sample time function (0~255 ADC clock).
- One internal channel from band-gap voltage (V_{BG}).
- One internal channel from internal pull-up/down circuit.
- Supports PDMA transfer mode.
- Supports Calibration mode.
- Supports Floating Detect Function

Note1: ADC sampling rate = (ADC peripheral clock frequency) / (total ADC conversion cycle)

Note2: If the internal channel for band-gap voltage is active, the maximum sampling rate will be 300 KSPS.

Note3: The ADC Clock frequency must be slower than or equal to PCLK.

6.18 Digital to Analog Converter (DAC)

6.18.1 Overview

The DAC module is a 12-bit, voltage output digital-to-analog converter. It can be configured to 12-or 8-bit output mode and can be used in conjunction with the PDMA controller. The DAC integrates a voltage output buffer that can be used to reduce output impendence and drive external loads directly without having to add an external operational amplifier.

6.18.2 Features

- Analog output voltage range: 0~AV_{DD}.
- Supports 12-or 8-bit output mode.
- Rail to rail settle time 5us.
- Supports up to four 12-bit 1 MSPS voltage type DAC.
- Reference voltage from internal reference voltage (INT_VREF), V_{REF} pin.
- DAC maximum conversion updating rate 1 MSPS.
- Supports voltage output buffer mode and bypass voltage output buffer mode.
- Supports software and hardware trigger, including Timer0~5,BPWM1 trigger to start DAC conversion.
- Supports PDMA mode.
- Supports group mode of synchronized update capability for two DACs.
- DAC output can be configured to retention when system reset.

6.19 Peripherals Interconnection

6.19.1 Overview

Some peripherals have interconnections which allow autonomous communication or synchronous action between peripherals without needing to involve the CPU. Peripherals interact without CPU saves CPU resources, reduces power consumption, operates with no software latency and fast responds.

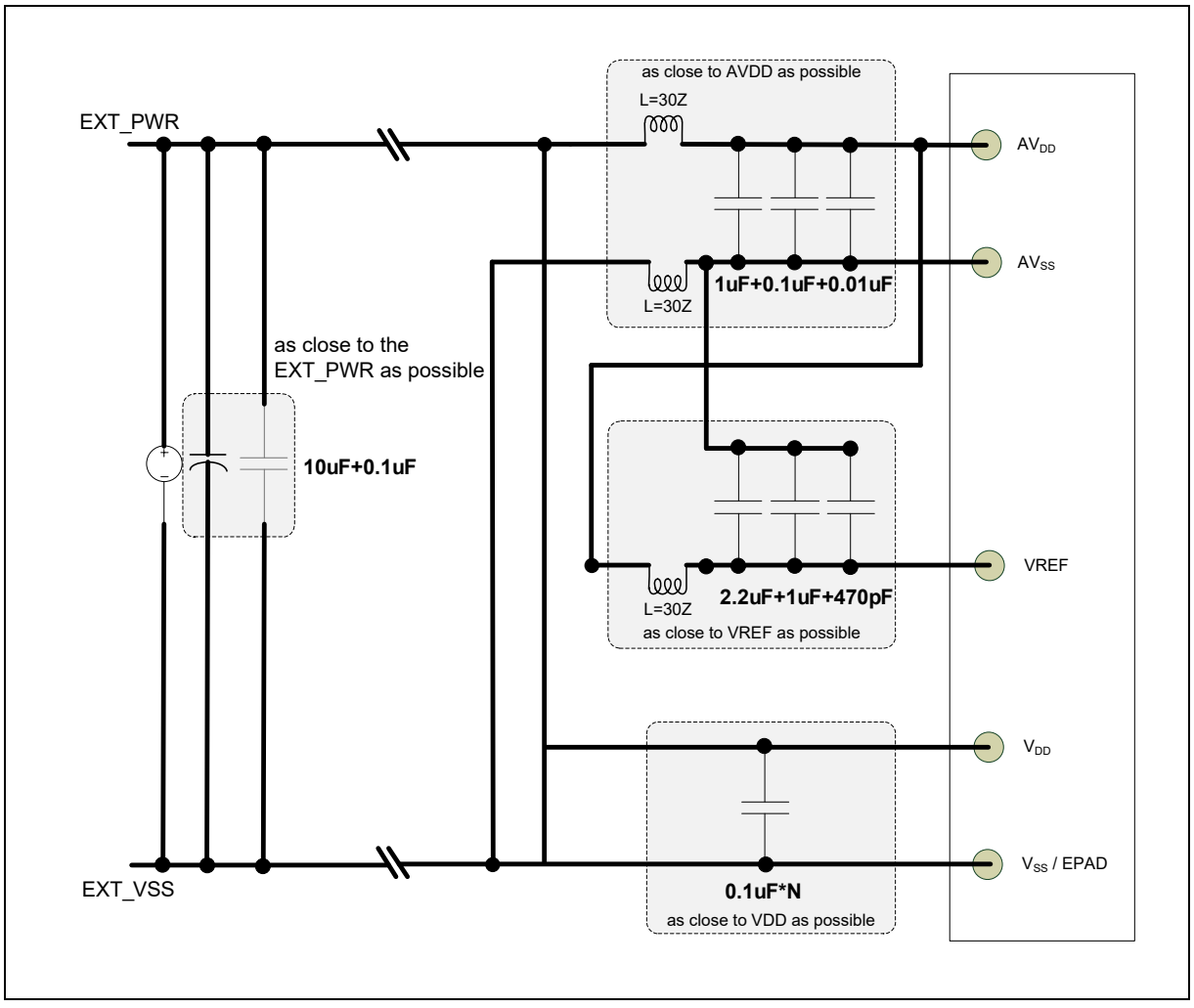
6.19.2 Peripherals Interconnect Matrix table

Source	Destination			
	ADC	DAC	PWM	Timer
LIRC	-	-	-	4
BPWM	1	2	-	-
Timer	1	2	3	5
Manchester Codec		6		7

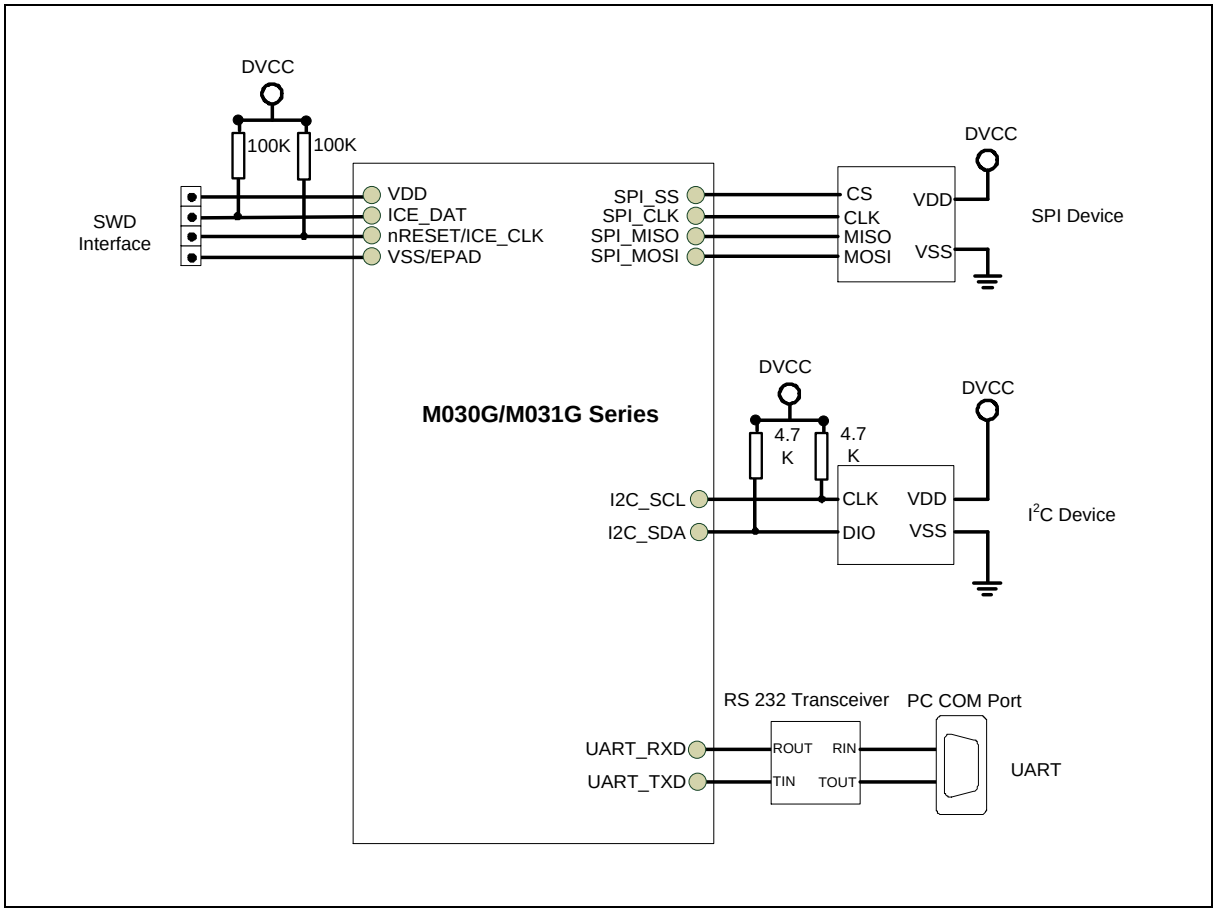
Table 6.19-1 Peripherals Interconnect Matrix table

7 APPLICATION CIRCUIT

7.1 Power Supply Scheme



7.2 Peripheral Application Scheme



8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	4.0	V
ΔV_{DD}	Variations between different power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on 5V-tolerance I/O	V_{SS}-0.3	5.5	V
	Input voltage on any other pin[*2]	V_{SS}-0.3	4.0	V

Note:

1. All main power (V_{DD}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.
2. Non 5V-tolerance I/O includes PA.0 ~ 3; PB.0 ~ 15; PF.0; nRESET pin. V_{IN} maximum value must be respected to avoid permanent damage. Refer to Table 8.1-2 for the values of the maximum allowed injected current

Table 8.1-1 Voltage Characteristics

8.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	150	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	100	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	20	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	
$I_{INJ(PIN)}$ [*3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [*3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by V_{IN}>A_{VDD} and a negative injection is caused by V_{IN}<V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current Characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (°C)
- θ_{JA} = thermal resistance junction-ambient (°C/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	°C
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[*1]	Thermal resistance junction-ambient 24-pin QFN(3x3 mm)	-	30	-	°C/Watt
	Thermal resistance junction-ambient 33-pin QFN(4x4 mm)	-	28	-	°C/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-3 Thermal Characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.1.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-7000	-	+7000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-1000	-	+1000	
LU[*3]	Pin current for latch-up[*3]	-400	-	+400	mA
V_{EFT}[*4]	Fast transient voltage burst	-4.4	-	+4.4	kV

Note:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test, the performace cretia class is 4A.

Table 8.1-4 EMC Characteristics

8.1.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been

opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
24-pin QFN(3x3 mm) [*1]	MSL 3
33-pin QFN(4x4 mm) [*1]	MSL 3

Note:

1. Determined according to IPC/JEDEC J-STD-020

Table 8.1-5 Package Moisture Sensitivity (MSL)

8.1.6 Soldering Profile

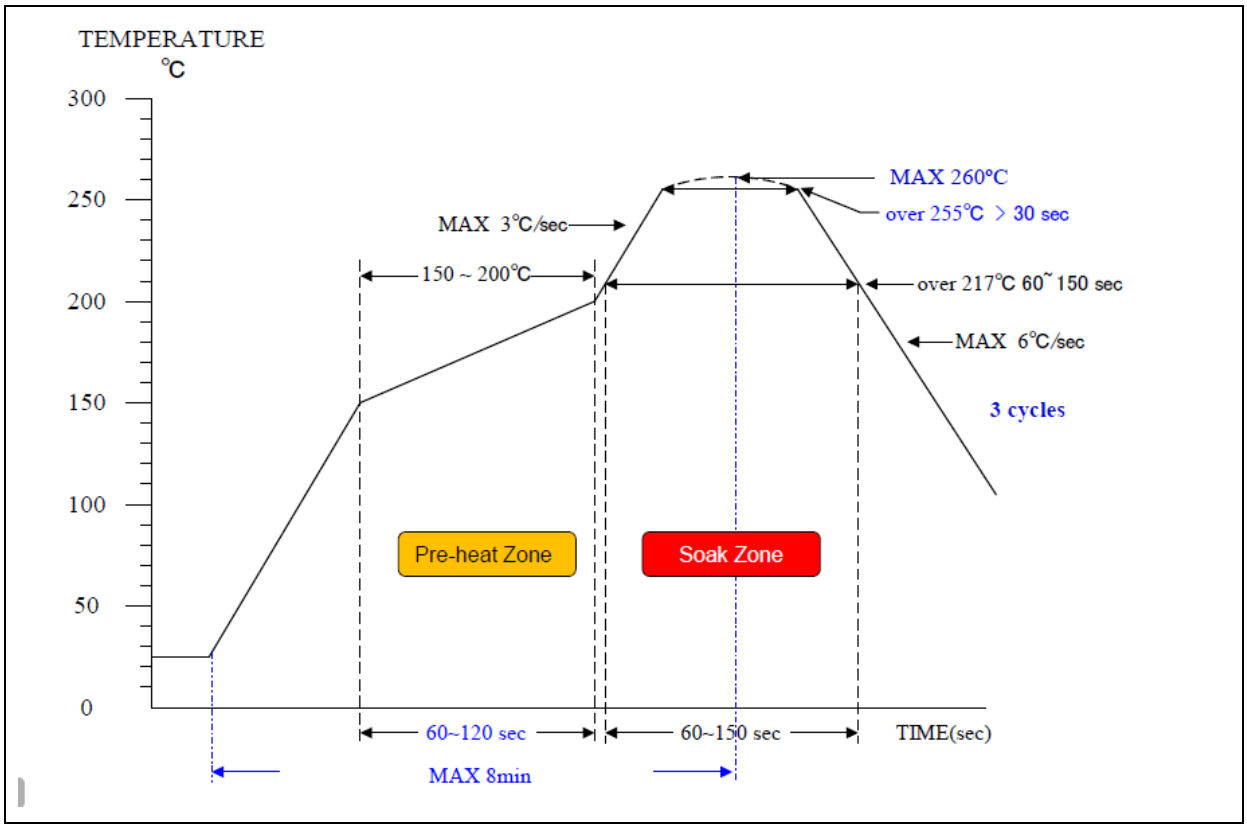


Figure 8.1-1 Soldering Profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217°C to peak)	3°C/sec. max
Preheat temperature 150°C ~200°C	60 sec. to 120 sec.
Temperature maintained above 217°C	60 sec. to 150 sec.
Time with 5°C of actual peak temperature	> 30 sec.
Peak temperature range	260°C
Ramp-down rate	6°C/sec ax.
Time 25°C to peak temperature	8 min. max
Note: 1.Determined according to J-STD-020C	

Table 8.1-6 Soldering Profile

8.2 General Operating Conditions

(V_{DD}-V_{SS} = 2.7 ~ 3.6V, T_A = 25°C, HCLK = 48/72 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
f_{HCLK}	Internal AHB clock frequency	-	-	72	MHz	V_{DD} = 2.7V~3.6V
V_{DD}	Operation voltage	2.7	-	3.6	V	VDD > BOD detect voltage while chip power on [*4]
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{REF}	Analog reference voltage	2.048	-	AV_{DD}		V_{REF} <= AV_{DD} - 0.2V, when VREFEN (SYS_VREFCTL[0]) =1'b1. V_{REF} <= AV_{DD}, when VREFEN (SYS_VREFCTL[0]) =1'b0.
V_{BG}[*3]	Band-gap voltage	1.16	1.23	1.31		
T_{VBG_ADC}[*3]	ADC sampling time when reading the band-gap voltage	20	-	-	µS	
I_{RUSH}[*2]	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	150	200	mA	
E_{RUSH}[*2]	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	-	2.25	3.00	µC	V_{DD} = 2.7 V, T_A = 105 °C, I_{RUSH} = 150 mA for 15 us

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation.
2. Guaranteed by design, not tested in production
3. Based on characterization, not tested in production unless otherwise specified.
4. BOD brown-out detect function is default enabled and BODVL is set to 0. While chip power up, VDD and AVDD should higher than BOD detect voltage, otherwise, chip will remain at reset stage.

Table 8.2-1 General Operating Conditions

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 2.7V ~ 3.6 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK0, 1} = f_{HCLK}$.
- Program run while(1) code in Flash.

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode, executed from Flash, all peripherals disable HIRC, PLL clock	72 MHz	14.30	14.65	14.80	15.05	mA
		48 MHz	9.80	9.95	10.25	10.50	
		24 MHz	6.40	6.50	6.80	7.00	
		12 MHz	4.70	4.75	5.00	5.20	
		4 MHz	3.50	3.55	3.75	3.95	
	Normal run mode, executed from Flash, all peripherals enable HIRC, PLL clock	72 MHz	22.65	23.05	23.50	23.85	
		48 MHz	15.45	15.75	16.20	16.45	
		24 MHz	9.35	9.55	9.85	10.10	
		12 MHz	6.25	6.35	6.65	6.85	
		4 MHz	4.15	4.20	4.45	4.65	

Note:

1. When analog peripheral blocks such as ADC, DAC, Temperature Sensor, INT_VREF, PLL, HIRC are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-1 Current Consumption in Normal Run Mode

Symbol	Conditions	F_{HCLK}	Typ	Max[*1] [*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode, all peripherals disable HIRC, PLL clock	72 MHz	6.90	7.00	7.25	7.50	mA
		48 MHz	4.05	4.10	4.35	4.55	
		24 MHz	3.55	3.60	3.80	4.00	
		12 MHz	3.25	3.25	3.50	3.60	
		4 MHz	3.00	3.05	3.25	3.45	
	Idle mode, all peripherals enable HIRC, PLL clock	72 MHz	15.15	15.45	15.90	16.25	
		48 MHz	9.60	9.75	10.15	10.40	
		24 MHz	6.30	6.40	6.70	6.95	
		12 MHz	4.60	4.70	4.95	5.15	
		4 MHz	3.50	3.55	3.75	3.95	

Note:

1. When analog peripheral blocks such as ADC, DAC, Temperature Sensor, INT_VREF, PLL, HIRC are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-2 Current Consumption in Idle Mode

Symbol	Test Conditions	Typ[*1]	Max[*2][*3]			Unit
		T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_PD}	Power-down mode, all peripherals disable	1730	1820[*4]	2080	2350[*4]	µA
	Power-down mode, UART/Timer/WDT use LIRC	1730	1825	2085	2355	

Note:

1. V_{DD} = AV_{DD} = 3.3V, LVR23 enabled, POR disabled and BOD disabled.
2. Based on characterization, not tested in production unless otherwise specified.
3. When analog peripheral blocks such as ADC, DAC, Temperature Sensor, INT_VREF, PLL, HIRC are ON, an additional power consumption should be considered.
4. Based on characterization, tested in production.

Table 8.3-3 Chip Current Consumption in Power-down Mode

8.3.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = 3.3 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock, f_{HCLK} = 48 MHz, $f_{PCLK0, 1}$ = f_{HCLK}.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on

Peripheral	I_{DD}[*1]	Unit
PDMA	305	uA
ISP	0.1	
CRC	44	
WDT/WWDT	120	
TMR0	270	
TMR1	260	
TMR2	315	
TMR3	320	
TMR4	290	
TMR5	270	
CLKO	75	
I2C0	60	
I2C1	55	
SPI0	665	
UART0	505	
ADC[*2]	530	
BPWM1	615	
DAC0[*3]	85	
DAC1[*3]	70	
Manch. Codec	675	
Temperature Sensor[*4]	0.1	

Note:

1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the DAC is turned on, add an additional power consumption per DAC for the analog part.
4. Temperature Sensor doesn't have clock enable bit for this test item. When the Temperature Sensor is turned on, add an additional power consumption per Temperature Sensor for the analog part.

Table 8.3-4 Peripheral Current Consumption

8.3.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.3-5 is measured on a wakeup phase with a 48 MHz HIRC oscillator.

Symbol	Parameter	Typ	Max	Unit
t_{WU_IDLE}	Wakeup from IDLE mode	5	6	cycles
t_{WU_NPD}[*1][*2]	Wakeup from normal power down mode	13	-	µs

Note:

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3. Guaranteed by design.

Table 8.3-5 Low-power Mode Wakeup Timings

8.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below V_{SS} or above V_{DD} except 5V-tolenece I/O should be avoided during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current , but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to V_{DD}) to pins that include analog function which may potentially injection currents.

Symbol	Parameter	Negative injection	Positive injection	Unit	Test Condition
$I_{INJ(PIN)}$	Injected current by a I/O Pin	-0	0	mA	Injected current on nReset pins
		-0	0		Injected current on PA0~PA3 and PB0~PB15 for analog input function
		-5	+5		Injected current on any other 5V-tolerance I/O

Table 8.3-6 I/O Current Injection Characteristics

8.3.5 I/O DC Characteristics

8.3.5.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage	0	-	$0.3*V_{DD}$	V	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{HY}[*1]	Hysteresis voltage of schmitt input	-	$0.2*V_{DD}$	-	V	
I_{LK}[*2]	Input leakage current	-1	-	1	µA	$V_{SS} < V_{IN} < V_{DD}$, Open-drain or input only mode
		-1	-	1		$V_{DD} < V_{IN} < 5$ V, Open-drain or input only mode on any other 5v tolerance pins
R_{PU}[*1]	Pull up resistor	32	38	54	kΩ	VDD = 3.6 V, Input mode
		45	60	79		VDD = 2.7 V, input mode

Note:
1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.

Table 8.3-7 I/O Input Characteristics

8.3.5.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[*1] [*2]	Source current for quasi-bidirectional mode and high level	-25.5	-28	-32	μA	V_{DD} = 3.3 V V_{IN}=(V_{DD}-0.4) V
		-18	-22	-24	μA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
	Source current for push-pull mode and high level	-8	-10	-15	mA	V_{DD} = 3.3 V V_{IN}=(V_{DD}-0.4) V
		-6	-8	-13	mA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
I_{SK}[*1] [*2]	Sink current for push-pull mode and low level	7.5	9	14.5	mA	V_{DD} = 3.3 V V_{IN}= 0.4 V
		6	7.5	13	mA	V_{DD} = 2.7 V V_{IN}= 0.4 V
C_{IO}[*1]	I/O pin capacitance	-	5	-	pF	

Note:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.3-8 I/O Output Characteristics

8.3.5.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	-	V	
R_{RST}[*1]	Internal nRESET pull up resistor	32	38	54	KΩ	VDD = 3.6 V
		45	60	79		VDD = 2.7 V
t_{FR}[*1]	nRESET input filtered pulse time	-	32	-	μS	Normal run and Idle mode 32us=3*512*HIRC
		31.36	-	32.64		Power down mode

Note:

1. Guaranteed by characterization result, not tested in production.

Table 8.3-9 nRESET Input Characteristics

8.4 AC Electrical Characteristics

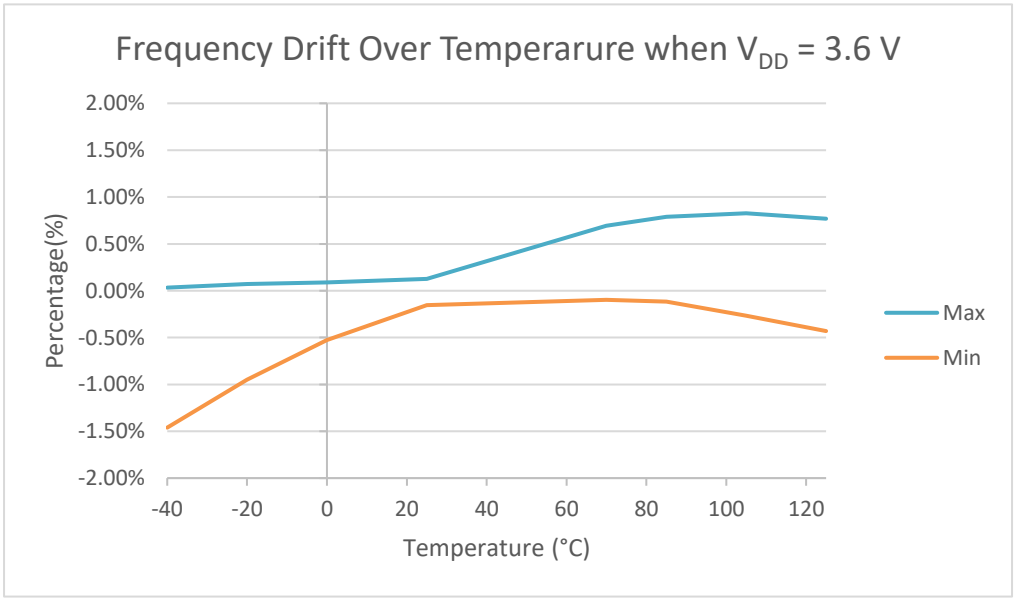
8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC)

The 48 MHz RC oscillator is calibrated in production.

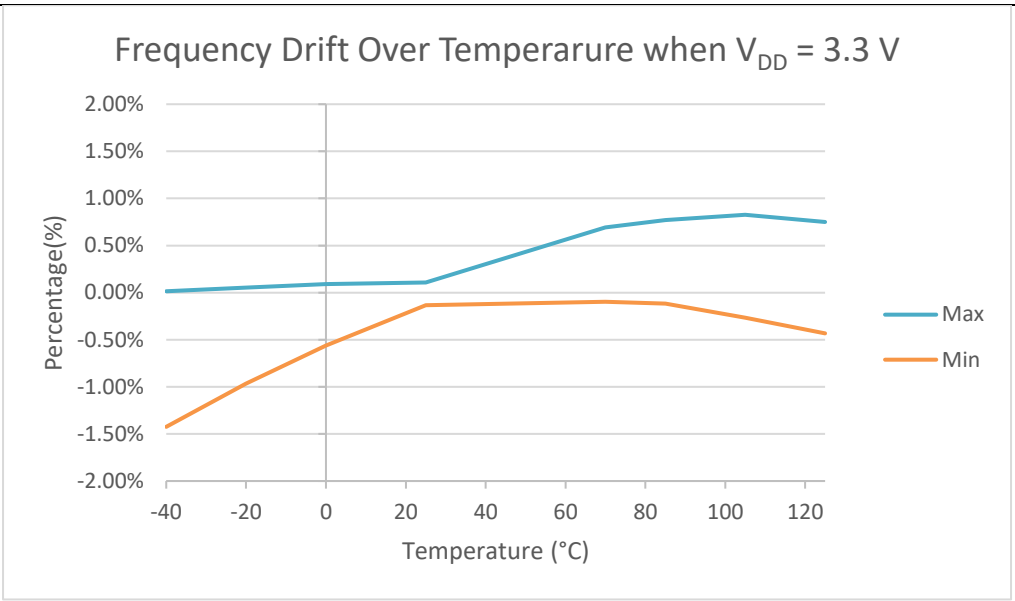
Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.7	3.3	3.6	V	
f_{HRC}[*1]	Oscillator frequnecy	-	48	-	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-0.5	-	+0.5	%	T_A = 25 °C, V_{DD} = 3.3V
		-0.7	-	+0.7	%	T_A = 0°C ~ +70 °C, V_{DD} = 3.3V
		-1	-	+1	%	T_A = -20°C ~ +105 °C, V_{DD} = 3.3V
		-2	-	+2	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.7 ~ 3.6V
I_{HRC}[*1]	Operating current	-	500	700	µA	
T_S[*2]	Stable time	-	-	20	µs	T_A = -40°C ~ +105 °C, V_{DD} = 2.7 ~ 3.6V

Note:
1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

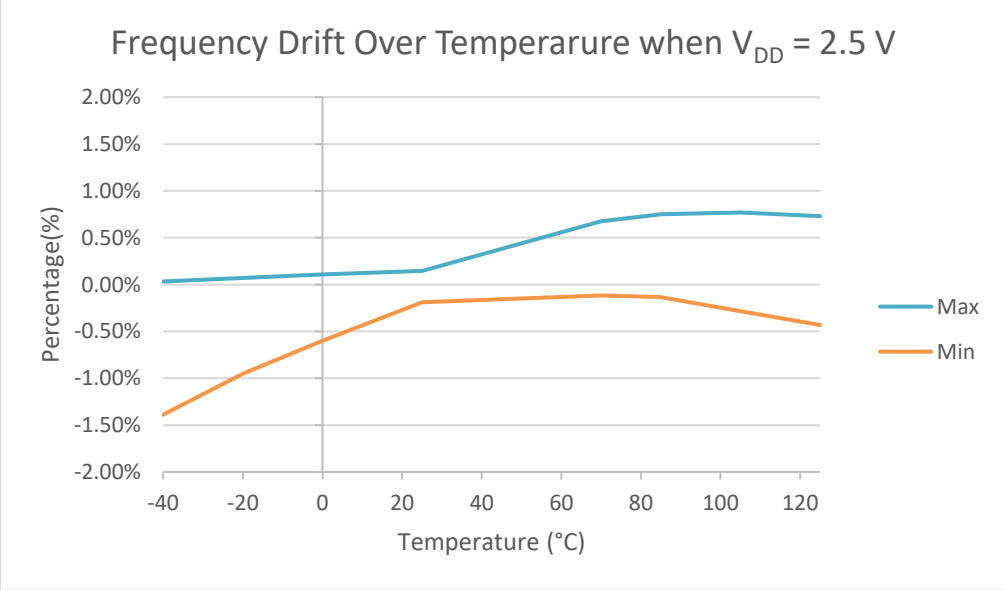
Table 8.4-1 48 MHz Internal High Speed RC Oscillator(HIRC) Characteristics



(a) Test Condition: V_{DD} = 3.6 V, Temp. = -40 ~ 125 °C



(b) Test Condition: V_{DD} = 3.3 V, Temp. = -40 ~ 125 °C



(c) Test Condition: V_{DD} = 2.5 V, Temp. = -40 ~ 125 °C

Note:

1. The graph is a statistical result using a limited number of samples. For the actual characetristic range, please refer to Table 8.4-1.

Figure 8.4-1 HIRC vs. Temperature

8.4.2 38.4 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operating voltage	2.7	3.3	3.6	V	
F_{LRC} [*2]	Oscillator frequnecy	-	38.4	-	kHz	
	Frequency drift over temperarure and volatge	-	1	-	%	T_A = 25 °C, V_{DD} = 3.3V
		-50	-	+50	%	T_A=-40~105 °C V_{DD}=2.7V~3.6V Without software calibration
I_{LRC}	Operating current	-	1	1.1	µA	V_{DD} = 3.3V
T_S	Stable time	-	100	-	µs	T_A=-40~105 °C V_{DD}=2.7V~3.6V

Note:

1. Guaranteed by characterization, not tested in production.
2. The 38.4 kHz low speed RC oscillator can be calibrated by user.

Table 8.4-2 38.4 kHz Internal Low Speed RC Oscillator(LIRC) characteristics

8.4.3 PLL Characteristics

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
f_{PLL_in}	PLL input clock	3.2	-	32	MHz	
f_{PLL_OUT}	PLL multiplier output clock	50	-	144	MHz	
f_{PLL_REF}	PLL reference clock	0.8	-	8	MHz	
f_{PLL_VCO}	PLL voltage controlled oscillator	200	-	500	MHz	
T_L	PLL locking time	-	-	500	µS	
Jitter[*2]	Cycle-to-cycle Jitter	-	200	350	pS	
I_{DD}	Power consumption	-	5	9	mA	V_{DD} =3.3V @ f_{PLL_OUT} = 144 MHz

Notes:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production

The f_{PLL_OUT} must meet the restrictions of CPU and peripheral.

Table 8.4-3 PLL characteristics

8.4.4 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Output high (90%) to low level (10%) fall time	-	6	ns	C_L = 30 pF, V_{DD} >= 2.7 V
		-	3.5		C_L = 10 pF, V_{DD} >= 2.7 V
$t_{r(IO)out}$	Output low (10%) to high level (90%) rise time	-	6	ns	C_L = 30 pF, V_{DD} >= 2.7 V

		-	3.5		C_L = 10 pF, V_{DD} >= 2.7 V
I_{DIO}[*4]	I/O dynamic current consumption	-	2.77	mA	C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		-	1.19		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz

Note:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$

Table 8.4-4 I/O AC Characteristics

8.5 Analog Characteristics

8.5.1 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	-	20	30	µA	AV_{DD} = 3.6V
I_{LVR}[*1]	LVR operating current	-	2	3.6		AV_{DD} = 3.6V
I_{BOD}[*1]	BOD operating current	-	3	5.5		AV_{DD} = 3.6V
V_{POR}	POR reset voltage	2	2.2	2.4	V	-
V_{LVR}	LVR reset voltage	2.16	2.3	2.44		-
V_{BOD}	BOD brown-out detect voltage	2.35	2.5	2.65		BODVL = 0
		2.54	2.7	2.86		BODVL = 1
T_{LVR_SU}[*1]	LVR startup time	-	140	240	µs	-
T_{LVR_RE}[*1]	LVR respond time	-	9	12		-
T_{BOD_SU}[*1]	BOD startup time	-	1000	1740		-
T_{BOD_RE}[*1]	BOD respond time	-	100	165		-
R_{VDDR}[*1]	V_{DD} rise time rate	10	-	-	µs/V	POR/LVR/BOD Enabled (BODVL=0)
R_{VDDF}[*1]	V_{DD} fall time rate	10	-	-		POR Enabled
		80	-	-		LVR Enabled
		470	-	-		BOD 2.5V Enabled
		305	-	-		BOD 2.7V Enabled

Note:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.5-1 Reset and Power Control Unit

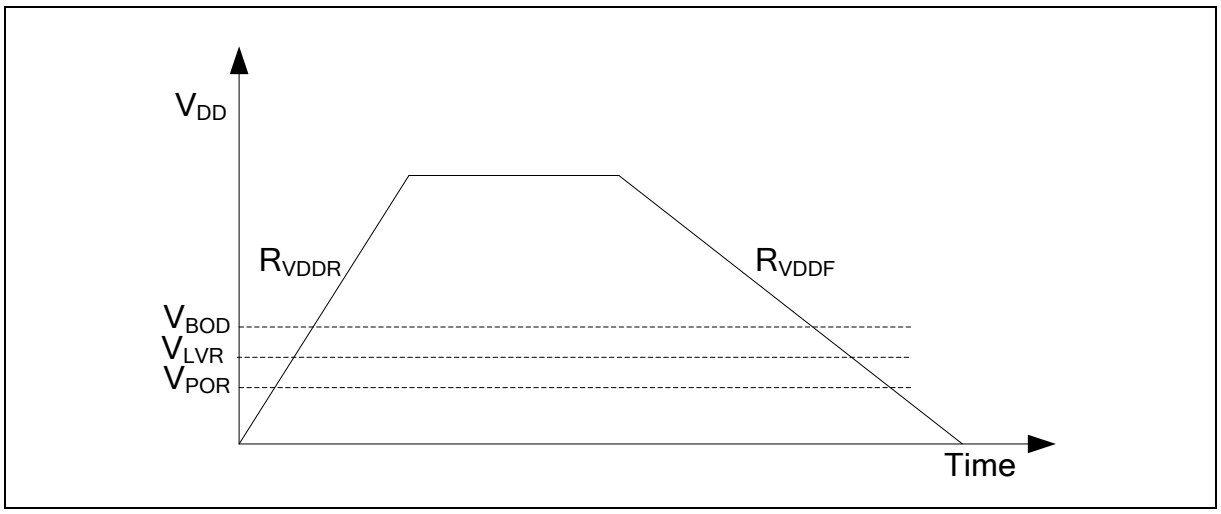


Figure 8.5-1 Power Ramp Up/Down Condition

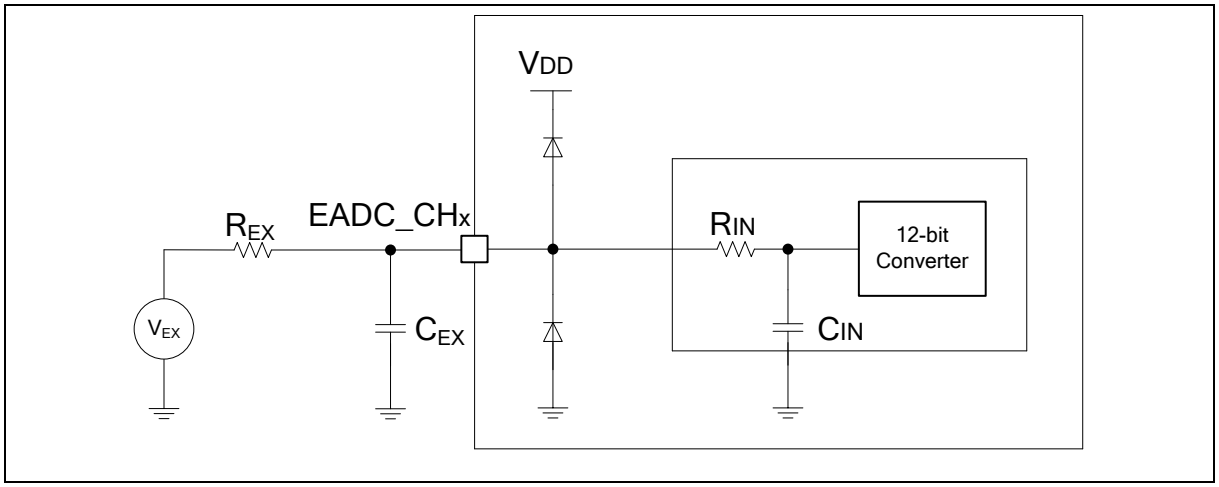
8.5.2 12-bit SAR ADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	125	°C	
AV_{DD}	Analog operating voltage	2.7	-	3.6	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	2.048	-	AV_{DD}	V	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
V_{CM}	Common-Mode Input Range	$V_{REF}/2$			V	Full differential input
I_{ADC}[*1]	Operating current (AV_{DD} + V_{REF} current)	46.8	165	176	µA	$AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V F_{ADC} = 24 MHz T_{CONV} = 17 * T_{ADC}
N_R	Resolution	12			Bit	
F_{ADC}[*1] $1/T_{ADC}$	ADC Clock frequency	4	-	24	MHz	
T_{SMP}	Sampling Time	1	-	256	$1/F_{ADC}$	T_{SMP} = (EXTSMPT(ADC_ESMPCTL[7:0]) + 1) * T_{ADC}
T_{CONV}	Conversion time	17	-	272	$1/F_{ADC}$	$T_{CONV} = T_{SMP}$ + 16 * T_{ADC}
F_{SPS}[*1]	Sampling Rate	-	-	1.4	MSPS	$F_{SPS} = F_{ADC} / T_{CONV}$ EXTSMPT(ADC_ESMPCTL[7:0]) = 0
INL[*1]	Integral Non-Linearity Error	-2	-	2	LSB	$V_{REF} = AV_{DD}$
DNL[*1]	Differential Non-Linearity Error	-1	-	2	LSB	$V_{REF} = AV_{DD}$
E_G[*1]	Gain error	-4	0.5	4	LSB	$V_{REF} = AV_{DD}$
E_O[*1]$_T$	Offset error	-4	0.5	4	LSB	$V_{REF} = AV_{DD}$
E_A[*1]	Absolute Error	-4	0.5	4	LSB	$V_{REF} = AV_{DD}$
ENOB[*1]	Effective number of bits	-	10.4	-	bits	F_{ADC} = 24 MHz $AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V Input Frequency = 10 kHz T_A = 25 °C
SNR[*1]	Signal-to-noise ratio	-	64.3	-		
THD[*1]	Total harmonic distortion	-	-70.7	-		
C_{IN}[*1]	Internal Capacitance	-	2.9	-	pF	
R_{IN}[*1]	Internal Switch Resistance	-	0.95	2	kΩ	
R_{EX}[*1]	External input impedance	-	-	50	kΩ	

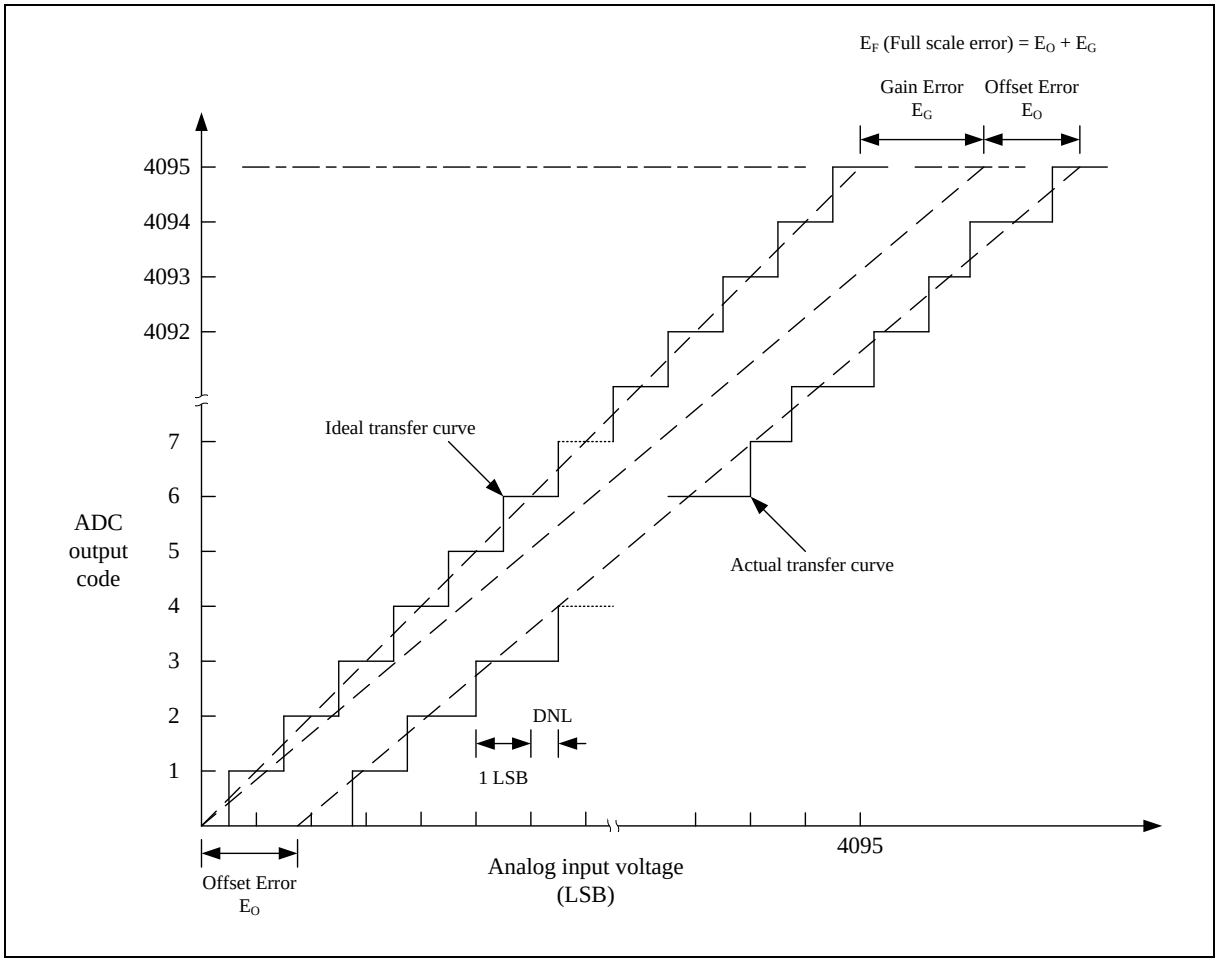
Note:

1. Guaranteed by characterization result, not tested in production.
2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} = \frac{k}{f_{ADC} \times C_{IN} \times \ln(2^{N+2})} - R_{IN}$$



Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5.3 Digital to Analog Converter (DAC)

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Analog supply voltage	2.7	3.3	3.6	V	
N_R	Resolution		12		bit	
V_{REF}	Reference supply voltage	2.048	-	AV_{DD}	V	$V_{REF} \le AV_{DD}$
DNL[*2]	Differential non-linearity error		±1	±3	LSB	12-bit mode
INL[*2]	Integral non-linearity error	-	±2	±5	LSB	12-bit mode
OE[*2]	Offset Error	-	-	±10	LSB	12-bit mode DACOUT buffer ON
		-	-	±5	LSB	12-bit mode DACOUT buffer OFF
GE[*2]	Gain Error	-	-	±10	LSB	12-bit mode DACOUT buffer ON
		-	-	±5	LSB	12-bit mode DACOUT buffer OFF
AE[*2]	Absolute Error	-	-	±10	LSB	12-bit mode DACOUT buffer ON
		-	-	±4	LSB	12-bit mode DACOUT buffer OFF
-	Monotonic		10-bit guaranteed		-	-
V_O[*1]	Output Voltage	0.2	-	AV_{DD} - 0.2	V	DACOUT buffer ON
		1*LSB	-	V_{REF}- 1*LSB	V	DACOUT buffer OFF
R_{LOAD}[*2] [*3]	Resistive load	5	-		kΩ	DACOUT buffer ON
R_O[*2]	Output impedance	-	8	20	kΩ	DACOUT buffer OFF
C_{LOAD}[*2] [*4]	Capacitive load	-	-	20	pF	DACOUT buffer OFF
		-	-	50	pF	DACOUT buffer ON
I_{DAC_AVDD}[*2]	DAC operating current on AV_{DD} supply	-	250	360	µA	AV_{DD} = 3.6V, no load, DACOUT buffer ON, lowest code (0x000)
						AV_{DD} = 3.6V, no load, DACOUT buffer ON, middle code (0x800)
I_{DAC_VREF}[*2]	DAC operating current on V_{REF} supply	-	-	200	µA	V_{REF} =2.5V, no load, worst case code (0x800)
T_B[*2]	Settling Time	-	5	6	µS	Full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value +/-1 LSB, $C_{LOAD} \le$ 50pF, RLOAD ≥ 5kΩ, Buffer ON, VREF = 2.5V

F_S	Update Rate	-	1	-	M_{SPS}	Max. frequency for a correct DAC_OUT change from core i to i+1LSB, $C_{LOAD} \leq 50pF$, $R_{LOAD} \geq 5k\Omega$
PSRR[*1]	Power Supply Rejection Ratio	-	-60	-40	dB	No R_{LOAD}, C_{LOAD} = 50pF

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production.
3. Resistive load between DACOUT and AV_{SS}.
4. Capacitive load at DACOUT pin.

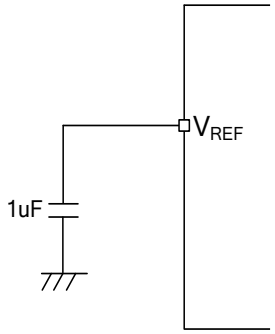
8.5.4 Internal Voltage Reference for M030G

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{REF_INT}	Internal reference voltage	2.017	2.048	2.079	V	AV_{DD} >= 2.7 V
		2.463	2.5	2.538		AV_{DD} >= 2.7 V
T_s[*1]	Stable time	-	-	2	mS	C_L =4.7 uF, V_{REF} initial=0, Preload is enabled.
		-	-	15	mS	C_L =4.7 uF, V_{REF} initial=3.6, Preload is enabled.
		-	-	480	µS	C_L =1 uF, V_{REF} initial=0, Preload is enabled.
		-	-	3000	µS	C_L =1 uF, V_{REF} initial=3.6, Preload is enabled.
I_{REF_INT}[*1]	V_{REF_INT} operating current	-	160	220	µA	
I_{REF_LOAD}	V_{REF_INT} output loading current	-	-	1.5	mA	

Note:

1. Guaranteed by characterization, not tested in production



Note: V_{REF_INT} is only supported while package includes V_{REF} pin with external capacitor.

Figure 8.5-2 Typical connection with internal voltage reference

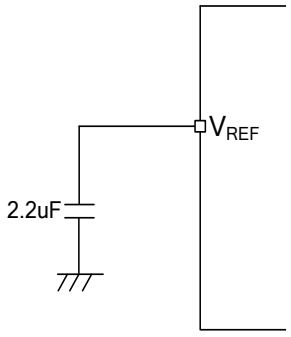
8.5.5 Internal Voltage Reference for M031G

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{REF_INT}	Internal reference voltage	2.017	2.048	2.079	V	AV_{DD} >= 2.7 V
		2.463	2.5	2.538		AV_{DD} >= 2.7 V
T_s[*1]	Stable time	-	-	2	mS	C_L =4.7 uF, V_{REF} initial=0, Preload is enabled.
		-	-	15	mS	C_L =4.7 uF, V_{REF} initial=3.6, Preload is enabled.
		-	-	900	µS	C_L =2.2 uF, V_{REF} initial=0, Preload is enabled.
		-	-	6000	µS	C_L =2.2 uF, V_{REF} initial=3.6, Preload is enabled.
I_{REF_INT}[*1]	V_{REF_INT} operating current	-	300	360	µA	
I_{REF_LOAD}	V_{REF_INT} output loading current	-	-	3	mA	

Note:

1. Guaranteed by characterization, not tested in production



Note: V_{REF_INT} is only supported while package includes V_{REF} pin with external capacitor.

Figure 8.5-3 Typical connection with internal voltage reference

8.5.6 Temperature Sensor

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
AV_{DD}	Analog supply voltage	2.7	3.3	3.6	V	
T_A	Temperature	-40	-	105	°C	
I_{TEMP}	Temperature Sensor operating current	-	200	-	µA	
T_{TEMP_ERR}[*1]	Internal Temperature Deviation	-1.6	-	+1.6	°C	T = 0 °C to 70 °C V_{DD} = 3.3 V

		-2	-	+2	°C	T = -40 °C to 105 °C V_{DD} = 2.7 V to 3.6 V
T_R	Temperature Resolution	-	0.0625	-	°C	
T_{CONV}	Conversion Time	-	84	100	ms	

Note:

1. Guaranteed by characterization, not tested in production

8.6 Communications Characteristics

8.6.1 SPI Dynamic Characteristics

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	24	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{DS}	Data input setup time	2	-	-	ns	
t_{DH}	Data input hold time	4	-	-	ns	
t_V	Data output valid time	-	-	5	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF

Note:
1. Guaranteed by design.

Table 8.6-1 SPI Master Mode Characteristics

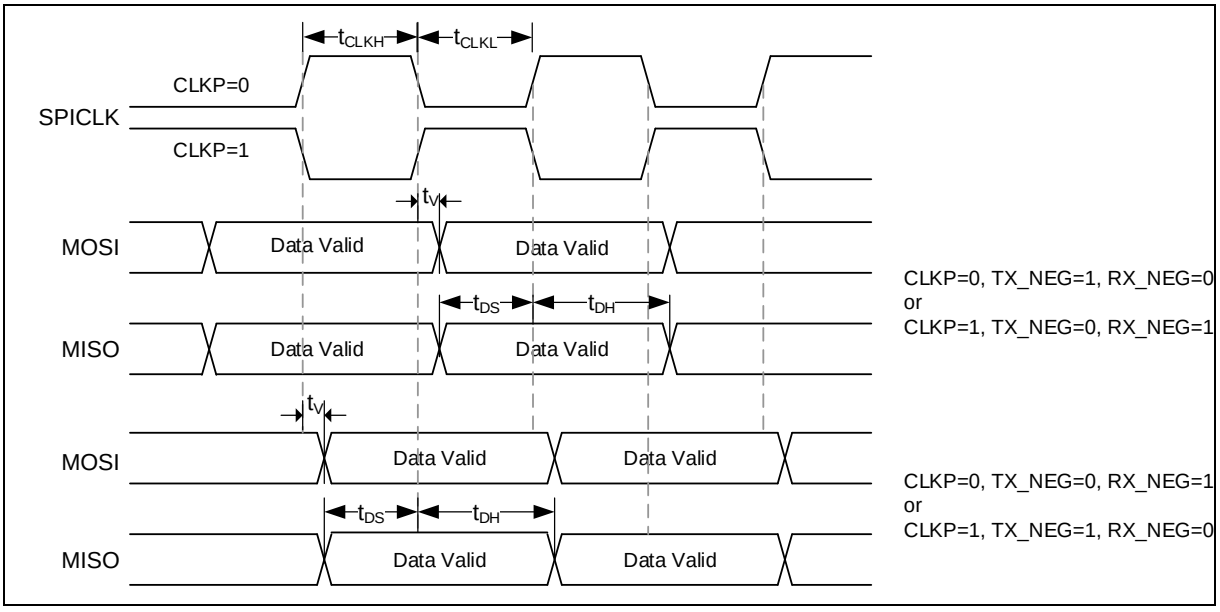


Figure 8.6-1 SPI Master Mode Timing Diagram

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	16	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2				
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2				
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns	
t_{DS}	Data input setup time	1.5	-	-	ns	
t_{DH}	Data input hold time	3.5	-	-	ns	
t_V	Data output valid time	-	-	17.5	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-2 SPI Slave Mode Characteristics

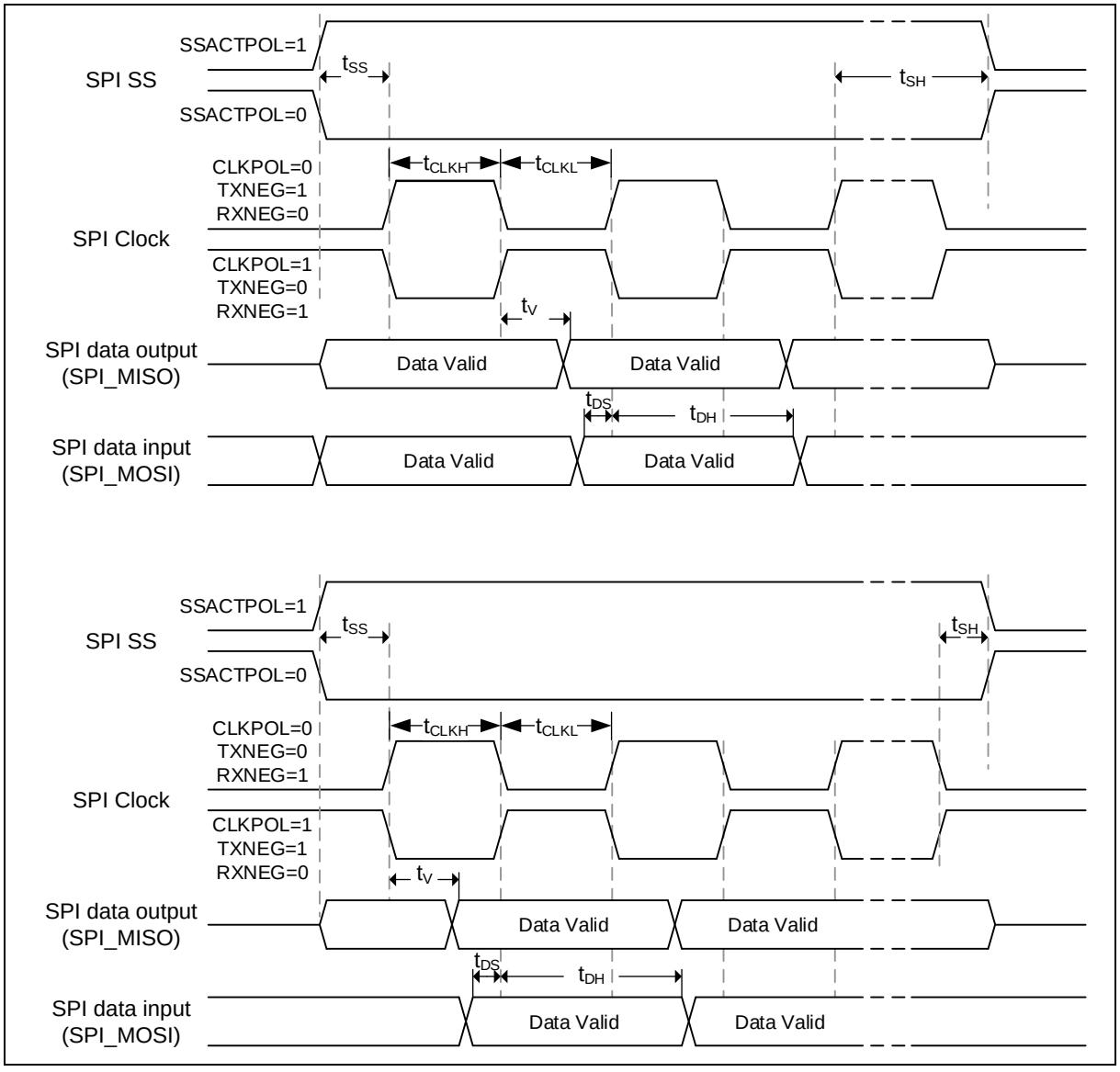


Figure 8.6-2 SPI Slave Mode Timing Diagram

8.6.2 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	µs
t_{HIGH}	SCL high period	4	-	0.6	-	µs
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	µs
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	µs
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	µs
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	µs
$t_{SU;DAT}$	Data setup time	250	-	100	-	ns
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	µs
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	ns
t_f	SCL/SDA fall time	-	300	-	300	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-3 I²C Characteristics

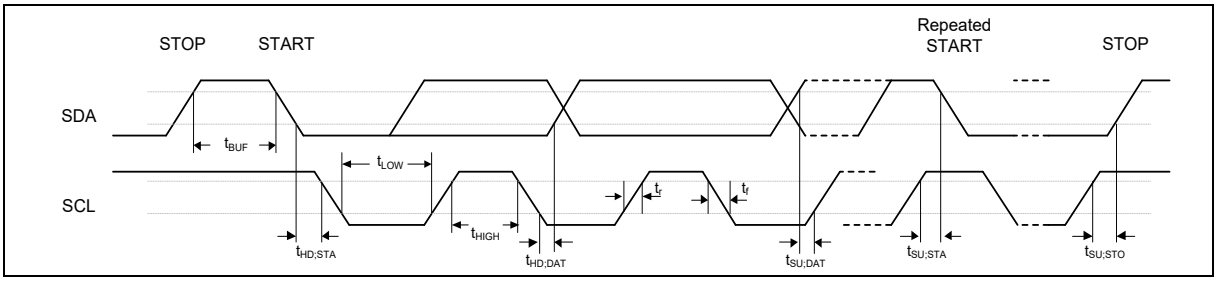


Figure 8.6-3 I²C Timing Diagram

8.7 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	1.62	1.8	1.98	V	T_A = 25°C
T_{ERASE}	Page erase time	-	20	-	ms	
T_{PROG}	Program time	-	60	-	µs	
I_{DD1}	Read current	-	7	-	mA	
I_{DD2}	Program current	-	8	-	mA	
I_{DD3}	Erase current	-	12	-	mA	
N_{ENDUR}	Endurance	20,000	-		cycles[2]	T_J = -40°C~125°C
T_{RET}	Data retention	10	-	-	year	20 kcycle[3] T_J = 85°C
		2	-	-	year	20 kcycle[3] T_J = 105°C

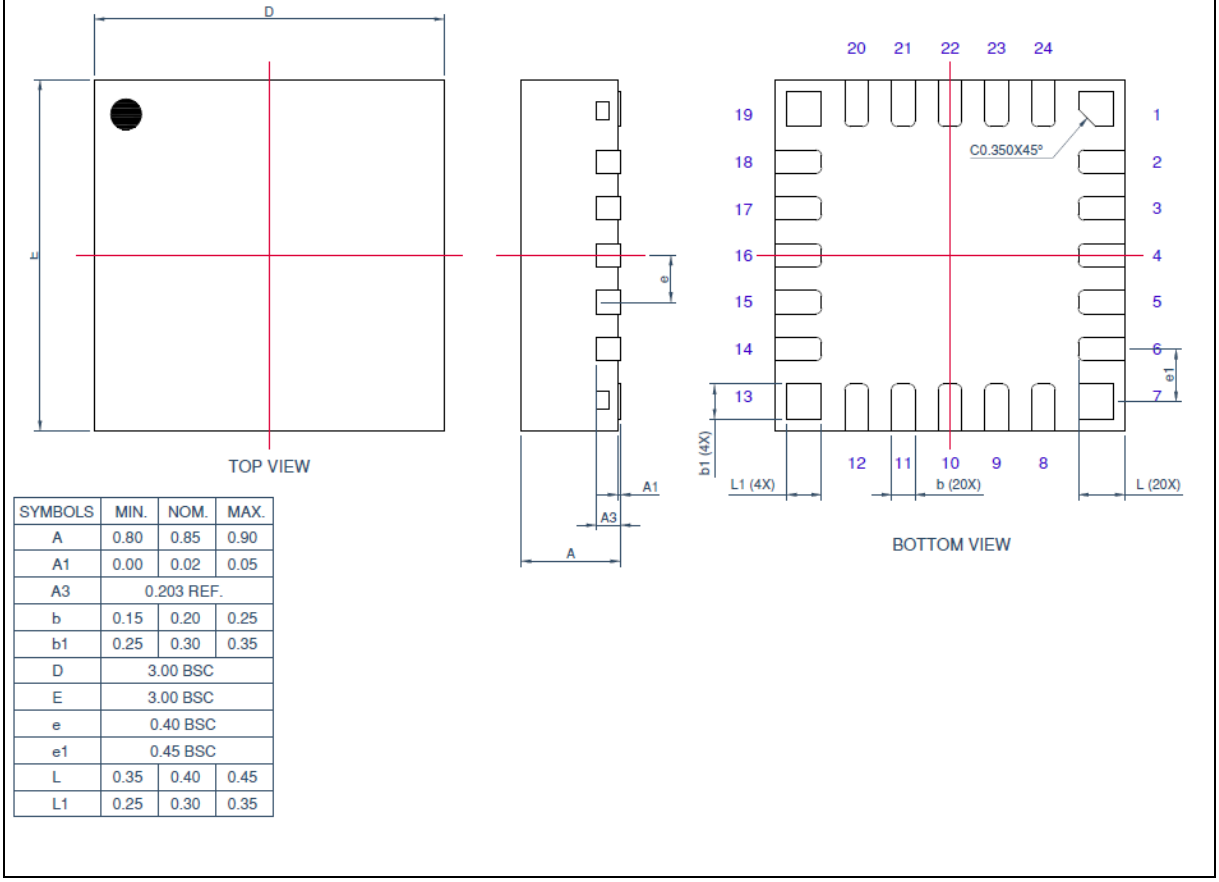
Note:

1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles.
3. Guaranteed by design.

Table 8.7-1 Flash DC Electrical Characteristics

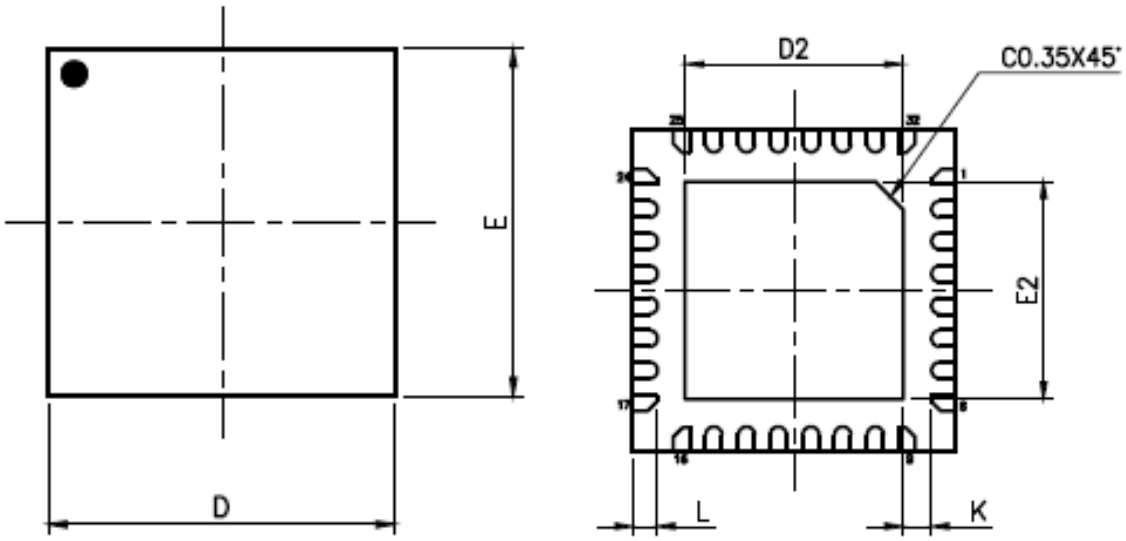
9 PACKAGE DIMENSIONS

9.1 QFN 24L (3x3x0.9 mm Pitch:0.40 mm)

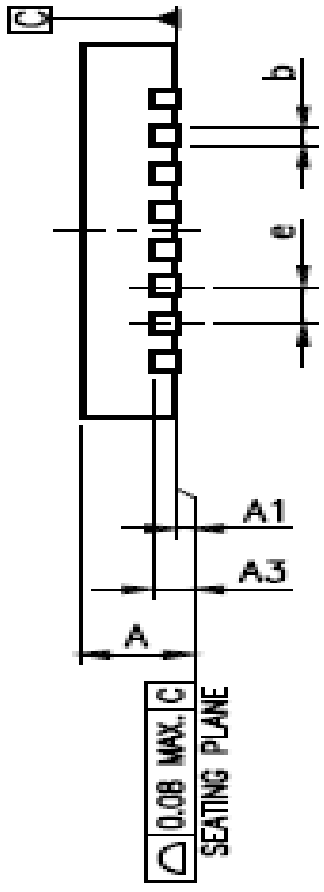


SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
b1	0.25	0.30	0.35
D		3.00 BSC	
E		3.00 BSC	
e		0.40 BSC	
e1		0.45 BSC	
L	0.35	0.40	0.45
L1	0.25	0.30	0.35

9.2 QFN 33L (4x4x0.8 mm Pitch:0.40 mm)



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
L	0.25	0.30	0.35
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
K	0.20	—	—



10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EADC	Enhanced Analog-to-Digital Converter
EBI	External Bus Interface
EMAC	Ethernet MAC Controller
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12 MHz Internal High Speed RC Oscillator
HXT	4~32 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation

QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TK	Touch Key
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Description
2021.5.31	1.00	Initial version.

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