

## 8-bit Microcontroller

# KM101LR05D/04D/03D

## Data Sheet

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# 1.1 Product Summary

This LSI user's manual describes KM101LR05D/04D/03D.

The detail of product specification is described mainly about KM101LR05D.

For the difference between each product, See [1.3 Comparison of Product Specification] and [1.4.1 Pin Configuration].

$V_{DD18}$  voltage after reset release, oscillation stabilization wait time after reset release and ROM capacity vary depending on the ROM name of each product. Table: 1.1.1 shows the difference of specifications between the ROM name.

Table:1.1.1 Product Summary

Product Name	ROM name *	$V_{DD18}$ voltage after reset release	Oscillation stabilization wait time after reset release	ROM (ReRAM) capacity (Program area/Data area)
KM101LR05D KM101LR04D KM101LR03D	XW	1.1 V	$2^{11}/(f_{SRC}/2)$	62 KB / 2 KB
	XX			59 KB / 4 KB
	XY			53 KB / 8 KB
	XZ			41 KB / 16 KB
	XA	1.8 V	$2^8/(f_{SRC}/2)$	62 KB / 2 KB
	XB			59 KB / 4 KB
	XC			53 KB / 8 KB
	XD			41 KB / 16 KB

\* ROM name: XA/XB/XC/XD/XW/XX/XY/XZ indicates the product that ReRAM is blank.



When using the debugger or programmer, set "Product name + ROM name" (e.g.: KM101LR05DXA/XW) in the field "Product type" or "Microcomputer product type".

When "ROM name" is set incorrectly, connect error is occurred.

When nothing is set to "ROM name", XA/XW is selected.

(e.g.: KM101LR05D → KM101LR05DXA/XW)

## 1.2 Hardware Features

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### ■ Features

In this document, the divided clock and the frequency of it are described as follows:

Divided clock: Clock name/n (n: division ratio)

Frequency:  $f_{\text{Clock name}}$

- CPU Core
  - AM13L core
  - LOAD-STORE architecture (3- or 4-stage Pipeline)
- Machine Cycle and Operating Voltage
  - High-Speed mode
    - 100 ns / 10 MHz (Max)( $V_{\text{DD30}}$ : 1.8 V to 3.6 V)
    - 1.0  $\mu\text{s}$  / 1 MHz (Max)( $V_{\text{DD30}}$ : 1.3 V to 3.6 V)
  - Low-Speed Mode
    - 25  $\mu\text{s}$  / 40 kHz (Max)( $V_{\text{DD30}}$ : 1.1 V to 3.6 V)
- Operating Mode
  - NORMAL mode (High-Speed mode)
  - SLOW mode (Low-Speed mode)
  - HALT mode (High-Speed/Low-Speed mode)
  - STOP mode
- Embedded Memory
  - ROM (ReRAM): 64 KB (Programmable area and Data area vary depending on the ROM name.  
For details, see Table:1.1.1.)
  - RAM: 4 KB
- ReRAM Specification
  - Program voltage ( $V_{\text{DD30}}$ ): 1.8 V to 3.6 V
  - Program cycles: 1000 times (Program area), 100000 times (Data area)
  - Data is rewritable in bytes without data erase.
- Clock Oscillator (4 circuits)
  - External Low-Speed Oscillation (SOSCCLK): 32.768 kHz (crystal or ceramic)
  - External High-Speed Oscillation (HOSCCLK): up to 10 MHz (crystal or ceramic)
  - Internal Low-Speed Oscillation (SRCCLK): 40 kHz  $\pm$  20 % ( $V_{\text{DD30}}$ : 1.1 V to 3.6 V)
  - Internal High-Speed Oscillation (HRCCLK): 10/8 MHz  $\pm$  3 % ( $V_{\text{DD30}}$ : 1.8 V to 3.6 V)  
1 MHz  $\pm$  10 % ( $V_{\text{DD30}}$ : 1.3 V to 3.6 V)
- Internal Operating Clock
  - System Clock (SYSCLK): 10 MHz (Max)  
SYSCLK is generated by dividing HCLK or SCLK, and the division ratio is 1, 2, 4, 8, 16 or 32.  
HCLK: HOSCCLK or HRCCLK  
SCLK: SOSCCLK or SRCCLK

- Interrupt Circuit  
KM101LR05D/04D/03D: 31 internal interrupts (except for NMI)  
8 external interrupts (IRQ interrupt: 7, KEY interrupt: 1)
  
- DMA (1 channel)
  - Data transfer size: 8 bits/16 bits
  - Maximum transfer counts: 1023
  - Activation trigger: external interrupts / internal interrupts / software (setting the DMA start bit)
  
- Watchdog Timer (WDT)
  - Function: 1st watchdog time-out generates NMI, and 2nd consecutive time-out generates a LSI reset.
  - Clock Source: WDTCLK (SOSCCLK or SRCCLK)
  
- Timer Counter: 13 units
  - General-purpose 8-bit timer (Timer 0/1/2/3/4/5): 6 units
  - General-purpose 16-bit timer (Timer 7/8/9): 3 units
  - 8-bit free-run (Timer 6) /Time-base timer: 1 unit each
  - RTC time base timer (RTC-TBT): 1 unit
  - Real Time Clock (RTC): 1 unit
  
- <Timer 0>
  - Function: Square wave output, additional pulse PWM output, event count, simple pulse width measurement
  - Clock Source: HCLK, HCLK/4, HCLK/16, HCLK/32, HCLK/64, SCLK, SYSCLK/2, SYSCLK/4, or TM0IO input
  
- <Timer 1 >
  - Function: Square wave output, event count, 16-bit cascade connection (connected with Timer 0)
  - Clock Source: HCLK, HCLK/4, HCLK/16, HCLK/64, HCLK/128, SCLK, SYSCLK/2, SYSCLK/8, or TM1IO input
  
- <Timer 2>
  - Function: Square wave output, additional pulse PWM output, event count, simple pulse width measurement
  - Clock Source: HCLK, HCLK/4, HCLK/16, HCLK/32, HCLK/64, SCLK, SYSCLK/2, SYSCLK/4, or TM2IO input
  
- <Timer 3 >
  - Function: Square wave output, event count, 16-bit cascade connection (connected with Timer 2)
  - Clock Source: HCLK, HCLK/4, HCLK/16, HCLK/64, HCLK/128, SCLK, SYSCLK/2, SYSCLK/8, or TM3IO input
  
- <Timer 4>
  - Function: Square wave output, additional pulse PWM output, event count, simple pulse width measurement
  - Clock Source: HCLK, HCLK/4, HCLK/16, HCLK/32, HCLK/64, SCLK, SYSCLK/2, SYSCLK/4, or TM4IO input
  
- <Timer 5 >
  - Function: Square wave output, event count, 16-bit cascade connection (connected with Timer 4)
  - Clock Source: HCLK, HCLK/4, HCLK/16, HCLK/64, HCLK/128, SCLK, SYSCLK/2, SYSCLK/8, or TM5IO input

## &lt;Timer 6&gt;

- Function: One-minute timer can be generated in combination with a time base timer.
- Clock Source: HCLK, HCLK/2<sup>7</sup>, HCLK/2<sup>13</sup>, SYSCLK, SCLK, SCLK/2<sup>7</sup> or SCLK/2<sup>13</sup>

## &lt;Time Base Timer&gt;

- Function: An interrupt can be generated at a given set time.
- Clock Source: HCLK or SCLK
- Interrupt generation cycle: 2<sup>N</sup>/f<sub>HCLK</sub>, 2<sup>N</sup>/f<sub>SCLK</sub> (N = 7, 8, 9, 10, 12, 13, 14, 15)

## &lt;Timer 7&gt;

- Function: Square wave output, PWM output (duty/cycle are programmable), one-shot pulse output, IGBT output, event count, and input capture
- Clock Source: Generated clock by dividing HCLK, SYSCLK, SCLK, or TM7IO input by 1, 2, 4 or 16.

## &lt;Timer 8 &gt;

- Function: Square wave output, PWM output (duty/cycle are programmable), event count, and input capture
- Clock Source: Generated clock by dividing HCLK, SYSCLK, SCLK, or TM8IO input by 1, 2, 4 or 16.

## &lt;Timer 9 &gt;

- Function: Square wave output, PWM output (duty/cycle are programmable), event count, and input capture
- Clock Source: Generated clock by dividing HCLK, SYSCLK, SCLK, or TM9IO input by 1, 2, 4 or 16.
- \* KM101LR03D cannot be used square wave output, PWM output, event count and TM9IO.

## &lt;RTC time base timer (RTC-TBT)&gt;

- Function: Clock generation for the Real Time Clock (RTC)  
Frequency correction  
(Correction Range: ±488 ppm to ±31220 ppm, Accuracy: approx. 0.48 ppm to 30.52 ppm)
- Clock Source: SOSCLK or SRCCLK

## &lt;Real Time Clock (RTC)&gt;

- Function: Calendar calculation, adjustment of leap year  
Periodic interrupt (0.5 s, 1 s, 1 min or 1 hour)  
Alarm0 interrupt (date/hour/minute), Alarm1 interrupt (month/day/hour/minute)
- Buzzer Output/Inverted Buzzer Output
- Output frequency: f<sub>HCLK</sub>/2<sup>M</sup> (M = 9, 10, 11, 12, 13, 14), f<sub>SCLK</sub>/2<sup>N</sup> (N = 3, 4)

## - Serial Interface: 4 units

## &lt;Serial Interface 0, 1&gt; (Full duplex UART/Clock synchronous serial)

- Function:
  - Full duplex UART:
    - Parity check, Detection of overrun error/framing error, Selectable transfer bits of 7 or 8
  - Clock synchronous serial (SPI compatible):
    - 2,3 or 4-wire communication, MSB/LSB first selectable, multiple bytes transmission is available.
- Clock Source: external clock, dedicated baud rate timer

## &lt;Serial Interface 2, 3&gt; (Multi-master IIC/Clock synchronous serial)

- Function:
  - Multi-master IIC
  - Clock synchronous serial (SPI compatible):
    - 2,3 or 4-wire communication, MSB/LSB first selectable, multiple bytes transmission is available.
- Clock Source: external clock, dedicated baud rate timer

## \* KM101LR03D

Serial Interface 3: Clock synchronous serial can be used in 2-wire communication only,

and is not compatible with SPI. (Chip select pin is not assigned.)

- A/D Converter (ADC): 1 unit
  - Resolution: 12 bits
  - Analog signal input channel
    - KM101LR05D: 8 channels
    - KM101LR04D: 6 channels
    - KM101LR03D: 4 channels
  
- I/O ports
  - KM101LR05D: 69 pins (selectable N-channel transistor drive strength: 55 pins)
  - KM101LR04D: 53 pins (selectable N-channel transistor drive strength: 41 pins)
  - KM101LR03D: 37 pins (selectable N-channel transistor drive strength: 27 pins)
  
- Clock Output
  - HCLK, SCLK, SYSCLK or RTCCLK can be output.
- Automatic Reset Circuit
- Low-voltage Detection Circuit (LVI)
- LCD Driver
  - <KM101LR05D>
    - 43 segment outputs, 4 common outputs (39 segment outputs, 8 common outputs)
    - Display mode: Static, 1/2 to 1/8 duty
    - Bias: 1/2, 1/3 (Built-in boost/ External resistor divider)
  - <KM101LR04D>
    - 31 segment outputs, 4 common outputs
    - Display mode: Static, 1/2 to 1/4 duty
  - <KM101LR03D>
    - 21 segment outputs, 4 common outputs
    - Display mode: Static, 1/2 to 1/4 duty

## KM101LR05D/04D/03D

- Package

KM101LR05D: TQFP080-P-1212(12 mm square, 0.5 mm pitch)

KM101LR04D: TQFP064-P-1010(10 mm square, 0.5 mm pitch)

KM101LR03D: TQFP048-P-0707( 7 mm square, 0.5 mm pitch)

- Operating Ambient Temperature: Ta = -40 °C to 85 °C

## 1.3 Comparison of Product Specification

Table:1.3.1 Functions

Function	Specification	KM101LR05D	KM101LR04D	KM101LR03D
Port	I/O port	69 pins	53 pins	37 pins
	N-channel transistor drive strength	55 pins	41 pins	27 pins
Interrupt	Internal interrupt	31	31	31
	External interrupt	8 (7: IRQ0-6, 1: KEY0-7)	8 (7: IRQ0-6, 1: KEY1-7)	8 (7: IRQ0-6, 1: KEY1-5)
Timer 5	Timer I/O	TM5IO	TM5IO	TM5IO
Timer 9	Timer I/O	TM9IO	TM9IO	-( *1)
Serial interface 1		√	√	√
Serial interface 3	Serial communication pins	SBO3/SDA3 SBT3/SCL3 SBI3 SBCS3	SBO3/SDA3 SBT3/SCL3 SBI3 SBCS3	SBO3/SDA3 SBT3/SCL3 - -
	Clock synchronous	2, 3 or 4-wire	2, 3 or 4-wire	2-wire
	SPI compatible	√	√	-( *2)
Buzzer	Buzzer output /Inverted buzzer output	BUZ NBUZ	BUZ NBUZ	BUZ NBUZ
ADC	Analog input	8 pins (AN0-7)	6 pins (AN2-7)	4 pins (AN2-5)
LCD driver	Segment output	43 pins (SEG0-42) /39 pins (SEG4-42)	31 pins (SEG0-30)	21 pins (SEG0-20)
	Common output	4 pins (COM0-3) /8 pins (COM0-7)	4 pins (COM0-3)	4 pins (COM0-3)
Oscillation		HOSCCLK SOSCCLK HRCCLK SRCCLK	HOSCCLK SOSCCLK HRCCLK SRCCLK	HOSCCLK SOSCCLK HRCCLK SRCCLK
Package		80-pin TQFP	64-pin TQFP	48-pin TQFP

\*1 Timer function is available.

\*2 Chip select pin is not assigned.



Table:1.3.2 Functions of I/O Port

I/O Port	KM101LR05D								KM101LR04D								KM101LR03D							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Port0	√	√	√	√	√	√	√	√	√	√	√	√	√	√	-	-	-	-	√	√	-	-	-	-
Port1	√	√	√	√	√	√	√	√	√	√	√	√	√	√	-	-	-	-	√	√	√	√	-	-
Port2	√	√	√	√	√	√	√	√	√	√	-	-	-	-	√	√	√	√	-	-	-	-	-	-
Port3	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
Port4	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	-	-	-	√	√	√	√	√
Port5	√	√	√	√	√	√	√	√	√	√	√	-	-	-	-	√	√	√	√	-	-	-	-	-
Port6	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	-	-	-	-	√	√	√	√
Port7	√	√	√	√	√	√	√	√	-	-	-	-	√	√	√	√	-	-	-	-	√	√	√	√
Port8	-	-	√	√	√	√	√	√	-	-	√	√	√	√	√	√	-	-	√	√	√	√	√	√

√ : implemented I/O port

√ : implemented I/O port (selectable N-channel transistor drive strength)

- : not implemented

Table:1.3.3 Functions of LCD Control

I/O Port	KM101LR05D								KM101LR04D								KM101LR03D							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Port2	-	SEG 36	SEG 37	SEG 38	SEG 39	SEG 40	SEG 41	SEG 42	-	SEG 28	-	-	-	-	SEG 29	SEG 30	-	SEG 20	-	-	-	-	-	-
Port3	SEG 28	SEG 29	SEG 30	SEG 31	SEG 32	SEG 33	SEG 34	SEG 35	SEG 20	SEG 21	SEG 22	SEG 23	SEG 24	SEG 25	SEG 26	SEG 27	SEG 12	SEG 13	SEG 14	SEG 15	SEG 16	SEG 17	SEG 18	SEG 19
Port4	SEG 20	SEG 21	SEG 22	SEG 23	SEG 24	SEG 25	SEG 26	SEG 27	SEG 12	SEG 13	SEG 14	SEG 15	SEG 16	SEG 17	SEG 18	SEG 19	-	-	-	SEG 7	SEG 8	SEG 9	SEG 10	SEG 11
Port5	SEG 12	SEG 13	SEG 14	SEG 15	SEG 16	SEG 17	SEG 18	SEG 19	SEG 8	SEG 9	SEG 10	-	-	-	-	SEG 11	SEG 4	SEG 5	SEG 6	-	-	-	-	-
Port6	SEG 4	SEG 5	SEG 6	SEG 7	SEG 8	SEG 9	SEG 10	SEG 11	SEG 0	SEG 1	SEG 2	SEG 3	SEG 4	SEG 5	SEG 6	SEG 7	-	-	-	-	SEG 0	SEG 1	SEG 2	SEG 3
Port7	COM 0	COM 1	COM 2	COM 3	COM 4/ SEG 0	COM 5/ SEG 1	COM 6/ SEG 2	COM 7/ SEG 3	-	-	-	-	COM 0	COM 1	COM 2	COM 3	-	-	-	-	COM 0	COM 1	COM 2	COM 3
Port8	-	-	VLC 2	VLC 3	C2	C1	-	-	-	-	VLC 2	VLC 3	C2	C1	-	-	-	-	VLC 2	VLC 3	C2	C1	-	-
-	VLC1								VLC1								VLC1							

-: not implemented



Set "0" to the registers and bits corresponding to the functions which are not implemented.

Table:1.3.4 Pin Functions

Pin No.			Power supply /Oscillations /Reset /Mode control	Port	External interrupt /KEY interrupt	Timer	Serial interface	Buzzer /Clock output	A/D
KM101 LR05D	KM101 LR04D	KM101 LR03D							
1	1	1	VSS						
2	2	2	XI						
3	3	3	XO						
4	4	4	NATRON						
5	5	5	NRST	P27					
6	6	6	OSC1	P80	IRQ2A				
7	7	7	OSC2	P81	IRQ3A				
8				P00		TM9IOC			
9				P01		TM4IOB			
10	8			P02		TM2IOB/TM8IOC		BUZB	
11	9			P03		TM0IOB/TM7IOC		NBUZB	
12	10	8		P04		TM7IOA	SBO3A/SDA3A		
13	11	9		P05		TM0IOA/TM2IOA	SBT3A/SCL3A	CLKOUTA	
14	12			P06		TM8IOB	SBI3A		
15	13			P07		TM9IOA	SBCS3A		
16				P10	IRQ0A/KEY0A				AN0
17				P11	IRQ1A/KEY1A				AN1
18	14	10		P12	IRQ4C/KEY2A				AN2
19	15	11		P13	IRQ5C/KEY3A				AN3
20	16	12	VREFF						
21	17	13	DMOD						
22	18	14	OCD_CLK	P14	IRQ4A/KEY4A				AN4
23	19	15	OCD_DATA	P15	IRQ5A/KEY5A				AN5
24	20			P16	IRQ6A/KEY6A				AN6
25	21			P17	KEY7A				AN7
26	22			P20		TM1IOB/TM9IOB			
27	23			P21		TM5IOA			
28				P22			SBI2B		
29				P23			SBO2B/SDA2B		
30				P24			SBT2B/SCL2B		
31				P25			SBCS2B		
32	24	16		P26			SBI1A/RXD1A		
33	25	17		P30			SBO1A/TXD1A		
34	26	18		P31			SBT1A		
35	27	19		P32			SBCS1A		
36	28	20		P33				BUZA	
37	29	21		P34		TM4IOA/TM7IOB		NBUZA	
38	30	22		P35			SBI0B/RXD0B		
39	31	23		P36			SBO0B/TXD0B		
40	32	24		P37			SBT0B		
41	33	25		P40			SBCS0B		
42	34	26		P41			SBI2A		
43	35	27		P42			SBO2A/SDA2A		
44	36	28		P43			SBT2A/SCL2A		

# KM101LR05D/04D/03D

Pin No.			Power supply /Oscillations /Reset /Mode control	Port	External interrupt /KEY interrupt	Timer	Serial interface	Buzzer /Clock output	A/D
KM101 LR05D	KM101 LR04D	KM101 LR03D							
45	37	29		P44			SBCS2A		
46	38			P45			SBI1B/RXD1B		
47	39			P46			SBO1B/TXD1B		
48	40			P47			SBT1B		
49	41			P50			SBCS1B		
50				P51			SBI3B		
51				P52			SBO3B/SDA3B		
52				P53			SBT3B/SCL3B		
53				P54	KEY0B		SBCS3B		
54	42	30		P55	KEY1B	TM1IOA			
55	43	31		P56	KEY2B	TM3IOA			
56	44	32		P57	KEY3B	TM8IOA		CLKOUTB	
57	45	33		P60	IRQ0B				
58	46	34		P61	IRQ1B				
59	47	35		P62	IRQ2B				
60	48	36		P63	IRQ3B				
61	49			P64	KEY4B		SBI0A/RXD0A		
62	50			P65	KEY5B		SBO0A/TXD0A		
63	51			P66	KEY6B		SBT0A		
64	52			P67	KEY7B		SBCS0A		
65	53	37		P70	IRQ6B				
66	54	38		P71	IRQ5B				
67	55	39		P72	IRQ4B	TM3IOB			
68	56	40		P73		TM5IOB			
69				P74					
70				P75					
71				P76					
72				P77					
73	57	41	C1	P82					
74	58	42	C2	P83					
75	59	43	VLC3	P84					
76	60	44	VLC2	P85					
77	61	45	VLC1						
78	62	46	VDD30						
79	63	47	VDD18						
80	64	48	VDD11						

\* See Table:1.3.3 for LCD control pins.

# 1.4 Pin Description

## 1.4.1 Pin Configuration

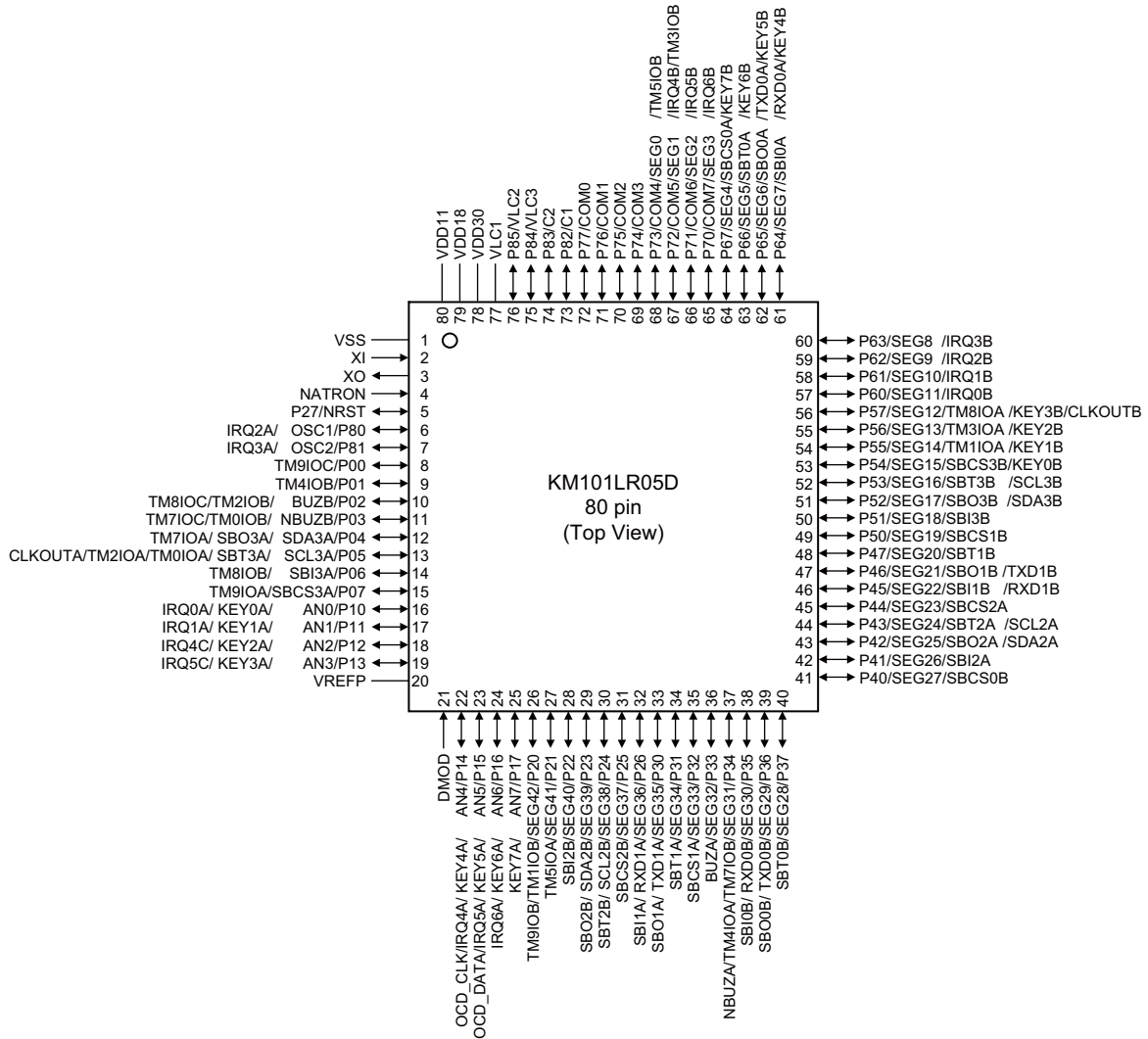


Figure:1.4.1 KM101LR05D Pin Configuration

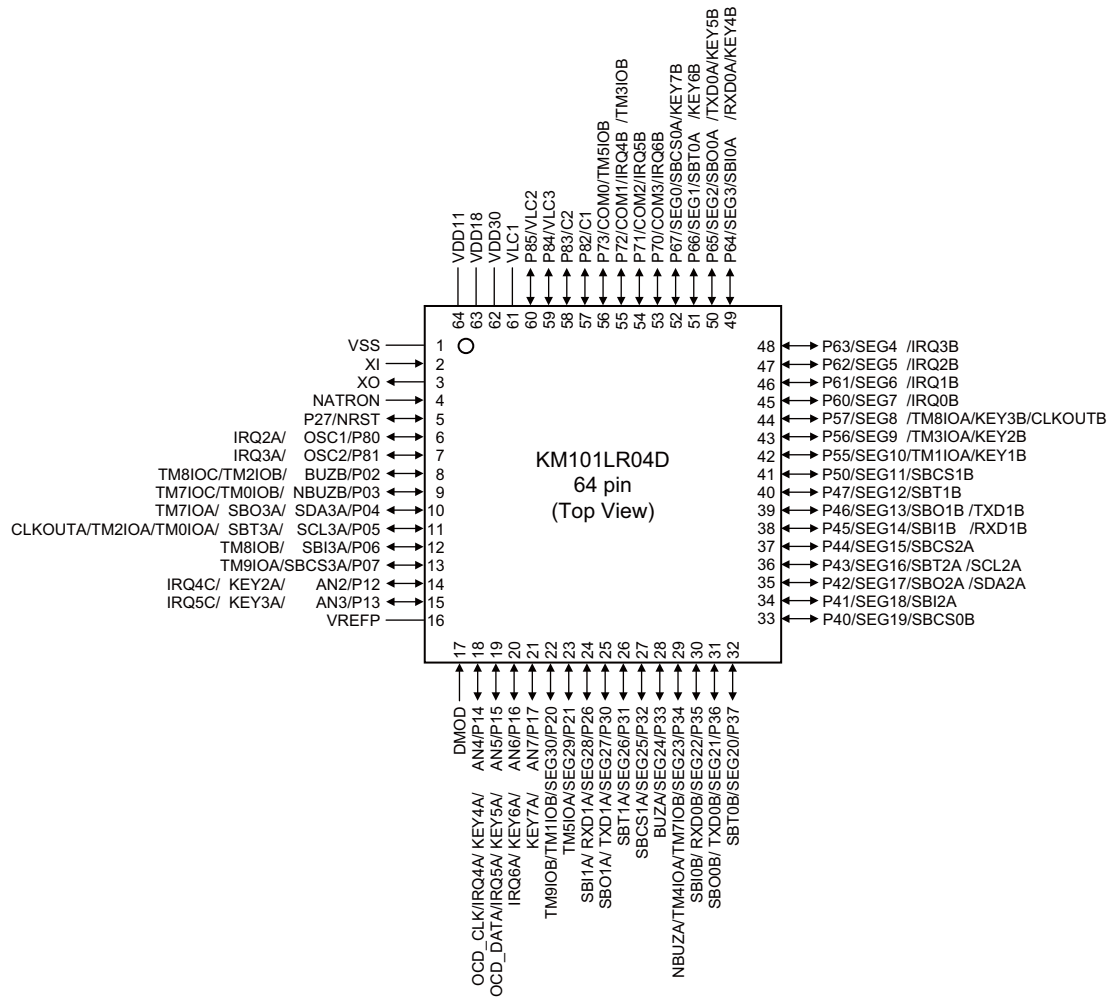


Figure:1.4.2 KM101LR04D Pin Configuration

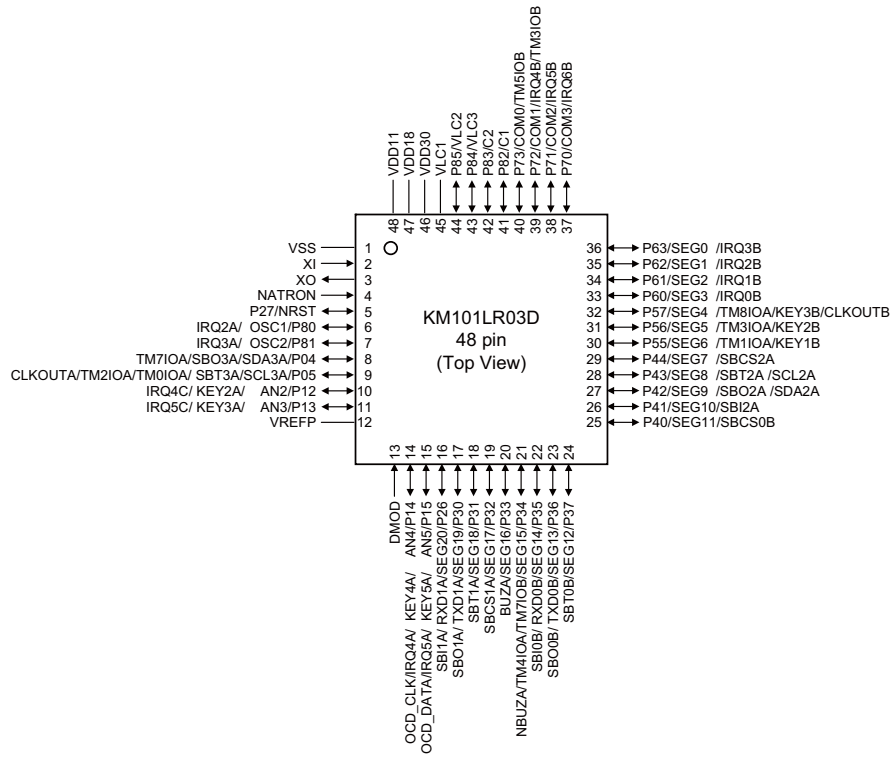


Figure:1.4.3 KM101LR03D Pin Configuration

## 1.4.2 Pin Description

Table:1.4.1 Power Supply/Oscillation/Reset/Mode Pin

Pin name	Input/ Output	Description
KM101LR 05D/04D/03D		
VDD30 VSS	-	Power supply pin Connect the capacitor of 1 $\mu$ F or more between VDD30 and VSS. Apply 0 V to VSS.
VDD18	-	Internal power output pin Connect the capacitor of 1 $\mu$ F between VDD18 and VSS to stable $V_{DD18}$ . Connect the bypass capacitor of 0.1 $\mu$ F between VDD18 and VSS.
VDD11	-	Internal power output pin (1.1 V) Connect the capacitor of 1 $\mu$ F or more between VDD11 and VSS.
VLC1 VLC2 VLC3	-	LCD power supply pin Supply the power under the following conditions. ( $V_{DD30} \leq V_{LC1} \leq 3.6$ V and $0$ V $\leq V_{LC3} \leq V_{LC2} \leq V_{LC1}$ ) Capacitors described in [Chapter LCD] of LSI User's Manual must be connected in each pin. When LCD function is not used, connect $V_{LC1}$ to $V_{DD30}$ .
C1 C2	-	LCD voltage boost capacitor pin When using the internal LCD booster circuit, connect the capacitor of 0.22 $\mu$ F between C1 and C2.
VREFP	-	ADC Reference power supply pin When ADC is not used, connect VREFP to VDD30. The voltage level of VREFP must be over 0.8 $V_{DD30}$ at any time including LSI power on.
OSC1 OSC2	Input Output	External high-speed oscillation pin When the external high-speed oscillation is needed, connect the oscillator to the pins. The external clock can be input through OSC1, and leave OSC2 open.
XI XO	Input Output	External low-speed oscillation pin When the external low-speed oscillation is needed, connect the oscillator to the pins.
NRST	Input Output	Reset pin (N-channel open drain pin) When NRST is set to "Low", LSI is initialized. LSI reset condition is described in [Chapter CPU] of LSI User's Manual.
DMOD	Input	Mode setting pin Always set DMOD to "Low" level, except for connecting the external LSI debugger or serial programmer.
NATRON	Input	Auto reset control pin To use the auto reset function, set NATRON to "Low" level. If not, set NATRON to "High" level.



The voltage level of VREFP must be over 0.8  $V_{DD30}$  at any time including LSI power on.

Table:1.4.2 General-purpose Port Function Pin

Pin name			Input/ Output	Output drive strength selectable	Description
KM101LR 05D	KM101LR 04D	KM101LR 03D			
P00	-	-	Input/ Output	Yes	Port 0 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected. -The drive strength of output Nch transistor can be changed.
P01	-	-		Yes	
P02	P02	-		Yes	
P03	P03	-		Yes	
P04	P04	P04		Yes	
P05	P05	P05		Yes	
P06	P06	-		Yes	
P07	P07	-		Yes	
P10	-	-	Input/ Output	No	Port 1 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected.
P11	-	-		No	
P12	P12	P12		No	
P13	P13	P13		No	
P14	P14	P14		No	
P15	P15	P15		No	
P16	P16	-		No	
P17	P17	-		No	
P20	P20	-	Input/ Output	Yes	Port 2 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected. -The drive strength of output Nch transistor can be changed.
P21	P21	-		Yes	
P22	-	-		Yes	
P23	-	-		Yes	
P24	-	-		Yes	
P25	-	-		Yes	
P26	P26	P26		Yes	
P27	P27	P27	Input/ Output	No	Port 2 -LSI is reset by setting P2OUT.P2OUT7 to "0".
P30	P30	P30	Input/ Output	Yes	Port 3 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected. -The drive strength of output Nch transistor can be changed.
P31	P31	P31		Yes	
P32	P32	P32		Yes	
P33	P33	P33		Yes	
P34	P34	P34		Yes	
P35	P35	P35		Yes	
P36	P36	P36		Yes	
P37	P37	P37		Yes	



# KM101LR05D/04D/03D

Pin name			Input/ Output	Output drive strength selectable	Description
KM101LR 05D	KM101LR 04D	KM101LR 03D			
P40	P40	P40	Input/ Output	Yes	Port 4 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected. -The drive strength of output Nch transistor can be changed.
P41	P41	P41		Yes	
P42	P42	P42		Yes	
P43	P43	P43		Yes	
P44	P44	P44		Yes	
P45	P45	-		Yes	
P46	P46	-		Yes	
P47	P47	-		Yes	
P50	P50	-	Input/ Output	Yes	Port 5 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected. -The drive strength of output Nch transistor can be changed.
P51	-	-		Yes	
P52	-	-		Yes	
P53	-	-		Yes	
P54	-	-		Yes	
P55	P55	P55		Yes	
P56	P56	P56		Yes	
P57	P57	P57		Yes	
P60	P60	P60	Input/ Output	Yes	Port 6 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected. -The drive strength of output Nch transistor can be changed.
P61	P61	P61		Yes	
P62	P62	P62		Yes	
P63	P63	P63		Yes	
P64	P64	-		Yes	
P65	P65	-		Yes	
P66	P66	-		Yes	
P67	P67	-		Yes	
P70	P70	P70	Input/ Output	Yes	Port 7 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected. -The drive strength of output Nch transistor can be changed.
P71	P71	P71		Yes	
P72	P72	P72		Yes	
P73	P73	P73		Yes	
P74	-	-		Yes	
P75	-	-		Yes	
P76	-	-		Yes	
P77	-	-		Yes	
P80	P80	P80	Input/ Output	No	Port 8 -At each port, the I/O direction and the pull-up resistor connection is controlled individually. -At LSI reset, each pin is set to input mode and the pull-up resistor is not connected.
P81	P81	P81		No	
P82	P82	P82		No	
P83	P83	P83		No	
P84	P84	P84		No	
P85	P85	P85		No	

Table:1.4.3 Special Function Pin

Pin name			Input/ Output	Description
KM101LR05D	KM101LR04D	KM101LR03D		
SBI0A(RXD0A) SBI0B(RXD0B) SBI1A(RXD1A) SBI1B(RXD1B) SBI2A SBI2B SBI3A SBI3B	SBI0A(RXD0A) SBI0B(RXD0B) SBI1A(RXD1A) SBI1B(RXD1B) SBI2A SBI3A	SBI0B(RXD0B) SBI1A(RXD1A)  SBI2A  SBI3A	Input	Serial data input pins -Pull-up resistor can be added by setting PnPLUP. -Select the input mode by setting PnDIR. -Select the serial data input by setting SCnMD1.SCnSBIS. (n = 0,1,2,3)
SBO0A(TXD0A) SBO0B(TXD0B) SBO1A(TXD1A) SBO1B(TXD1B) SBO2A(SDA2A) SBO2B(SDA2B) SBO3A(SDA3A) SBO3B(SDA3B)	SBO0A(TXD0A) SBO0B(TXD0B) SBO1A(TXD1A) SBO1B(TXD1B) SBO2A(SDA2A) SBO3A(SDA3A)	SBO0B(TXD0B) SBO1A(TXD1A)  SBO2A(SDA2A)  SBO3A(SDA3A)	Input/ Output	Serial data I/O pins -Pull-up resistor can be added by setting PnPLUP. -Select the output mode by setting PnDIR. -Select the serial data output by setting SCnMD1.SCnSBOS. (n = 0,1,2,3) -Select the push-pull or Nch-open drain by setting PnODC.
SBT0A SBT0B SBT1A SBT1B SBT2A(SCL2A) SBT2B(SCL2B) SBT3A(SCL3A) SBT3B(SCL3B)	SBT0A SBT0B SBT1A SBT1B SBT2A(SCL2A) SBT3A(SCL3A)	SBT0B SBT1A  SBT2A(SCL2A)  SBT3A(SCL3A)	Input/ Output	Serial clock I/O pins -Pull-up resistor can be added by setting PnPLUP. -Select the input or output mode by setting PnDIR. -Select the serial clock I/O by setting SCnMD1.SCnSBTS. (n = 0,1,2,3) -Select the push-pull or Nch-open drain by setting PnODC.
SBCS0A/SBCS0B SBCS1A/SBCS1B SBCS2A/SBCS2B SBCS3A/SBCS3B	SBCS0A/SBCS0B SBCS1A/SBCS1B SBCS2A SBCS3A	SBCS0B SBCS1A SBCS2A SBCS3A	Input/ Output	Serial chip select I/O pins -Pull-up resistor can be added by setting PnPLUP. -Select the input or output mode by setting PnDIR. -Select the serial chip select I/O by setting SCnMD3.SCnSBTS. (n = 0,1) or SCnMD2.SCnSBCSEN(n = 2,3)
TM0IOA/TM0IOB TM1IOA/TM1IOB TM2IOA/TM2IOB TM3IOA/TM3IOB TM4IOA/TM4IOB TM5IOA/TM5IOB TM7IOA/TM7IOB/ TM7IOC TM8IOA/TM8IOB/ TM8IOC TM9IOA/TM9IOB TM9IOC	TM0IOA/TM0IOB TM1IOA/TM1IOB TM2IOA/TM2IOB TM3IOA/TM3IOB TM4IOA TM5IOA/TM5IOB TM7IOA/TM7IOB/ TM7IOC TM8IOA/TM8IOB/ TM8IOC TM9IOA/TM9IOB	TM0IOA TM1IOA TM2IOA TM3IOA/TM3IOB TM4IOA TM5IOB TM7IOA/TM7IOB  TM8IOA	Input/ Output	Timer I/O pins -When capturing the external event signal, select the input mode by setting PnDIR. -To output the timer output signal, select the output mode by setting PnDIR, and the output port with TMIOENn/TMIOSELn (n = 0,1).
AN0/AN1/AN2/AN3/ AN4/AN5/AN6/AN7	AN2/AN3/ AN4/AN5/AN6/AN7	AN2/AN3/ AN4/AN5	Input	Analog input pins for ADC -Select the analog input pin with ANEN0.
IRQ0A/IRQ0B IRQ1A/IRQ1B IRQ2A/IRQ2B IRQ3A/IRQ3B IRQ4A/IRQ4B/ IRQ4C IRQ5A/IRQ5B/ IRQ5C IRQ6A/IRQ6B	IRQ0B IRQ1B IRQ2A/IRQ2B IRQ3A/IRQ3B IRQ4A/IRQ4B/ IRQ4C IRQ5A/IRQ5B/ IRQ5C IRQ6A/IRQ6B	IRQ0B IRQ1B IRQ2A/IRQ2B IRQ3A/IRQ3B IRQ4A/IRQ4B/ IRQ4C IRQ5A/IRQ5B/ IRQ5C IRQ6B	Input	External interrupt input pins -Select the external interrupt pin with IRQIEN, IRQISEL0 and IRQISEL1.

# KM101LR05D/04D/03D

Pin name			Input/ Output	Description
KM101LR05D	KM101LR04D	KM101LR03D		
KEY0A/KEY0B KEY1A/KEY1B KEY2A/KEY2B KEY3A/KEY3B KEY4A/KEY4B KEY5A/KEY5B KEY6A/KEY6B KEY7A/KEY7B	KEY1B KEY2A/KEY2B KEY3A/KEY3B KEY4A/KEY4B KEY5A/KEY5B KEY6A/KEY6B KEY7A/KEY7B	KEY1B KEY2A/KEY2B KEY3A/KEY3B KEY4A KEY5A KEY6A	Input	Key interrupt input pins -Select the key interrupt pin with KEYIEN and KEYSSEL.
COM0-7	COM0-3	COM0-3	Output	LCD common output pins -Select the common output pin with LCCTRn.
SEG0-42	SEG0-30	SEG0-20	Output	LCD segment output pins -Select the segment output pin with LCCTRn.
BUZA/BUZB	BUZA/BUZB	BUZA	Output	Buzzer output pin -Select the buzzer output pin with BUZCNT.
NBUZA/NBUZB	NBUZA/NBUZB	NBUZA	Output	Inverted Buzzer output pin -Select the inverted buzzer output pin with BUZCNT.
CLKOUTA/ CLKOUTB	CLKOUTA/ CLKOUTB	CLKOUTA/ CLKOUTB	Output	Clock output pins -Select the clkout pin with CLKOUT.
OCD_CLK OCD_DATA	OCD_CLK OCD_DATA	OCD_CLK OCD_DATA	Input/ Output	On-board debugger I/O pins These pins are used for on-board debugging.

# 1.5 Electrical Characteristics

## 1.5.1 Absolute Maximum Ratings

A. Absolute Maximum Ratings \*2 \*3

 $V_{SS} = 0\text{ V}$ 

Parameter		Symbol	Rating	Unit	
A1	Supply voltage	$V_{DD30}$	-0.3 to +4.6	V	
A2	Input pin voltage	$V_I$	-0.3 to $V_{DD30} + 0.3$ (up to 4.6)	V	
A3	Output pin voltage	$V_O$	-0.3 to $V_{DD30} + 0.3$ (up to 4.6)		
A4	Input/Output pin voltage	$V_{IO1}$	-0.3 to $V_{DD30} + 0.3$ (up to 4.6)		
A5	Peak output current	Except P1/8 *4	$I_{OL1}$ (peak)	30	mA
A6		P1/8	$I_{OL2}$ (peak)	10	
A7		All pins	$I_{OH}$ (peak)	-10	
A8	Average output current *1	Except P1/8 *4	$I_{OL1}$ (avg)	20	
A9		P1/8	$I_{OL2}$ (avg)	5	
A10		All pins	$I_{OH}$ (avg)	-5	
A11	Total output current for all pins *1	$I_{TOL}$	60		
A12		$I_{TOH}$	-60		
A13	Power dissipation	$P_T$	230 ( $T_a = +85\text{ °C}$ )	mW	
A14	Operating ambient temperature	$T_{opr}$	-40 to +85	°C	
A15	Storage temperature	$T_{stg}$	-55 to +125		

\*1 The values are applied to any period of 100 ms.

\*2 To stabilize the internal power supply voltage, connect bypass capacitors as follows to at least one or more points close to the LSI: Capacitors of 1 $\mu$ F or more between VDD30 and VSS, Capacitors of 0.1  $\mu$ F and 1 $\mu$ F or more between VOUT18 and VSS.

\*3 The absolute maximum ratings are the limit values beyond which the IC may be damaged. Operation is not guaranteed under these conditions.

\*4 The value is applied when selecting the large current output by setting PnNLC register.

## 1.5.2 Operating Condition

### B. Operating Condition

$V_{SS} = 0\text{ V}$   
 $T_a = -40\text{ °C to }+85\text{ °C}$

Parameter	Symbol	Condition	Limits			Unit	
			MIN	TYP	MAX		
Supply voltage *6							
B1	Supply voltage	$V_{DD1}$	$f_{\text{SYSCLK}} \leq 10.0\text{ MHz}$	1.8	--	3.6	V
B2		$V_{DD2}$	$f_{\text{SYSCLK}} \leq 1.0\text{ MHz}^*7$	1.3	--	3.6	
B3		$V_{DD3}$	$f_{\text{SYSCLK}} \leq 40\text{ kHz}^*8^*10$	1.1	--	3.6	
B4	RAM retention supply voltage	$V_{DD4}$	At STOP mode *10	1.1	--	3.6	
Operating speed *9							
B5	Instruction execution time $1/f_{\text{SYSCLK}}$	$t_{c1}$	$V_{DD30} = 1.8\text{ V to }3.6\text{ V}$	0.1	--	--	$\mu\text{s}$
B6		$t_{c2}$	$V_{DD30} = 1.3\text{ V to }3.6\text{ V}$	1.0	--	--	
B7		$t_{c3}$	$V_{DD30} = 1.1\text{ V to }3.6\text{ V}^*10$	25.0	--	--	

\*6  $f_{\text{SYSCLK}}$ : Frequency for the system clock

\*7 When  $f_{\text{SYSCLK}}$  is generated by using the internal high-speed oscillation.

\*8 When  $f_{\text{SYSCLK}}$  is generated by using the external low-speed oscillation or the internal low-speed oscillation.

\*9  $t_{c1,2}$ : When  $f_{\text{SYSCLK}}$  is generated by using the internal high-speed oscillation or the external high-speed oscillation.  
 (However, for  $t_{c2}$ , only by using the internal high-speed oscillation)  
 $t_{c3}$ : When  $f_{\text{SYSCLK}}$  is generated by using the internal low-speed oscillation.

\*10 When using auto reset function, the lowest voltage is the auto reset detection voltage.

$V_{DD30} = V_{RSTL}$  to 3.6 V,  $V_{SS} = 0\text{ V}$   
 $V_{RSTL} = 1.1\text{ V}$  at auto reset function  
 $T_a = -40\text{ °C to }+85\text{ °C}$

Parameter	Symbol	Condition	Limits			Unit	
			MIN	TYP	MAX		
External high-speed oscillation Figure:1.5.1							
B8	Frequency	$F_{\text{HOSCCLK}}$	$V_{DD30} = 1.8\text{ V to }3.6\text{ V}$	1.0	--	10.0	MHz
External low-speed oscillation Figure:1.5.2							
B9	Frequency	$F_{\text{SOSCCLK}}$	$V_{DD30} = V_{RSTL}$ to 3.6 V	--	32.768	--	kHz
Internal high-speed RC oscillation *11							
B10	Frequency	$F_{\text{HRCCLK10}}$	$V_{DD30} = 1.8\text{ V to }3.6\text{ V}$ FCNT = "00"	--	10	--	MHz
B11		$F_{\text{HRCCLK8}}$	$V_{DD30} = 1.8\text{ V to }3.6\text{ V}$ FCNT = "01"	--	8	--	MHz
B12		$F_{\text{HRCCLK1}}$	$V_{DD30} = 1.3\text{ V to }3.6\text{ V}$ FCNT = "10"	--	1	--	MHz

$V_{DD30} = V_{RSTL}$  to 3.6 V,  $V_{SS} = 0$  V  
 $V_{RSTL} = 1.1$  V at auto reset function  
 $T_a = -40$  °C to +85 °C

Parameter		Symbol	Condition	Limits			Unit
				MIN	TYP	MAX	
B13	Temperature/Voltage dependence	$E_{F1}$	$f_{HRCCLK} = 8/10$ MHz $T_a = 0$ °C to +50 °C	-1.5	--	1.5	%
B14		$E_{F2}$	$f_{HRCCLK} = 8/10$ MHz $T_a = -40$ °C to +85 °C	-3.0	--	3.0	
B15	Temperature/Voltage dependence	$E_{F5}$	$f_{HRCCLK} = 1$ MHz $T_a = -40$ °C to +85 °C	-10.0	--	10.0	%
Internal low-speed RC oscillation							
B16	Frequency	$F_{SRCCLK}$	$V_{DD30} = V_{RSTL}$ to 3.6 V	--	40	--	kHz
B17	Temperature/Voltage dependence	$E_{F6}$	$T_a = -40$ °C to +85 °C	-20.0	--	20.0	%

\*11 Output frequency of the internal high-speed RC oscillation can be selected by setting the FCNT bit of HCLKCNT register.

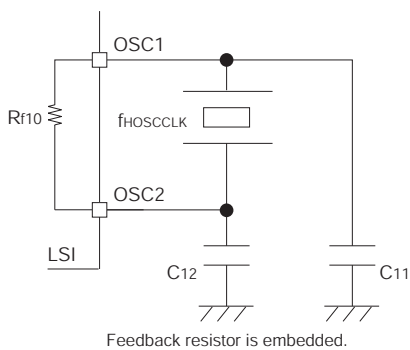


Figure:1.5.1 High-speed oscillation

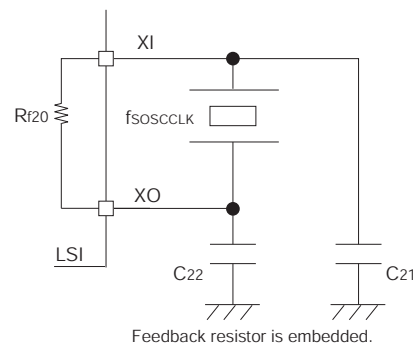


Figure:1.5.2 Low-speed oscillation



Connect the external capacitance to match the oscillator used.  
 When using the crystal or ceramic oscillator, consult your oscillator manufacturer to decide the external capacitance value since the oscillation frequency changes depending on the capacitor value.



The external low-speed oscillation of other than 32.768 kHz can't be used.

$V_{DD30} = 1.8\text{ V to }3.6\text{ V}, V_{SS} = 0\text{ V}$   
 $V_{RSTL} = 1.1\text{ V}$  at auto reset function  
 $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$

Parameter	Symbol	Condition	Limits			Unit
			MIN	TYP	MAX	
External clock input 1 OSC1 (OSC2 is open.)						
B18	Clock frequency	$f_{HOSCCLK}$	1.0	--	10.0	MHz
B19	High period time *12	$t_{wh1}$	45	--	--	ns
B20	Low period time *12	$t_{wl1}$				
B21	Rise time	$t_{wr1}$	--	--	5.0	
B22	Fall time	$t_{wf1}$	--	--	5.0	

\*12 Set the clock duty ratio to the value from 45 % to 55 %.

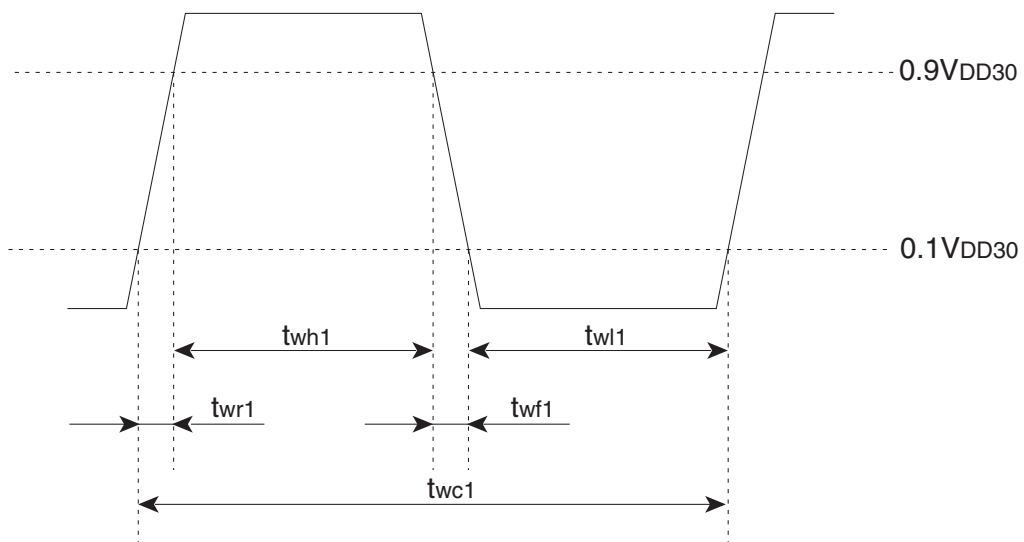


Figure:1.5.3 OSC1 timing diagram

1.5.3 DC Characteristics

C. DC Characteristics

$V_{SS} = 0\text{ V}$   
 $T_a = -40\text{ °C to }+85\text{ °C}$

Parameter	Symbol	Condition	Limits			Unit
			MIN	TYP	MAX	
Supply current *13						
C1 *14	$I_{DD1}$	$f_{HOSCCLK} = 10\text{ MHz}$ $V_{DD30} = 3.0\text{ V}, V_{DD18} = 1.8\text{ V}$ $[f_{SYSCLK} = f_{HOSCCLK}]$	--	2.1	3.1	mA
C2	$I_{DD2}$	$f_{HRCCLK} = 10\text{ MHz}$ $V_{DD30} = 3.0\text{ V}, V_{DD18} = 1.8\text{ V}$ $[f_{SYSCLK} = f_{HRCCLK}]$	--	2.1	3.0	
C3	$I_{DD3}$	$f_{HRCCLK} = 8\text{ MHz}$ $V_{DD30} = 3.0\text{ V}, V_{DD18} = 1.8\text{ V}$ $[f_{SYSCLK} = f_{HRCCLK}]$	--	1.72	2.5	
C4	$I_{DD4}$	$f_{HRCCLK} = 8\text{ MHz}$ $V_{DD30} = 3.0\text{ V}, V_{DD18} = 1.8\text{ V}$ $[f_{SYSCLK} = f_{HRCCLK}/2]$	--	0.94	1.5	
C5	$I_{DD5}$	$f_{HOSCCLK} = 4\text{ MHz}$ $V_{DD30} = 3.0\text{ V}, V_{DD18} = 1.8\text{ V}$ $[f_{SYSCLK} = f_{HOSCCLK}]$	--	0.84	1.3	
C6	$I_{DD6}$	$f_{HRCCLK} = 1\text{ MHz}$ $V_{DD30} = 3.0\text{ V}, V_{DD18} = 1.3\text{ V}$ $[f_{SYSCLK} = f_{HRCCLK}]$	--	0.22	0.36	
C7	$I_{DD7}$	$f_{SOSCCLK} = 32.768\text{ kHz}$ $V_{DD30} = 3.0\text{ V}, V_{DD18} = 1.1\text{ V}$ $[f_{SYSCLK} = f_{SOSCCLK}]$	--	5.6	9.5	$\mu\text{A}$
C8	$I_{DD8}$	$f_{SRCCLK} = 40\text{ kHz}$ $V_{DD30} = 3.0\text{ V}, V_{DD18} = 1.1\text{ V}$ $[f_{SYSCLK} = f_{SRCCLK}]$	--	6.7	11.6	



## C. DC Characteristics

$V_{SS} = 0\text{ V}$   
 $T_a = -40\text{ °C to }+85\text{ °C}$

Parameter		Symbol	Condition	Limits			Unit	
				MIN	TYP	MAX		
C9	Supply current in HALT	$I_{DD9}$	HALT0 mode $f_{HRCCLK} = 8\text{ MHz}$ $V_{DD30} = 3.0\text{ V}, V_{DD18} = 1.1\text{ V}$	--	0.24	0.33	$\mu\text{A}$	
C10		$I_{DD10}$	HALT2 mode $f_{SOSCCLK} = 32.768\text{ kHz}$ $V_{DD30} = 3.0\text{ V}, V_{DD18} = 1.1\text{ V}$ $T_a = 25\text{ °C}$ (HOSCCLK/HRCCLK/SRCCLK are stopped)	--	0.2	0.4		
C11		$I_{DD11}$	HALT3 mode $f_{SOSCCLK} = 32.768\text{ kHz}$ $V_{DD30} = 3.0\text{ V}, V_{DD18} = 1.1\text{ V}$ $T_a = 25\text{ °C}, \text{HALTMOD} = 1$ (HOSCCLK/HRCCLK/SRCCLK are stopped)	--	0.5	0.7		
C12		$I_{DD12}$	HALT3 mode $f_{SOSCCLK} = 32.768\text{ kHz}$ $V_{DD30} = 3.0\text{ V}, V_{DD18} = 1.1\text{ V}$ $T_a = 85\text{ °C}, \text{HALTMOD} = 1$ (HOSCCLK/HRCCLK/SRCCLK are stopped)	--	--	2.9		
C13		Supply current in STOP	$I_{DD13}$	$V_{DD30} = 3.0\text{ V}, V_{DD18} = 1.1\text{ V}$ $T_a = 25\text{ °C}$ (HOSCCLK/HRCCLK/SOSCCLK/SRCCLK are stopped)	--	0.06		0.24
C14			$I_{DD14}$	$V_{DD30} = 3.0\text{ V}, V_{DD18} = 1.1\text{ V}$ $T_a = 85\text{ °C}$ (HOSCCLK/HRCCLK/SOSCCLK/SRCCLK are stopped)	--	--		2.6

\*13 The supply current is measured with  $T_a = 25\text{ °C}$ , no-load, and all the analog part in the power-down state. (The pull-up/down resistors are not connected.) Each supply current is measured with the following conditions.

$I_{DD1,5}$  (Operating supply current): After setting all input and output pins to the input mode,  $V_{DD18}$  (the Logic supply voltage) to 1.8 V, the oscillation mode to NORMAL (the external oscillation), hold the input pins to  $V_{DD30}$  level and input the 10/4 MHz square wave, which has the amplitude from  $V_{DD30}$  to  $V_{SS}$ , from OSC1 pin.

$I_{DD2,3,4}$  (Operating supply current): After setting all input and output pins to the input mode,  $V_{DD18}$  (the Logic supply voltage) to 1.8 V, the oscillation mode to NORMAL (the internal high-oscillation: 10/8 MHz), hold the input pins to  $V_{DD30}$  level.

$I_{DD6}$  (Operating supply current): After setting all input and output pins to the input mode,  $V_{DD18}$  (the Logic supply voltage) to 1.3 V, the oscillation mode to NORMAL (the internal high-oscillation: 1 MHz), hold the input pins to  $V_{DD30}$  level.

$I_{DD7}$  (Operating supply current): After setting all input and output pins to the input mode,  $V_{DD18}$  (the Logic supply voltage) to 1.1 V, the oscillation mode to SLOW (the external oscillation), hold the input pins to  $V_{DD30}$  level and input the 32.768 kHz square wave, which has the amplitude from  $V_{DD11}$  to  $V_{SS}$ , from XI pin.

$I_{DD8}$  (Operating supply current): After setting all input and output pins to the input mode,  $V_{DD18}$  (the Logic supply voltage) to 1.1 V, the oscillation mode to SLOW (the internal low-oscillation: 40 kHz), hold the input pins to  $V_{DD30}$  level.

$I_{DD9}$  (Supply current in HALT): After setting all input and output pins to the input mode, the oscillation mode to HALT0 (the internal high-oscillation), hold the input pins to  $V_{DD30}$  level.

$I_{DD10}$  (Supply current in HALT): After setting all input and output pins to the input mode, the oscillation mode to HALT2 (the external low-oscillation), hold the input pins to  $V_{DD30}$  level and input the 32.768 kHz square wave, which has the amplitude from  $V_{DD11}$  to  $V_{SS}$ , from XI pin.

$I_{DD11,12}$  (Supply current in HALT): After setting all input and output pins to the input mode, the oscillation mode to HALT3 (the external low-oscillation), hold the input pins to  $V_{DD30}$  level and input the 32.768 kHz square wave, which has the amplitude from  $V_{DD11}$  to  $V_{SS}$ , from XI pin.

$I_{DD13,14}$  (Supply current in STOP): After setting  $V_{DD18}$  (the Logic supply voltage) to 1.1 V and the oscillation mode to STOP, hold the input pins to  $V_{DD30}$  level and make OSC1 and XI pins open.

# KM101LR05D/04D/03D

$V_{DD30} = V_{RSTL}$  to 3.6 V,  $V_{SS} = 0$  V  
 $V_{RSTL} = 1.1$  V at auto reset function  
 $T_a = -40$  °C to +85 °C

Parameter		Symbol	Condition	Limits			Unit
				MIN	TYP	MAX	
Input pin 1 NATRON (Schmitt input)							
C15	High-level input voltage	$V_{IH1}$		$0.8V_{DD30}$	--	$V_{DD30}$	V
C16	Low-level input voltage	$V_{IL1}$		0	--	$0.2V_{DD30}$	
C17	Input leakage current	$I_{LK1}$	$V_I = 0$ V to $V_{DD30}$	--	--	$\pm 1$	$\mu$ A
Input pin 2 DMOD (Schmitt input)							
C18	High-level input voltage	$V_{IH2}$		$0.8V_{DD30}$	--	$V_{DD30}$	V
C19	Low-level input voltage	$V_{IL2}$		0	--	$0.2V_{DD30}$	
C20	Pull-down resistance	$I_{RL2}$	$V_{DD30} = 3.0$ V, $V_I = V_{DD30}$	30	100	300	k $\Omega$
Input/Output pin 3 (Schmitt input) KM101LR05D: P10 to P17, P80 to P85 KM101LR04D: P12 to P17, P80 to P85 KM101LR03D: P12 to P15, P80 to P85							
C21	High-level input voltage	$V_{IH3}$		$0.8V_{DD30}$	--	$V_{DD30}$	V
C22	Low-level input voltage	$V_{IL3}$		0	--	$0.2V_{DD30}$	
C23	Input leakage current	$I_{LK3}$	$V_I = 0$ V to $V_{DD30}$	--	--	$\pm 1$	$\mu$ A
C24	Pull-down resistance	$I_{RH3}$	$V_{DD30} = 3.0$ V, $V_I = V_{SS}$ with pull-up resistor	30	100	300	k $\Omega$
C25	High-level output voltage	$V_{OH3}$	$V_{DD30} = 3.0$ V, $I_{OH} = -2.0$ mA	2.4	--	--	V
C26	Low-level output voltage	$V_{OL3}$	$V_{DD30} = 3.0$ V, $I_{OL} = 2.0$ mA	--	--	0.4	
Input/Output pin 4 (Schmitt input) KM101LR05D: P00 to P07, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77 KM101LR04D: P02 to P07, P20, P21, P26, P30 to P37, P40 to P47, P50, P55 to P57, P60 to P67, P70 to P73 KM101LR03D: P04, P05, P26, P30 to P37, P40 to P44, P55 to P57, P60 to P63, P70 to P73							
C27	High-level input voltage	$V_{IH4}$		$0.8V_{DD30}$	--	$V_{DD30}$	V
C28	Low-level input voltage	$V_{IL4}$		0	--	$0.2V_{DD30}$	
C29	Input leakage current	$I_{LK4}$	$V_I = 0$ V to $V_{DD30}$	--	--	$\pm 1$	$\mu$ A
C30	Pull-down resistance	$I_{RH4}$	$V_{DD30} = 3.0$ V, $V_I = V_{SS}$ with pull-up resistor	30	100	300	k $\Omega$
C31	High-level output voltage	$V_{OH4}$	$V_{DD30} = 3.0$ V, $I_{OH} = -2.0$ mA	2.4	--	--	V
C32	Low-level output voltage 1	$V_{OL41}$	$V_{DD30} = 3.0$ V, $I_{OL} = 2.0$ mA at Large output current OFF	--	--	0.4	
C33	Low-level output voltage 2	$V_{OL42}$	$V_{DD30} = 3.0$ V, $I_{OL} = 8.0$ mA at Large output current ON	--	--	0.4	

# KM101LR05D/04D/03D

$V_{DD30} = V_{RSTL}$  to 3.6 V,  $V_{SS} = 0$  V  
 $V_{RSTL} = 1.1$  V at auto reset function  
 $T_a = -40$  °C to +85 °C

Parameter	Symbol	Condition	Limits			Unit	
			MIN	TYP	MAX		
Input pin 5 P27(NRST) (Schmitt input)							
C34	High-level input voltage	$V_{IH5}$		$0.8V_{DD30}$	--	$V_{DD30}$	V
C35	Low-level input voltage	$V_{IL5}$		0	--	$0.15V_{DD30}$	
C36	Pull-down resistance	$I_{RH5}$	$V_{DD30} = 3.0$ V, $V_I = V_{SS}$ with pull-up resistor	30	100	300	k $\Omega$
Display output pin 1 KM101LR05D: COM0 to COM7 (at $V_{LC1}$ , $V_{SS}$ output) KM101LR04D: COM0 to COM3 (at $V_{LC1}$ , $V_{SS}$ output) KM101LR03D: COM0 to COM3 (at $V_{LC1}$ , $V_{SS}$ output)							
C37	Potential difference of output waveform	$V_{OCM}$	$V_{DD30} = V_{LC1} = 3.0$ V $I_{COM} = 10$ $\mu$ A	--	--	0.6	V
Display output pin 2 KM101LR05D: SEG0 to SEG42 (at $V_{LC1}$ , $V_{SS}$ output) KM101LR04D: SEG0 to SEG30 (at $V_{LC1}$ , $V_{SS}$ output) KM101LR03D: SEG0 to SEG20 (at $V_{LC1}$ , $V_{SS}$ output)							
C38	Voltage difference of output waveform	$V_{OSG}$	$V_{DD30} = V_{LC1} = 3.0$ V $I_{SEG} = 2$ $\mu$ A	--	--	0.6	V
LCD boost output pin 1 KM101LR05D: VLC1, VLC2, VLC3 (VLC3: Triple output compared to the reference voltage output) KM101LR04D: VLC1, VLC2, VLC3 (VLC3: Triple output compared to the reference voltage output) KM101LR03D: VLC1, VLC2, VLC3 (VLC3: Triple output compared to the reference voltage output)							
C39	Output voltage	$V_{LC1}$	$V_{DD30} = V_{RSTL}$ to 3.0 V $V_{LC3} = 1.0$ V, $T_a = 25$ °C LCD display OFF, SEG/COM with no load, LCD boost clock = 125 kHz	2.7	3.0	3.3	V
C40		$V_{LC2}$		1.8	2.0	2.2	
C41		$V_{LC3}$		0.9	1.0	1.1	

1.5.4 A/D Converter Characteristics

D. A/D Converter characteristics \*14

$V_{DD30} = 3.0\text{ V}$   $V_{SS} = 0\text{ V}$   
 $T_a = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$

Parameter		Symbol	Condition	Limits			Unit
				MIN	TYP	MAX	
D1	Resolution	RSL		--	--	12	Bits
D2	Nonlinearity error	INL	$V_{DD30} = 3.0\text{ V}$ , $V_{SS} = 0\text{ V}$ $V_{REFP} = 3.0\text{ V}$ $T_{AD} = 750\text{ ns}$	--	--	$\pm 4$	LSB
D3	Differential non-linearity error	DNL		--	--	$\pm 3$	
D4	Zero voltage transition	$E_{ZS}$		--	10	30	mV
D5	full-scale voltage transition	$E_{FS}$		2970	2990	--	
D6	AD conversion time	$t_{CV}$	$f_{SYSCLK} = 8\text{ MHz}$ , $T_{AD} = 750\text{ ns}$	15.38	--	--	$\mu\text{s}$
D7	Sampling time	$t_s$	$T_{AD} = 750\text{ ns}$	1.5	--	--	$\mu\text{s}$
D8	Reference voltage	$V_{REFP}$	$V_{REFP} \leq V_{DD30}$	1.8	--	$V_{DD30}$	V
D9	Analog input voltage	$V_{AIN}$		$V_{SS}$	--	$V_{REFP}$	
D10	Analog input leakage current	$I_{AINL}$	At channel off $V_{ADIN} = 0\text{ V}$ to $V_{DD30}$	--	--	$\pm 1$	$\mu\text{A}$

\*14  $T_{AD}$  denotes the clock cycle for A/D conversion.  
 The value from D2 to D5 are guaranteed under the condition of  $V_{DD30} = V_{REFP} = 3.0\text{ V}$  and  $V_{SS} = 0\text{ V}$ .

1.5.5 Reset/Power supply Detection Characteristics

E. Reset/Power supply Detection Characteristics

$V_{DD30} = V_{RSTL}$  to 3.6 V,  $V_{SS} = 0$  V  
 $V_{RSTL} = 1.1$  V at auto reset function  
 $T_a = -40$  °C to  $+85$  °C

Parameter	Symbol	Condition	Limits			Unit	
			MIN	TYP	MAX		
Reset							
E1	Operating supply current	$V_{DD3}$	With auto reset	$V_{RSTL}$	--	3.6	V
E2	Auto reset voltage detection level	$V_{RSTH}$	$V_{DD30} = \text{"Low"} \rightarrow \text{"High"}$	1.10	1.23	1.35	
E3		$V_{RSTL}$	$V_{DD30} = \text{"High"} \rightarrow \text{"Low"}$	1.10	1.18	1.30	
E4	Slope of voltage startup	$SL_{VDD30}$		--	--	1.0	V/ms
Power supply Detection							
E5	Detection voltage	$V_{LVI}$		1.00	1.10	1.20	V
				1.05	1.15	1.25	
				1.10	1.20	1.30	
				1.15	1.25	1.35	
				1.20	1.30	1.40	
				1.25	1.35	1.45	
				1.30	1.40	1.50	
				1.40	1.50	1.60	
				1.50	1.60	1.70	
				1.60	1.70	1.80	
				1.70	1.80	1.90	
				1.80	1.90	2.00	
				1.90	2.00	2.10	
				2.00	2.10	2.20	
				2.10	2.20	2.30	
				2.20	2.30	2.40	
				2.30	2.40	2.50	
2.40	2.50	2.60					
2.50	2.60	2.70					
2.60	2.70	2.80					
2.70	2.80	2.90					
2.80	2.90	3.00					

1.5.6 ReRAM Program Condition

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F. ReRAM Program Condition

$V_{DD30} = 1.8\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$   
 $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$

Parameter	Symbol	Condition	Limits			Unit	
			MIN	TYP	MAX		
F1	Supply voltage for programming	$V_{DDEW}$	1.8	--	3.6	V	
F2	Guaranteed number of rewriting *15	$NUM_{w1}$	Program area	1000	--	--	time
		$NUM_{w2}$	Data area	100000	--	--	
F3	Data hold time	$T_{HOLD}$	10	--	--	year	

\*15 The number of rewriting is counted by a byte unit.

# 1.6 Package Dimension

■ Package code: TQFP080-P-1212 Unit: mm

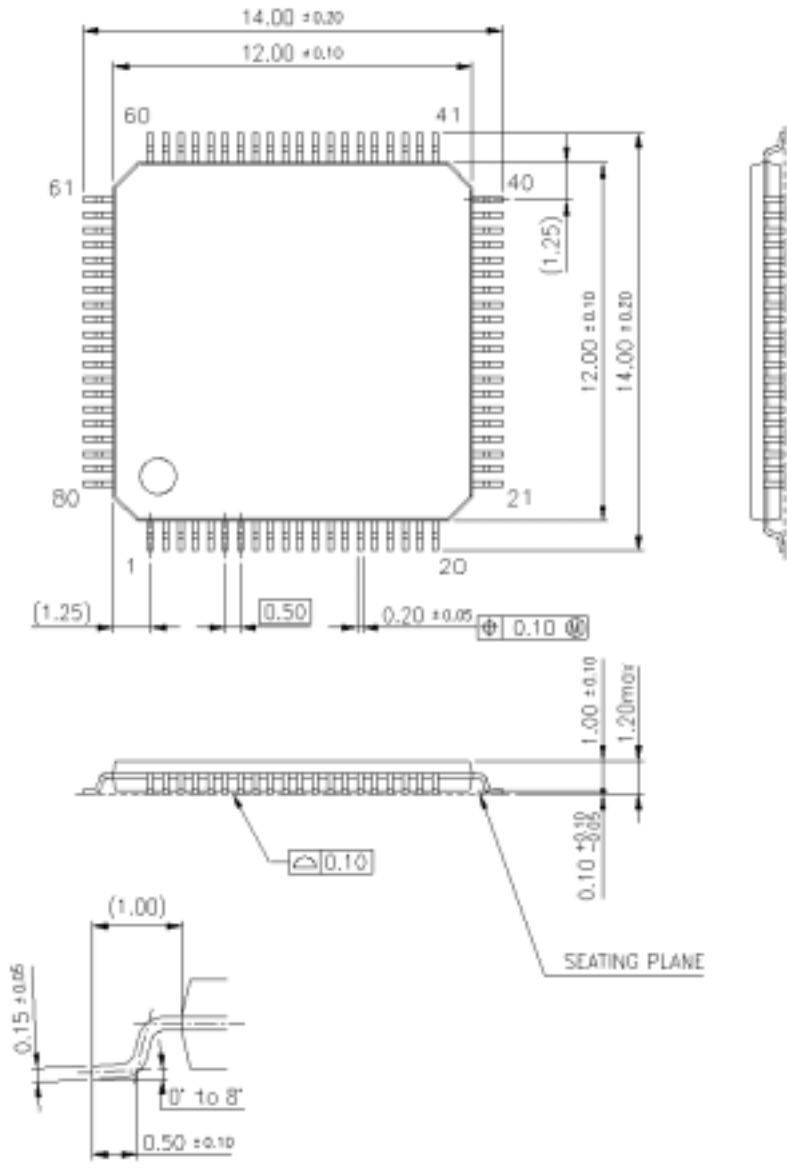


Figure:1.6.1 80-pin TQFP Package Dimension

■ Package code: TQFP064-P-1010 Unit: mm

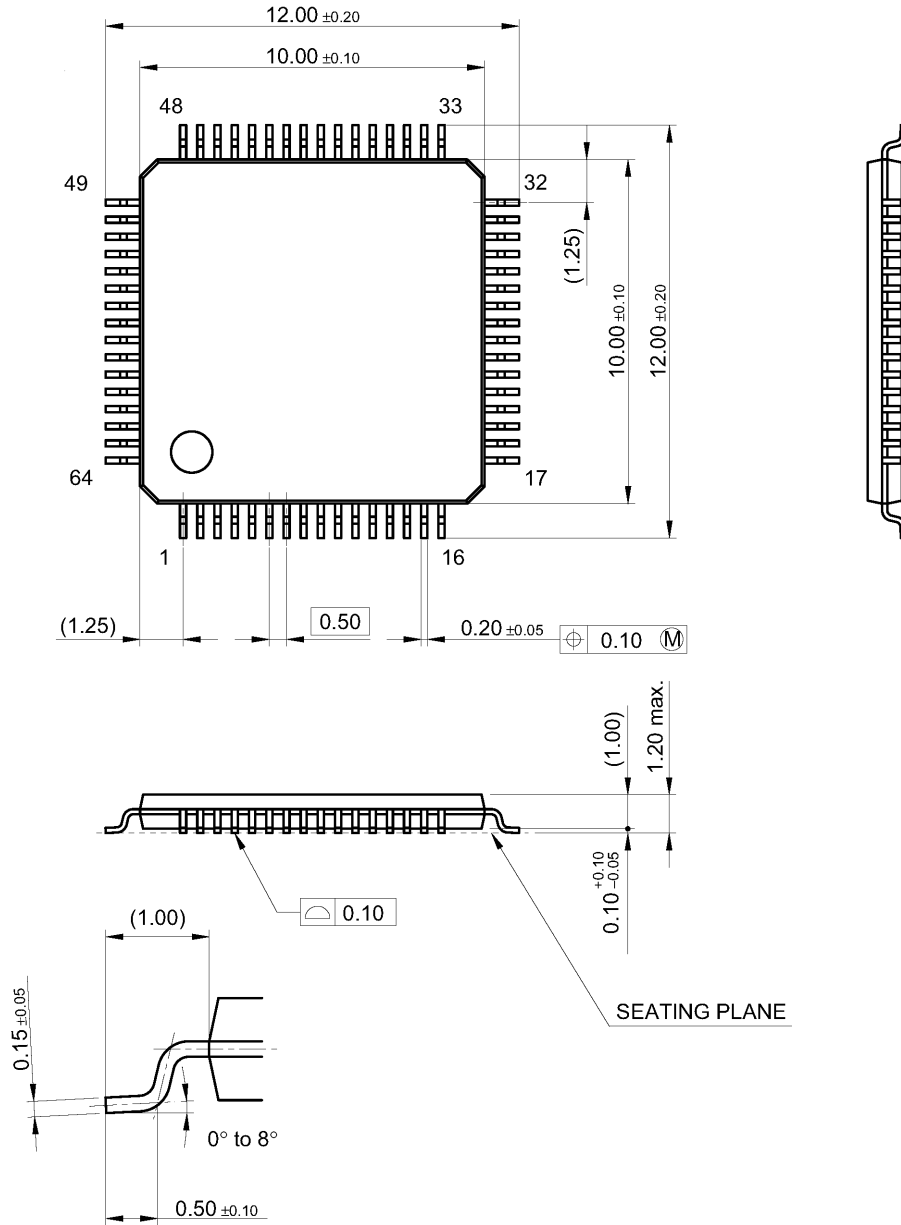


Figure:1.6.2 64-pin TQFP Package Dimension





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