# N572F072/P072

# Data Sheet

## 32-BIT MULTI-ALGORITHM VOICE PROCESSOR (NuVoice™)

*Release Date: Aug 2014*
*Revision 1.4*

# Table of Content

# 1. General Description

The N572F072 is the enhanced NuVoice™ series from N572F065. NuVoice is the first SoC specific for voice applications based on Cortex™-M0 CPU. It runs up to 48MHz and equips with 72KB flash and 8KB SRAM for high performance process of audio and voice algorithms. Integrating rich analog peripherals, like pre-amplifier, ADC, DAC, hardware mixer, and PA, this chip saves a lot of system design effort and cost.

To unfold the high performance M0 and high density of SRAM, advanced algorithms are designed, optimized, and tested with N572 chips. These algorithms include voice changer, low-bit rate compression – NuOne; NuSound; NuLite; NuVox, beat detection, pitch in and pitch out, talk2sing, and more in developing. In additional to algorithms developed by Nuvoton, we also seek third parties for more interesting features/software to enrich the applications on N572.

With the NVIC in M0, the latency of interrupt and response time to external events is very short and efficient. Multiple algorithms can be run together smoothly and naturally.

The development tools are based on Keil™ MDK using C/C++ programming language. This is a robust and easy to use environment for software development and debug. Features in Keil™ MDK are compiler, debugger, and profiler. With the Nu-Link™ and evaluation board, the overall system, including HW and SW, can work seamlessly in your system testing and verification. In this full-features development environment and tools, you can design and build application software in an efficient way and get optimized code that can best realize your idea on N572.

Following is a brief table of all Part No. of NuVoice Series:

| Part No. | N572F072 | N572P072 | N572F065 |
|---|---|---|---|
| Program ROM | 72KB Flash | 64KB OTP + 8KB Flash | 64KB Flash |
| SRAM | 8KB | | |
| CPU freq | 48MHz | | |
| SPI Interface | Master/Slave mode 12MHz, 1 set<br>Master mode 24MHz (3.3V), 1 set | | Master mode 12MHz, 2 sets |
| USB | N/A | N/A | FS/12Mbps |

# 2. Features

- **Core**
  - ARM® Cortex™-M0 core runs up to 48MHz
  - Support low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 16 interrupt inputs, each with 4-level of priority
  - 24-bit SysTick timer
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- **Widely operating voltage range from 2.4V to 5.5V**
- **Flash Memory**
  - 72KB Flash (for N572F072)
  - 64KB OTP and 8KB Flash (for N572P072)
  - Support ISP for Flash update
  - 512 bytes page erase for Flash
  - Support 2-wire ICP update from ICE interface

- Security Lock preventing content in Flash access from external interface

- **SRAM Memory**
  - 8KB embedded SRAM
- **Clock Control**
  - Flexible selection for different applications
  - Support PLL, up to 48MHz, for high performance system operation
  - External 32KHz crystal input for RTC function and system clock
  - Internal 48MHz RC oscillator
- **GPIO**
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
- **Timers**
  - 3 sets of the timer with 8-bit pre-scaler and 16-bit timer.
  - Counter auto reload.
  - IR carrier generator
  - One fixed frequency timer
- **Watch Dog Timer**
  - Default ON/OFF by configuration setting
  - Multiple clock sources
  - 8 selectable time out period from around 32ms ~ 8sec (based on 32768Hz clock)
  - Able to wake up power down/sleep
  - Interrupt or reset selectable on watchdog time-out
- **RTC**
  - Support time out interrupt
  - Support wake up function
- **PWM Timer**
  - One 16-bit timer and four 16-bit comparators
  - Five clock selectors
  - One 8-bit pre-scaler and one clock divider
  - Two Dead-Zone generators
  - Programmable duty control of output waveform
  - Auto reload mode or one-shot pulse mode
  - Capture function
- **SPI**
  - Two sets of SPI device
  - Master mode up to 24MHz (3.3V)
  - Support master/slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - 2 slave/device select lines

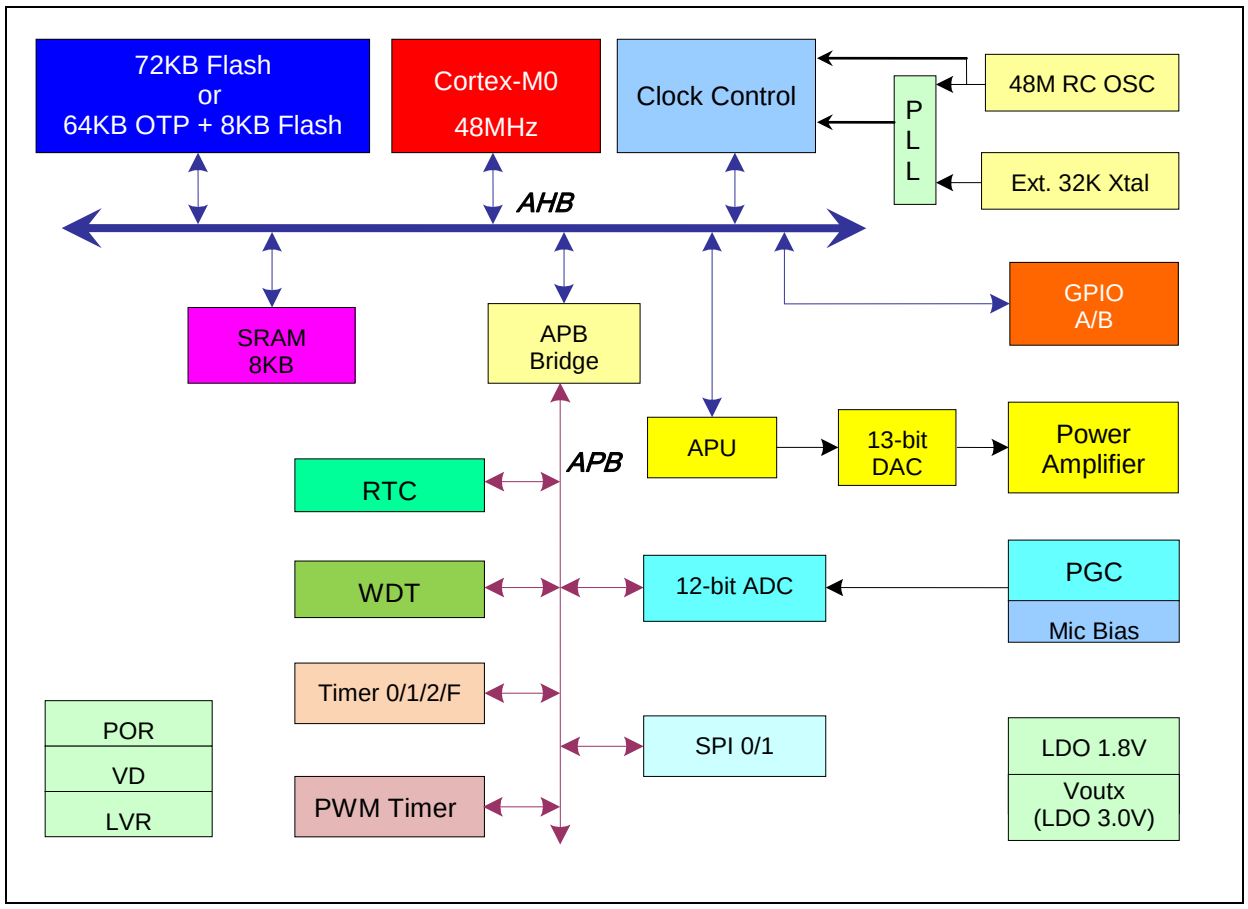
  - Two 32-bit buffers

- **ADC**
  - 8-ch 12-bit with 320Ksps
  - Single scan/single cycle scan/continuous scan
  - 8 channels share 8 result registers
  - Programmable channel scan sequence
  - Threshold voltage detection
  - Conversion start by S/W or an external pin
  - Programmable gain control for sound record
  - Internal microphone bias
- **APU**
  - 13-bit DAC
  - H/W mixer with 2 channel PCM inputs
  - Embedded power amplifier
  - 7-level volume control
- **Voltage Detector**
  - with 2 levels: 3.0V/2.7V
- **LDO**
  - Built-in 1.8V LDO
- **Voltage Output**
  - Built-in 3V regulator power supply Voutx for driving external spi-flash
- **Low Voltage Reset 1.8V**
- **Operating Temperature: 0℃~70℃**
- **Packages:**
  - All Green package (RoHS)
  - 7mmx7mm LQFP 64-pin or COB

# 3. Application Fields

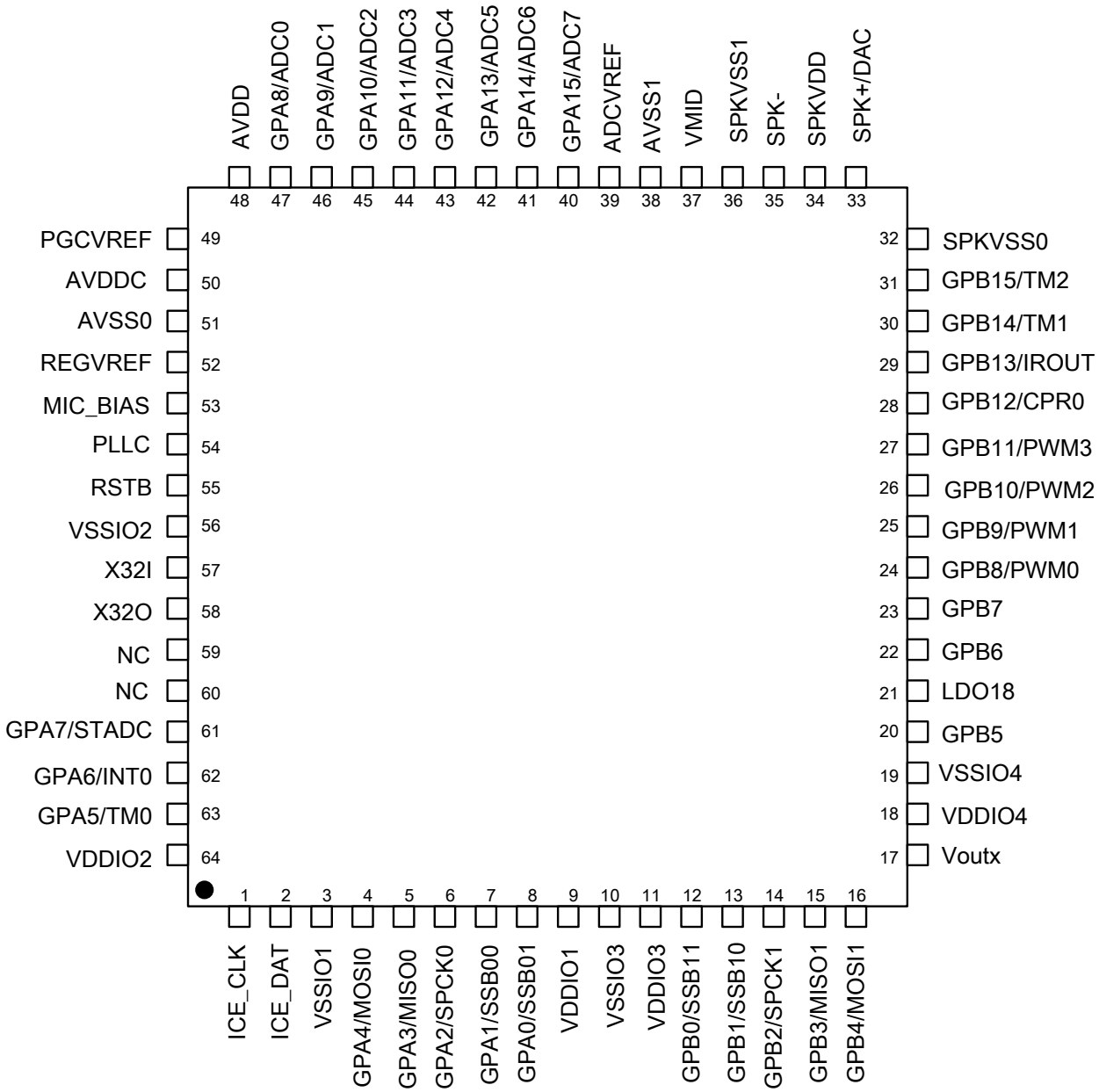
- **Recordable story books**
- **Karaoke musical player**
- **Toy masks with voice change**
- **Voice recognition toys**
- **Interactive toys on learning of music, languages**
- **Toy robots**

# 4. Functional Block Diagram



# 5. Pin Configuration

## 5.1 Pin Diagram



## 5.2 Pad Description

| Name | Type | Description |
|---|---|---|
| **1. GPIO** | | |
| GPA0 ~ GPA15 | I/O | Bidirectional general purpose I/O ports. Most of these pins have alternate function, refer to section 5.3 for detail. |
| GPB0 ~ GPB15 | I/O | Bidirectional general purpose I/O ports. Most of these pins have alternate function, refer to section 5.3 for detail. |
| **2. Oscillator** | | |
| X32I | I | 32KHz crystal input |
| X32O | O | 32KHz crystal output |
| PLLC | A | Capacitor connection for built-in PLL1 |
| **3. PGC and ADC** | | |
| AVDD | P | Analog power supply |
| AVSS0 | P | Analog ground |
| AVSS1 | P | Analog ground |
| ADCVREF | A | Reference voltage input for ADC |
| MIC_BIAS | A | Microphone bias output |
| AVDDC | A | Regulator output pin for ADC and PGC, its output voltage is 0.85xAVDD. Connect an external 4.7uF capacitor to AVSS. |
| PGCVREF | A | AVDDC/2 for PGC. A 4.7uF (or higher) capacitor for low pass filter to filter power noise is needed. |
| REGVREF | A | AVDD/2 for microphone output. A 4.7uF (or higher) capacitor for low pass filter to filter power noise is needed. |
| **4. Speaker Driver** | | |
| DAC/SPK+ | O | Speaker positive output pin, or current type DAC output. |
| SPK- | O | Speaker negative output pin. |
| SPKVDD | P | Analog power supply |
| SPKVSS1 | P | Analog ground. |
| SPKVSS0 | P | Analog ground. |
| VMID | A | Connect a capacitor to SPKVSS1 |
| **5. Power** | | |
| VDDIO4 | P | Power supply for I/O port, LVR, LVD and source of LDO. |

| | | |
|---|---|---|
| VSSIO4 | P | Ground pin, connect to 0V. |
| VDDIO2 | P | Power supply for I/O port, SWD, and RSTB |
| VSSIO2 | P | Ground pin, connect to 0V. |
| VDDIO1 | P | Power supply for I/O port. |
| VSSIO1 | P | Ground pin, connect to 0V. |
| VDDIO3 | P | Power supply for I/O port. |
| VSSIO3 | P | Ground pin, connect to 0V. |
| LDO18 | P | 1.8V LDO output |
| Voutx | P | 3.0V regulator output for driving external |
| **6. SWD** | | |
| ICE_CLK | I | Serial Wired Debugger Clock pin |
| ICE_DAT | I/O | Serial Wired Debugger Data pin |
| **7. Other** | | |
| RSTB | I | Reset input pin, low active. Internal pull-high. |

## 5.3 Alternate Function List of GPIO

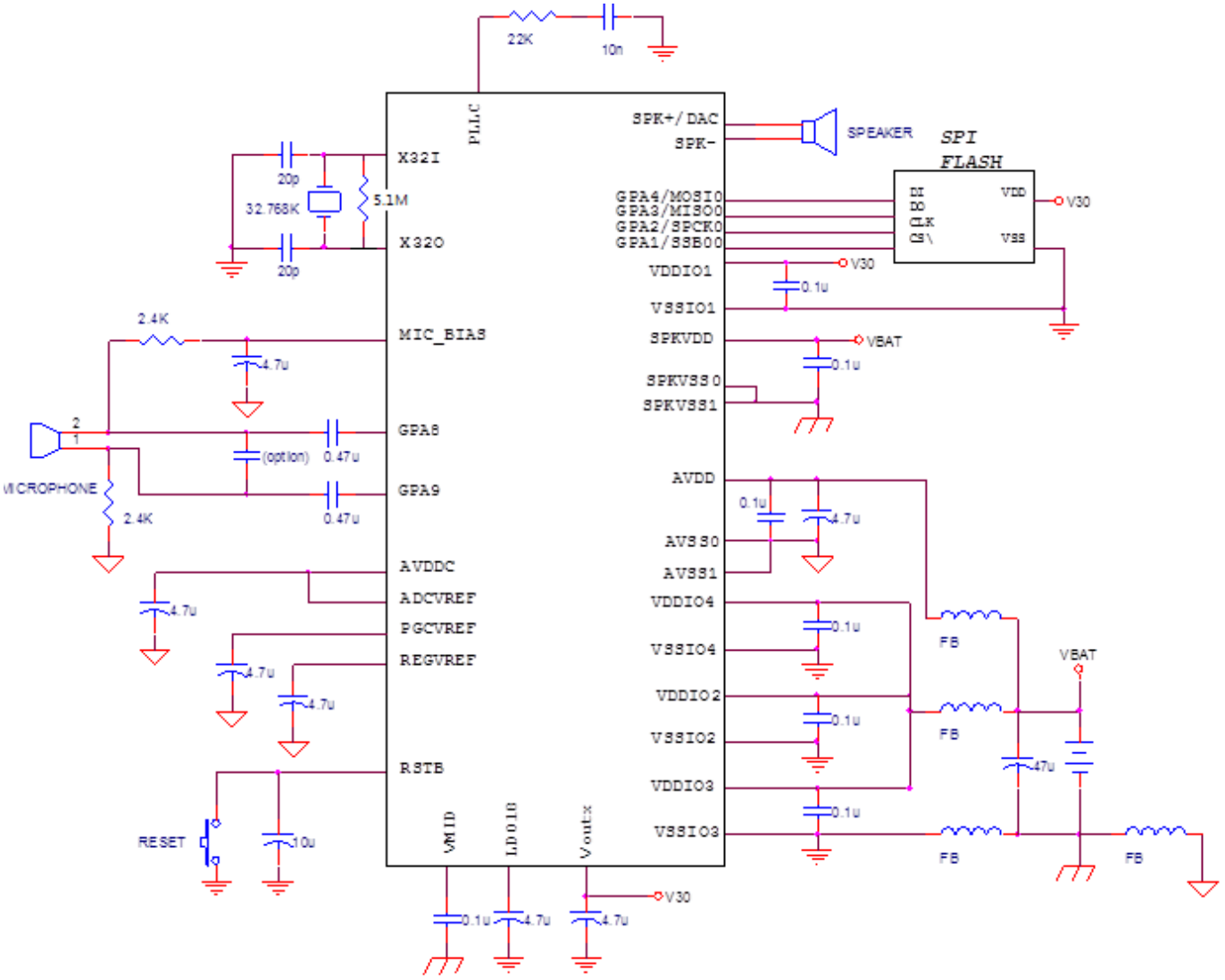
| GPIO | Power | Alternate | I/O of Alternate | Function Description |
|---|---|---|---|---|
| GPA0 | VDDIO1 | SSB01 | O | SPI0 2nd chip select pin |
| GPA1 | VDDIO1 | SSB00 | O | SPI0 1st chip select pin |
| GPA2 | VDDIO1 | SPCK0 | O | SPI0 serial clock output |
| GPA3 | VDDIO1 | MISO0 | I | SPI0 master data input |
| GPA4 | VDDIO1 | MOSI0 | O | SPI0 master data output |
| GPA5 | VDDIO2 | TM0 | I | Timer0 counter external clock input |
| GPA6 | VDDIO2 | INT0 | I | External interrupt input pin |
| GPA7 | VDDIO2 | STADC | I | ADC external trigger input |
| GPA8 | AVDD | ADC0 | A | ADC analog input 0 |
| GPA9 | AVDD | ADC1 | A | ADC analog input 1 |
| GPA10 | AVDD | ADC2 | A | ADC analog input 2 |
| GPA11 | AVDD | ADC3 | A | ADC analog input 3 |
| GPA12 | AVDD | ADC4 | A | ADC analog input 4 |
| GPA13 | AVDD | ADC5 | A | ADC analog input 5 |
| GPA14 | AVDD | ADC6 | A | ADC analog input 6 |
| GPA15 | AVDD | ADC7 | A | ADC analog input 7 |
| GPB0 | VDDIO3 | SSB11 | O | SPI1 2nd chip select output pin |
| GPB1 | VDDIO3 | SSB10 | I/O | SPI1 1st chip select output/input pin |
| GPB2 | VDDIO3 | SPCK1 | I/O | SPI1 serial clock output/input |
| GPB3 | VDDIO3 | MISO1 | I/O | SPI1 master data input, slave data output |
| GPB4 | VDDIO3 | MOSI1 | I/O | SPI1 master data output, slave data input |
| GPB5 | VDDIO4 | - | | |
| GPB6 | VDDIO4 | - | | |
| GPB7 | VDDIO4 | - | | |
| GPB8 | VDDIO4 | PWM0 | O | PWM output pin 0 |
| GPB9 | VDDIO4 | PWM1 | O | PWM output pin 1 |

| | | | | |
|---|---|---|---|---|
| GPB10 | VDDIO4 | PWM2 | O | PWM output pin 2 |
| GPB11 | VDDIO4 | PWM3 | O | PWM output pin 3 |
| GPB12 | VDDIO4 | CPR0 | I | Capture input |
| GPB13 | VDDIO4 | IROUT | O | IR carrier output |
| GPB14 | VDDIO4 | TM1 | I | Timer1 counter external clock input |
| GPB15 | VDDIO4 | TM2 | I | Timer2 counter external clock input |

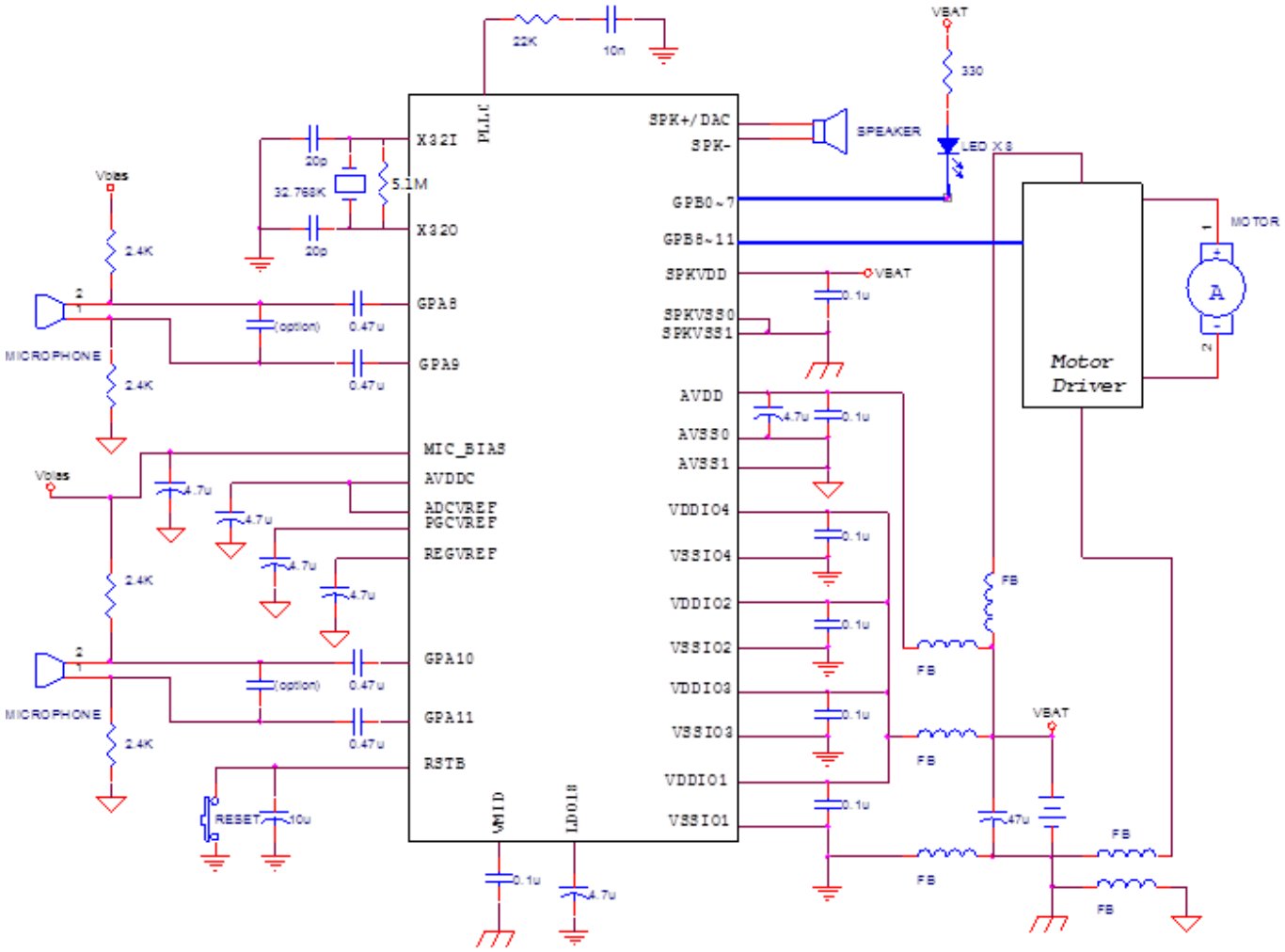
I: Input, O: Output, A: Analog input

# 6. Typical Application Circuit

## 6.1 Recording and Playback



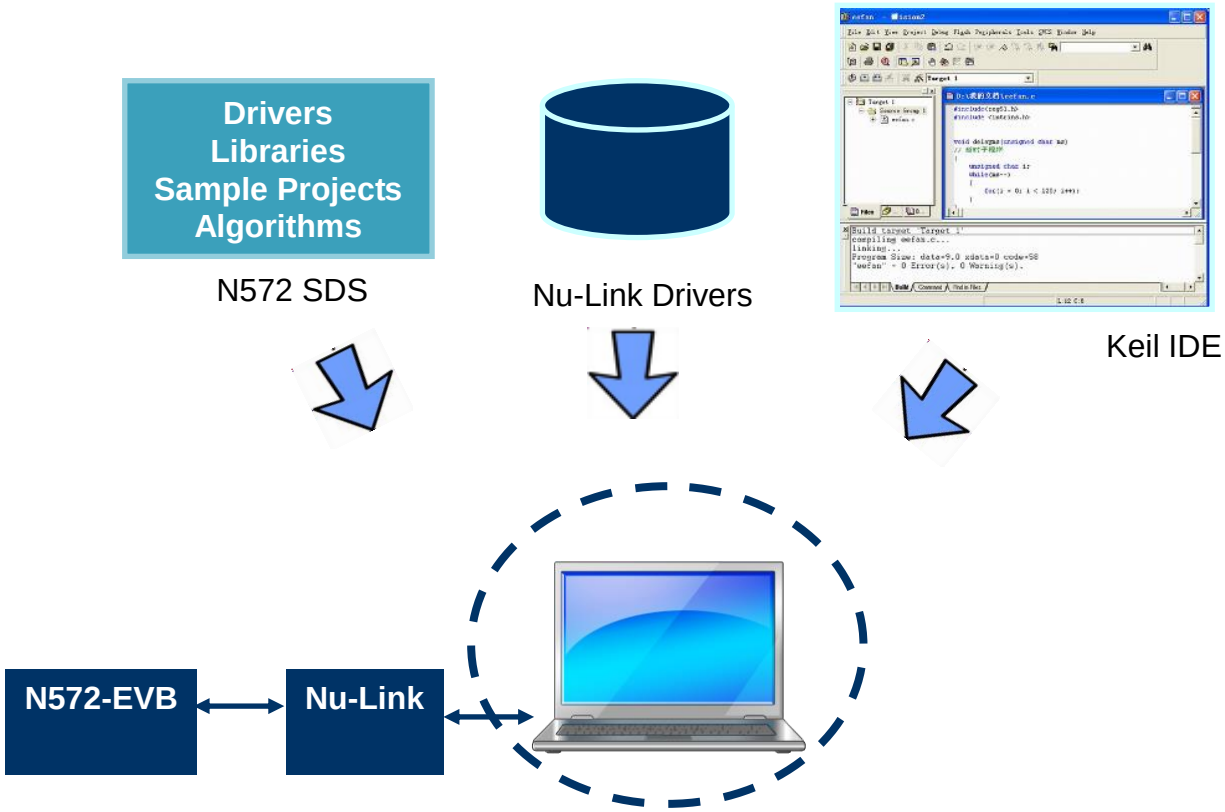
## 6.2 Dual Microphones for Sound Direction Detection and Motor Control



# 7. Software and Development Environment

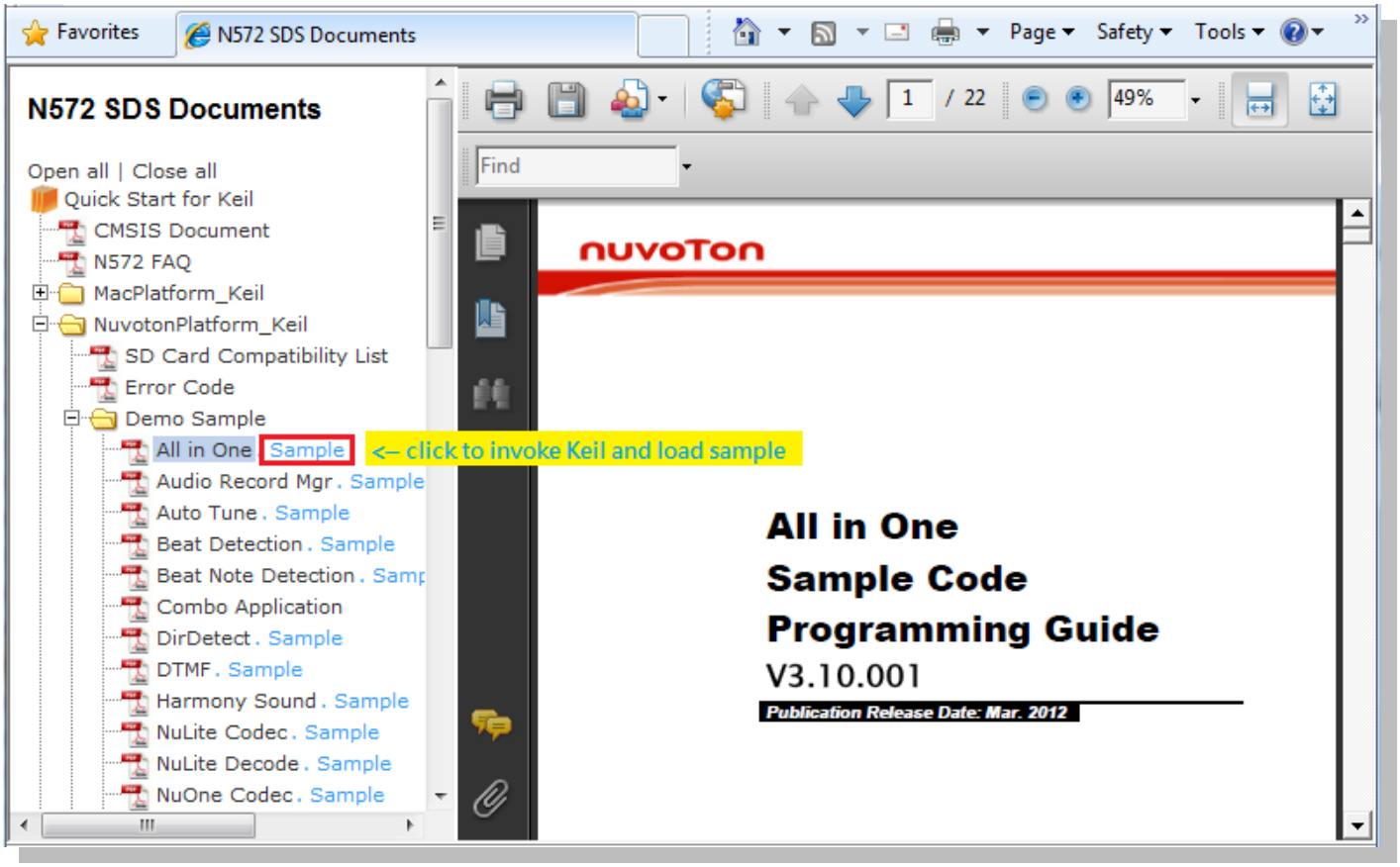
## 7.1 Development Environment

The Keil™ MDK includes IDE, compiler, linker, and debugger is for your software development. Debug hardware requires Nu-Link™ and N572 EVB. A Nu-Link driver is required to add views of peripherals and add-ons within MDK's IDE. With software library, you can develop and debug in the MDK environment. Please refer to Programming Guide for details.



## 7.2 Library and Document Guide

N572 SDS is for N572F072/P072/F065 which provides a bunch of sample codes, libraries, document, and EVB schematic for your reference. To get familiar with the whole development environment, please install Keil then this SDS. There will be a **N572 SDS Document Index** under **N572 SDS Vxxx** from Start menu to show all the useful information. Even better is the links to directly open Keil and load sample projects in a click!




The algorithms are collected in library. **Demo Sample** is also a good place for user to understand the capability of NuVoice™.

## 7.3 Supported Codec

Following table shows the supported codec and suggested sample rate and corresponding bit rate. The Bit Rate of NuOne, NuLite, and NuSound could be configurable. For example, using 8K sample rate, the bit rate could be 8Kbps (1bit per sample) or 12Kbps (1.5 bit per sample) or 16Kbps (2 bit per sample). Details please refer to document in SDS.

| Codec | Sample Rate (Hz) *note1 | Bit Rate (bps) | For | Availability |
|---|---|---|---|---|
| NuOne | 8K~20K | 8K ~ 20K @1b/sample *note2 | Speech, Music | Codec |
| NuLite | 8K~12K | 9.6K ~ 14.4K @1.2b/sample *note2 | Speech, Music | Codec |
| NuSound | 8K~20K | 16K~40K @2b/sample *note3 | Speech, Music | Decoder |
| MD4 | 8K~20K | 32K~80K | Speech, Music | Decoder |
| IMAADPCM | 8K~20K | 32K~80K | Speech, Music | Codec |
| LP8 | 8K~20K | 64K~160K | Speech, Music | Codec |
| NuVox24 | 8K | 2.4K | Speech | Decoder |
| NuVox53/63 | 8K | 5.3K/6.3K | Speech | Decoder |

*note1: suggested sampling rate

*note2: bits per sample range from 0.5b/sample ~ 3b/sample, with 0.1b/sample incremental step

*note3: bits per sample range from 1.5b/sample ~ 3b/sample, with 0.1b/sample incremental step

# 8. Electrical Characteristics

## 8.1 Absolute Maximum Ratings

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| DC Power Supply | VDD–VSS | -0.3 | +7.0 | V |
| Input Voltage | VIN | VSS-0.3 | VDD+0.3 | V |
| Oscillator Frequency | $1/t_{CLCL}$ | 0 | 48 | MHz |
| Operating Temperature | TA | 0 | +70 | °C |
| Storage Temperature | TST | -55 | +150 | °C |
| Maximum Current into $V_{DD}$ | | - | 120 | mA |
| Maximum Current out of $V_{SS}$ | | | 120 | mA |
| Maximum Current sunk by an I/O pin | | | 35 | mA |
| Maximum Current sourced by an I/O pin | | | 35 | mA |
| Maximum Current sunk by total I/O pins | | | 100 | mA |
| Maximum Current sourced by total I/O pins | | | 100 | mA |

## 8.2 DC Electrical Characteristics

VDD-VSS=4.5V, TA=25°C, unless otherwise specified.

| PARAMETER | SYM | SPECIFICATION | | | | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| Operation voltage | $V_{DD}$ | 2.4 | | 5.5 | V | |
| Power Ground | $V_{SS}$ $AV_{SS}$ | -0.3 | | | V | |
| Analog Operating Voltage | $AV_{DD}$ | 0 | | $V_{DD}$ | V | |
| Analog Reference Voltage | Vref | 0 | | $AV_{DD}$ | V | |
| Operating Current at Normal Run Mode | $I_{DD1}$ | | 20 | | mA | $V_{DD}$=5.5V@48MHz, enable all IPs' clock |
| | $I_{DD3}$ | | 18 | | mA | $V_{DD}$=3V@48MHz, enable all IPs' clock |
| Operating Current at Idle Mode | $I_{IDLE2}$ | | 3 | | mA | $V_{DD}$=5.5V@48MHz, disable all IPs |
| | $I_{IDLE4}$ | | 3 | | mA | $V_{DD}$=3V@48MHz, disable all IPs |
| Operating Current at Power-down Mode | $I_{PWD1}$ | | 10 | 15 | μA | $V_{DD}$ = 5.5V, No load, disable Voutx, LVD, LVR, … |
| | $I_{PWD2}$ | | 9 | 15 | μA | $V_{DD}$ = 3.3V, No load, disable Voutx, |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | | | LVD, LVR, … |
| Input Current GPA/GPB | $I_{IN1}$ | -60 | - | +15 | μA | $V_{DD}$ = 5.5V, $V_{IN}$ = 0V or $V_{IN}$=$V_{DD}$ |
| Input Current at RSTB [1] | $I_{IN2}$ | -160 | -130 | -100 | μA | $V_{DD}$ = 5.5V, $V_{IN}$ = 0.45V |
| Input Leakage Current GPA/GPB | $I_{LK}$ | -0.1 | - | +0.1 | μA | $V_{DD}$ = 5.5V, 0<$V_{IN}$<$V_{DD}$ |
| Input Low Voltage GPIO (TTL input) | $V_{IL1}$ | -0.3 | - | 1.0 | V | $V_{DD}$ = 4.5V |
| | | -0.3 | - | 0.6 | | $V_{DD}$ = 2.4V |
| Input High Voltage GPIO (TTL input) | $V_{IH1}$ | 2.2 | - | $V_{DD}$ +0.2 | V | $V_{DD}$ = 5.5V |
| | | 1.5 | - | $V_{DD}$ +0.2 | | $V_{DD}$ = 3.0V |
| Source Current GPA/GPB (Quasi-bidirectional Mode) | $I_{SR11}$ | -300 | -370 | -450 | μA | $V_{DD}$ = 4.5V, $V_S$ = 2.4V |
| | $I_{SR12}$ | -50 | -70 | -90 | | $V_{DD}$ = 2.7V, $V_S$ = 2.2V |
| | $I_{SR13}$ | -40 | -60 | -80 | | $V_{DD}$ = 2.5V, $V_S$ = 2.0V |
| Source Current GPA/GPB (Push-pull Mode) | $I_{SR21}$ | -20 | -24 | -28 | mA | $V_{DD}$ = 4.5V, $V_S$ = 3.0V |
| | $I_{SR22}$ | -4 | -6 | -8 | | $V_{DD}$ = 2.7V, $V_S$ = 2.2V |
| | $I_{SR23}$ | -3 | -5 | -7 | | $V_{DD}$ = 2.5V, $V_S$ = 2.0V |
| Sink Current GPA/GPB (Quasi-bidirectional and Push-pull Mode) | $I_{SK1}$ | 10 | 16 | 20 | mA | $V_{DD}$ = 4.5V, $V_S$ = 0.45V |
| | $I_{SK2}$ | 7 | 10 | 13 | | $V_{DD}$ = 2.7V, $V_S$ = 0.45V |
| | $I_{SK3}$ | 6 | 9 | 12 | | $V_{DD}$ = 2.5V, $V_S$ = 0.45V |

**Notes:** 1. RSTB pin is a Schmitt trigger input.

## 8.3 AC Electrical Characteristics

The following data are measured under VDD-VSS=4.5V, TA=25°C, unless otherwise specified.

### 8.3.1 Internal 48MHz RC Oscillator

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Center Frequency | | | 48.24 | | MHz |
| Calibrated Internal Oscillator Frequency | +25°C | -1 | | +1 | % |
| Operating current | $V_{DD}$=1.8V | | 900 | | uA |

## 8.4 Analog Characteristics

The following data are measured under VDD-VSS=4.5V, TA=25°C, unless otherwise specified.

### 8.4.1 12-bit SAR ADC

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Resolution | - | - | - | 12 | Bit |
| Differential nonlinearity error | DNL | - | ±1 | - | LSB |
| Integral nonlinearity error | INL | - | ±1 | - | LSB |
| Offset error | EO | - | ±1 | - | LSB |
| Gain error (Transfer gain) | EG | - | 1 | - | - |
| Monotonic | - | Guaranteed | | | - |
| ADC clock frequency | FADC | - | - | 8 | MHz |
| Sample & Conversion time | TADC | - | 25 | - | Clock |
| Sample rate | FS | - | - | 320 | Ksps |
| Supply voltage | VDD | - | 1.8 | - | V |
| | VDDA | 3 | - | 5.5 | V |
| Supply current (Avg.) | IDD | - | 0.5 | - | mA |
| | $I_{DDA}$ | - | 1.5 | - | mA |
| Reference voltage | VREFP | - | VDDA | - | V |

### 8.4.2 Voice Recorder

| Parameter | Sym. | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operation Voltage | VDDA | | 3 | 5 | 5.5 | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| Operation Current | IDD | | | 3.5 | | mA |
| Programmable Gain | PG | | 0 | | 30 | dB |
| Preamp Gain | PAG | | 20 | | 40 | dB |
| Offset Bit | OS | 9-bit Control | -64 | | 64 | mV |
| THD+N | THD+N | Preamp Gain=40dB, Programmable Gain=0dB | | -55 | | dB |

### 8.4.3 1.8V LDO for Internal Core

| Parameter | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| Input Voltage | | 2.4 | 5 | 5.5 | V |
| Output Voltage | | -- | 1.8 | -- | V |

### 8.4.4 Voutx (3.0V LDO) for External Driving

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input Voltage | | 3.3 | 5 | 5.5 | V |
| Output Voltage | | -10% | 3.0 | +10% | V |
| | Turn off | | floating | - | V |
| $I_{load}$ | | | | 40 | mA |

### 8.4.5 Low Voltage Reset

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Threshold voltage | Temperature=25°C | 1.6 | 1.8 | 2.0 | V |

### 8.4.6 Voltage Detector

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Detected Voltage | CVDTV=0 | | 2.7 | | V |
| | CVDTV=1 | | 3.0 | | V |

### 8.4.7 Power Amplifier and DAC

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Operation voltage | SPKVDD | 2.4 | 4.5 | 5.5 | V |
| Output Power | SPKVDD=4.5V, 8Ω BTL load, 0dB gain | | 400 | | mW |

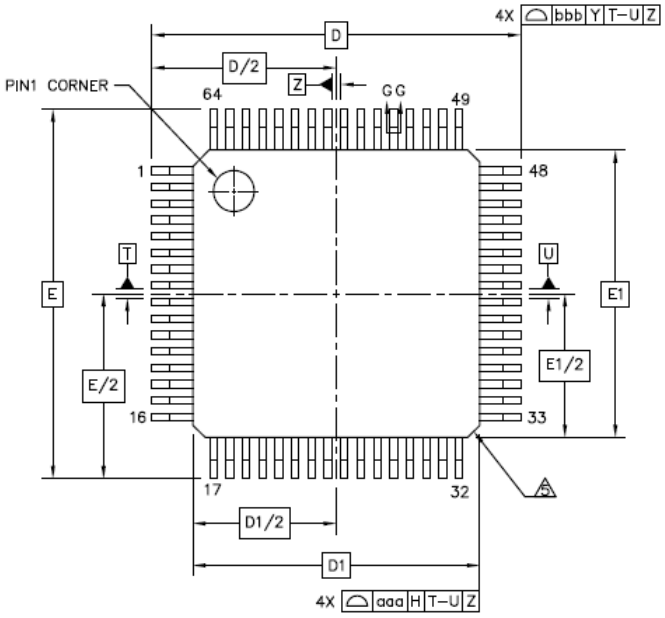
| | | | | | |
|---|---|---|---|---|---|
| Total Harmonic Distortion | SPKVDD=4.5V, 8Ω BTL load, 0dB gain, 400mW | | -48 | | dB |
| Power Amplifier Gain | | -18 | | 0 | dB |
| DAC output current | DACGN=0 | 2.4 | 3 | 3.6 | mA |
| | DACGN=1 | 4.0 | 5.0 | 6.0 | |
| DAC operation Current | SPKVDD=4.5V | | 4 | | mA |
| DAC Quiescent Current | SPKVDD=4.5V | | 200 | | μA |
| Power Amplifier Quiescent Current | DAC fine-tuned, SPKVDD=4.5V | | 6 | | mA |
| Power Down Current | DAC fine-tuned, SPKVDD=4.5V | | 1 | | μA |
| Operation Current | SPKVDD=4.5V, 400mW | | 250 | | mA |

### 8.4.8 PLL

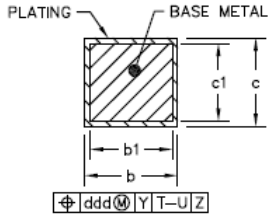
| PARAMETER | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Operating Voltage Range | VDD | | -- | 1.8 | -- | V |
| Temperature | | | 0 | 25 | 70 | °C |
| Input Clock Frequency | Fin | | -- | 32.768 | -- | KHz |
| Output Clock Frequency | Fout | | -- | 48 | -- | MHz |
| Duty Cycle | -- | Fout=48MHz | 40 | 50 | 60 | % |
| Operating Current | Iop | 25°C | | 3 | | mA |

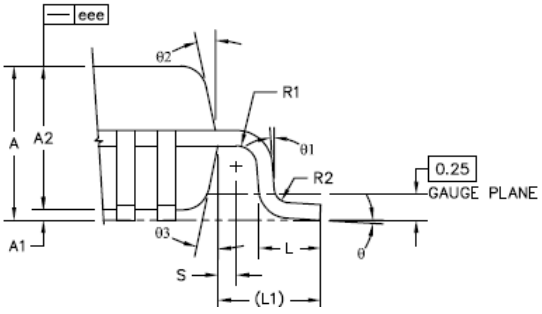
# 9. Package Information

64L LQFP(7x7x1.4mm footprint 2.0mm)




| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | --- | --- | 1.6 |
| STAND OFF | | A1 | 0.05 | --- | 0.15 |
| MOLD THICKNESS | | A2 | 1.35 | 1.4 | 1.45 |
| LEAD WIDTH(PLATING) | | b | 0.13 | 0.18 | 0.23 |
| LEAD WIDTH | | b1 | 0.13 | 0.16 | 0.19 |
| L/F THICKNESS(PLATING) | | c | 0.09 | --- | 0.2 |
| L/F THICKNESS | | c1 | 0.09 | --- | 0.16 |
| BODY SIZE | X | D | 9 BSC | | |
| | Y | E | 9 BSC | | |
| | X | D1 | 7 BSC | | |
| | Y | E1 | 7 BSC | | |
| LEAD PITCH | | e | 0.4 BSC | | |
| | | L | 0.45 | 0.6 | 0.75 |
| FOOTPRINT | | L1 | 1 REF | | |
| | | θ | 0° | 3.5° | 7° |
| | | θ1 | 0° | --- | --- |
| | | θ2 | 11° | 12° | 13° |
| | | θ3 | 11° | 12° | 13° |
| | | R1 | 0.08 | --- | --- |
| | | R2 | 0.08 | --- | 0.2 |
| | | S | 0.2 | --- | --- |
| PACKAGE EDGE TOLERANCE | | aaa | 0.2 | | |
| LEAD EDGE TOLERANCE | | bbb | 0.2 | | |
| COPLANARITY | | ccc | 0.08 | | |
| LEAD OFFSET | | ddd | 0.07 | | |
| MOLD FLATNESS | | eee | 0.05 | | |



# 10. Ordering Information

| PART NUMBER | PACKAGE | SPECIAL FEATURE | PB FREE + HALOGEN FREE (GREEN) | RELEASE DATE |
|---|---|---|---|---|
| N572F072 | NA (Die Form) | MTP | Yes | Available |
| N572F072G | LQFP 64pin 7mmx7mm | MTP | Yes | Available |
| N572P072 | NA (Die Form) | OTP + MTP | Yes | Available |
| N572P072G | LQFP 64pin 7mmx7mm | OTP + MTP | Yes | Available |

# 11. Revision History

| VERSION | DATE | DESCRIPTIONS |
|---|---|---|
| 1.0 | Oct, 2011 | Preliminary draft |
| 1.1 | May, 2012 | Review to make official release |
| 1.2 | Nov, 2012 | Add codec table<br>Add section of Application Fields<br>Keep only 64KB OTP+ 8KB Flash for N572P072 |
| 1.3 | Aug, 2013 | Update Operating Temperature as 0℃~70℃<br>Update application circuit<br>Remove supply voltage VDD & un-calibrated part in 8.3.1 table<br>Update minimum input spec of SPKVDD & 1.8V LDO to 2.4V. |
| 1.4 | Aug, 2014 | Update Internal RC 48MHz Center Frequency as 48.24MHz (typical)<br>Update Calibrated Internal Oscillator Frequency as ±1%<br>Correct Voice Recorder THD+N as -55dB (typical) |

## Important Notice

**Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".**

**Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.**

**All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.**