ARM® Cortex®-M4

32-bit Microcontroller

NuMicro® Family
NUC442 Series
Datasheet

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1 GENERAL DESCRIPTION

1.1 NuMicro™ NUC442 General Description

The NuMicro™ NUC442 Connectivity series with embedded Cortex®-M4F core with DSP extensions and a Floating Point Unit runs up to 84 MHz with 256/512 Kbytes embedded flash memories and 64K-byte embedded SRAM. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timers, RTC, PDMA, EBI, UART, Smart Card interface, SD HOST, SPI, I^2C, I^2S, PWM Timer, GPIO, LIN, CAN, PS/2, 12-bit ADC, analog comparator, operational amplifier, temperature sensor, Low Voltage Reset Controller and Brown-out Detector. The NUC442 also provides USB 2.0 full-speed Device/Host/OTG, USB 2.0 HS device and security functions such as tamper detection, symmetric cryptographic accelerator and secure Hash function accelerator.

Product Series	Ethernet	USB	CAN	SD Host	UART	SPI	I^2C	Smart Card Interface	Security	ADC
NUC442		•	•	•	•	•	•	•	•	•

Table 1.1-1 Key Features Support Table

The NuMicro™ NUC442 series is suitable for a wide range of applications such as:

- Industrial Automation
- PLCs
- Inverters
- Home Automation
- Security Alarm System
- Power Metering
- Portable Data Collector
- Portable RFID Reader
- System Supervisors
- USB Accessories
- Smart Card Reader
- Printer
- POS
- Motor Control

2 FEATURES

2.1 NuMicro™ NUC442 Features – Connectivity Series

- Core
  - ARM® Cortex®-M4 core running up to 84 MHz
  - Supports DSP extension
    - Supports hardware divider
  - Supports IEEE 754 compliant Floating-point Unit (FPU)
  - Supports Memory Protection Unit (MPU)
  - One 24-bit system timer
  - Supports low power sleep mode
    - Supports both WFI and WFE instructions
  - Single-cycle 32-bit hardware multiplier
  - Supports Nested Vectored Interrupt Controller (NVIC)
    - Supports programmable 256 level priorities for interrupts
  - Supports programmable maskable interrupts
- Build-in LDO for wide operating voltage ranged from 2.5 V to 5.5 V
- Flash Memory
  - 256/512 Kbytes Flash memory
  - Configurable program code/data allocation
  - ISP loader sizes 16 Kbytes
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports In-system program (ISP), In application program (IAP) update
  - 2 Kbytes page erase for flash
  - Supports fast parallel programming mode by external programmer
- SRAM
  - 64 Kbytes embedded SRAM
  - 24 Kbytes SRAM with hardware parity check
  - Supports byte-, half-word- and word-access parity check
  - Supports exception (NMI) generated once a parity check error occurs
  - Supports PDMA mode
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed RC oscillator for system operation (variation < 2% at -40℃ ~ +105℃)
  - Built-in 10 kHz low speed RC oscillator for Watchdog Timer and Wake-up operation
  - Built-in 4~24 MHz high speed oscillator for external crystal input for precise timing operation
  - Built-in 32.768 kHz low speed oscillator for external crystal input for RTC function and low power system operation
  - Supports one PLL, up to 84 MHz for high performance system operation, sourced from
    - Built-in 22.1184 MHz high speed RC oscillator
    - 4~24 MHz external high speed crystal oscillator
  - Supports clock failure detection for system clock
  - Supports exception (NMI) generated once a clock failure detected
  - Flexible selection for different applications
  - Supports clock out
  - CPU clock source can be selected from USB PHY Embedded PLL
- EBI
  - Supports accessible space up to 256MB configured into 4 memory blocks (64MB/Memory Block), the actually external addressable space is dependent on

package pin out
- Dedicated external chip select pin for each memory block
- Supports 8-/16-bit data width
- Supports byte write in 16-bit data width mode
- Supports PDMA mode
- Supports Address/Data Separated/Multiplexed Mode
- Supports Timing parameters individual adjustment for each memory block
- Supports "Timing Transparent Encrypt/Decrypt" for protecting data in each memory block (Individual Enable/Disable)

● GPIO

- Four I/O modes:
  - Quasi-bidirectional
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable
- I/O pin configured as interrupt source with edge/level trigger setting
- High driver and high sink IO mode support (To source 20mA and sink 15mA at 5V)
- Supports up to 114/101/77/45 GPIOs for LQFP144/128/100/64, respectively.

● PDMA (Peripheral DMA)

- Supports 16 independent configurable channels for automatic data transfer between memories and peripherals
- Supports normal and Scatter-Gather Transfer modes
- Supports 2 types of priorities modes: fixed-priority and round-robin modes
- Supports byte-, half-word- and word-access
- Auto increment the source and destination address
- Supports 16-level FIFO
- Supports bus abort status flag

● Timer

- Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Supports event counting function to count the event from external pin
- Supports input capture function to capture or reset counter value

● PWM

- Supports up to two 6-channel PWM outputs with 16-bit resolution
- Supports 8-bit presale and clock divider
- Supports period point, center point and edge point PWM Interrupt
- Supports One-shot or Auto-reload PWM counter operation mode
- Supports Edge-aligned or Center-aligned PWM counter type
- Supports 8-bit dead zone with maximum divided 8 pre-scale
- Supports brake function source from pin or comparator output
- Supports mask function for each PWM pin
- Supports independent, complementary, synchronized and group PWM output mode
- Supports trigger ADC start conversion at PWM counter period point, PWM counter center point, PWM output rising edge and PWM output falling edge
- Supports 12 Capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports capture interrupt

● EPWM (Enhanced PWM)

- Supports up to two EPWM
- Each EPWM has

- Three independent 16-bit PWM duty control units with maximum 6 port pins
- Group control bit: PWM2 and PWM4 are synchronized with PWM0
- Supports Edge-aligned mode and Center-aligned mode
- Programmable dead-time insertion between complementary paired PWMs
- Each pin of from PWM0 to PWM5 has independent polarity setting control
- Mask output control for Electrically Commutated Motor operation
- Tri-state output at reset and brake state
- Hardware brake protections
- Two Interrupt Sources
- PWM signals before polarity control stage are defined in view of positive logic. The PWM ports active high or active low are controlled by polarity control register.
- High Source/Sink current

- Enhanced Input Capture Timer
  - Supports up to two Input Capture Timer/Counter Units, Input Capture 0 and Input Capture 1
  - Each unit has own interrupt vector
  - 24-bit Input Capture up-counting timer/counter
  - With noise filter in front end of input ports
  - Edge detector with three options
    - Rising edge detection
    - Falling edge detection
    - Both edge detection
  - Each input channel is supported with one capture counter hold register
  - Captured event reset/reload capture counter option
  - Supports compare-match function
- Quadrature Encoder Interface (QEI)
  - Supports up to two QEI controllers, QEI0 and QEI1
  - Each QEI has
    - Two QEI phase inputs, QEA and QEB; One Index input
    - One QEI control register (QEI_CTR) and one QEI Status Register (QEI_STS)
    - Four Quadrature encoder pulse counter operation modes
- Watchdog Timer
  - Supports multiple clock sources
  - 8 selectable time out period from 1.6ms ~ 26.0sec (depending on clock source)
  - Able to wake up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
- Window Watchdog Timer
  - Supports multiple clock sources
  - Window set by 6-bit counter with 11-bit pre-scale
  - Interrupt or reset selectable on time-out
- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Supports wake-up function
  - Supports 96 bytes backup registers
  - Programmable backup-register erase function

- Supports external power input pin (V_{BAT})
- Supports tamper detection function

- Tamper Detection
  - Supports external tamper detection up to 2 input pins
  - Reset, NMI or Interrupt generated once tamper detected
- UART
  - Supports up to six UART controllers
  - Supports flow control (CTS and RTS)
  - UART0 with 64-byte FIFO is for high speed
  - UART1~5 with 16-byte FIFO for standard device
  - Supports IrDA (SIR) and LIN function
  - Supports RS-485 9-bit mode and direction control
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports PDMA mode
- Smart Card Interface
  - Supports up to six ISO-7816-3 ports
  - Compliant to ISO-7816-3 T=0, T=1
  - Separate receive / transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 267 ETU)
  - A 24-bit and two 8 bit time out counter for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation/deactivation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware auto deactivation sequence when detect the card is removal
  - Supports UART function
- PS/2 Device Controller
  - Host communication inhibit and request to send detection
  - Reception frame error detection
  - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
  - Double buffer for data reception
  - S/W override bus
- I^2C
  - Supports up to five sets of I^2C device
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allowing versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports speed up to 1Mbps
  - Supports PDMA mode
  - Supports multi-address wake-up function
- SPI

- Up to four sets of SPI controllers
- Supports Master or Slave mode operation
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode
- Configurable bit length of a transfer word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports byte reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface
- Master up to 32 MHz, and Slave up to 16 MHz (chip working at 5V)

● I^2S

- Supports up to two I^2S interface
- Interface with external audio CODEC
- Supports Master and Slave mode
- Capable of handling 8-, 16-, 24- and 32-bit word sizes
- Supports mono and stereo audio data
- Supports I^2S and MSB justified data format
- Each provides two 8-word FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Each supports two PDMA requests, one for transmitting and the other for receiving

● USB 2.0 Controller

- Supports one set of USB 2.0 FS Device/Host/OTG or USB 2.0 HS Device
- Supports one set of USB 2.0 FS Host
- FS Host compatible with Open HCI 1.0 specification
- Compliant to USB specification version 2.0
- OTG supports USB OTG Supplement 1.3
- On-chip USB Transceiver
- Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
- Auto suspend function when no bus signaling for 3 ms
- Provides 12 programmable endpoints and one dedicated control end point
- Supports 4095 bytes internal SRAM as USB buffer
- Provides remote wake-up capability
- On-chip 5V to 3.3V LDO for USB PHY
- On-chip PLL able to support 480 MHz clock
- Supports DMA master

● CAN 2.0

- Supports up to two CAN controllers
- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1M bit/s
- Each supports 32 Message Objects
- Each Message Object has its own identifier mask
- Programmable FIFO mode (concatenation of Message Object)
- Supports interrupts
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications
- Supports power-down wake-up function

● SD Host Interface

- Supports SD (Secure Digital) card and SD HOST interface
- Compliant with SD Memory Card Specification Version 2.0
- Supports 1 and 4-bit modes
- Supports 25 MHz to achieve 100 Mbps at 3.3V operation

- Supports DMA master

- Cryptographic Accelerator
  - DES/TDES accelerator
    - Supports hardware DES (Data Encryption Standard)/TDES (Triple DES) accelerator
    - Supports 56, 112 and 168-bit keys
    - Supports ECB, CBC, CFB, OFB and CTR modes
    - Compliant with NIST 800 38A
  - AES accelerator
    - Supports hardware AES (Advanced Encryption Standard) accelerator
    - Supports 128-, 192- and 256-bit keys
    - Supports ECB, CBC, CFB, OFB and CTR modes
    - Compliant with NIST 800 38A
  - Secure Hash Function accelerator
    - Supports hardware SHA (Secure Hash) accelerator
    - Supports SHA-1 and SHA-224, -256
    - Compliant with FIPS 180-2

- Random Number Generator
  - Supports random bit generator
  - Supports a random number generator programmable 64, 128, 192 and 256 bits

- Image Capture Interface
  - CCIR601 & CCIR656 interfaces supported for connection to CMOS image sensor
  - Resolution up to 3M pixel
  - YUV422 and RGB565 color format supported for data-in from CMOS sensor
  - YUV422, RGB565, RGB555 and Y-only color format supported for data storing to system memory
  - Planar and packet data format supported for data storing to system memory
  - Image cropping supported with the cropping window up to 4096x2048
  - Image scaling-down supported
  - Vertical and horizontal scaling-down for preview mode supported
  - Scaling factor as N/M
  - Two pairs of configurable 8-bit N and 8-bit M for vertical and horizontal scaling-down
  - The value of N has to be equal to or less than M
  - Frame rate control supported
  - Combines two interlace fields to a single frame supported for data in from TV-decoder

- Cyclic Redundancy Calculation Unit
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - Programmable initial value
  - Supports programmable order reverse setting for input data and CRC checksum
  - Supports programmable 1's complement setting for input data and CRC checksum
  - Supports 8/16/32-bit of data width
  - Interrupt generated once checksum error occurs

- ADC
  - Supports two operating modes: ADC mode and EADC (Enhance ADC mode with dual ADC Sampling)
  - Selected as ADC mode
    - Supports single 12-bit ADC conversion
    - Analog input voltage range: 0~AV_{DD}
    - Up to 12 external single-ended analog input channels
    - Up to 6 differential analog input pairs
    - Supports single ADC interrupt
    - Supports easy control for power saving

    - External V_{REF} pin can be used as input
    - Supports PDMA transfer
  - Selected as EADC mode
    - Supports two 12-bit ADC simultaneous conversion
    - Analog input voltage range: 0~ AV_{DD}
    - Up to 16 external single-ended analog input channels
    - Each ADC can convert individually at normal operation
    - Four ADC interrupts with individual interrupt vector addresses
    - An A/D conversion source can be triggered by different events
    - Conversion results are held in 16 data registers with valid and overrun indicators
    - Sampling-oriented trigger setting and input setting for each sampling
    - Supports converting internal OP0, OP1 Amplifier output voltage
    - Supports converting internal band-gap voltage, internal temperature sensor output and analog ground
- Analog Comparator
  - Supports up to three rail-to-rail analog comparators
  - External input or internal Band-gap voltage selectable at negative node
  - Interrupts generated when compare results change
  - Supports power-down wake-up
- Operational Amplifier
  - Supports up to two analog operational amplifiers
  - Outputs can be used as the input of ADC
- Debug
  - Supports Flash Patch and Breakpoint Unit (FPB)
    - Supports 8 hardware breakpoints
    - Supports 6 watchpoints
  - Supports the following debug ports
    - 2-pin Serial Wire Debug port (SWD)
- Supports 96-bit Unique ID (UID)
- Supports 128-bit Unique Customer ID (UCID)
- One built-in temperature sensor with 1℃ resolution
- Brown-out Detector
  - With 4 levels: 4.4 V/ 3.7 V/ 2.7 V/ 2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 2.0 V
- Operating Temperature: -40℃~105℃
- Packages
  - All Green package (RoHS)
  - LQFP 144-pin/ 128-pin/ 100-pin/ 64-pin

3 ABBREVIATIONS

3.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SD	Secure Digital

SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3.1-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro™ NUC442 Connectivity Series Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP Loader ROM (KB)	I/O	Timer	Connectivity								Ethernet	PWM	Comp	OP	ADC (12-Bit)	RTC	ISO-7816-3*	ISP/ICP/IAP	Package
						UART	SPI	I^2C	USB	LIN	CAN	SC	I^2S									
NUC442JI8AE	512	64	16	114	4	6+6	4	5	v	6	2	6	2	--	16	3	2	x2, 16-ch	v	6	v	LQFP144
NUC442JG8AE	256	64	16	114	4	6+6	4	5	v	6	2	6	2	--	16	3	2	x2, 16-ch	v	6	v	LQFP144
NUC442KI8AE	512	64	16	100	4	6+6	4	5	v	6	2	6	2	--	16	3	2	x2, 16-ch	v	6	v	LQFP128
NUC442KG8AE	256	64	16	100	4	6+6	4	5	v	6	2	6	2	--	16	3	2	x2, 16-ch	v	6	v	LQFP128
NUC442VI8AE	512	64	16	77	4	6+5	4	5	v	6	2	5	2	--	16	3	--	x2, 16-ch	v	5	v	LQFP100
NUC442VG8AE	256	64	16	77	4	6+5	4	5	v	6	2	5	2	--	16	3	--	x2, 16-ch	v	5	v	LQFP100
NUC442RI8AE	512	64	16	45	4	4+3	3	2	v	4	2	3	1	--	8	2	--	x2, 8-ch	v	3	v	LQFP64
NUC442RG8AE	256	64	16	45	4	4+3	3	2	v	4	2	3	1	--	8	2	--	x2, 8-ch	v	3	v	LQFP64

*Marked in this table (6+6) means 6 UART + 6 ISO-7816 UART

*ISO-7816 UART supports full duplex mode

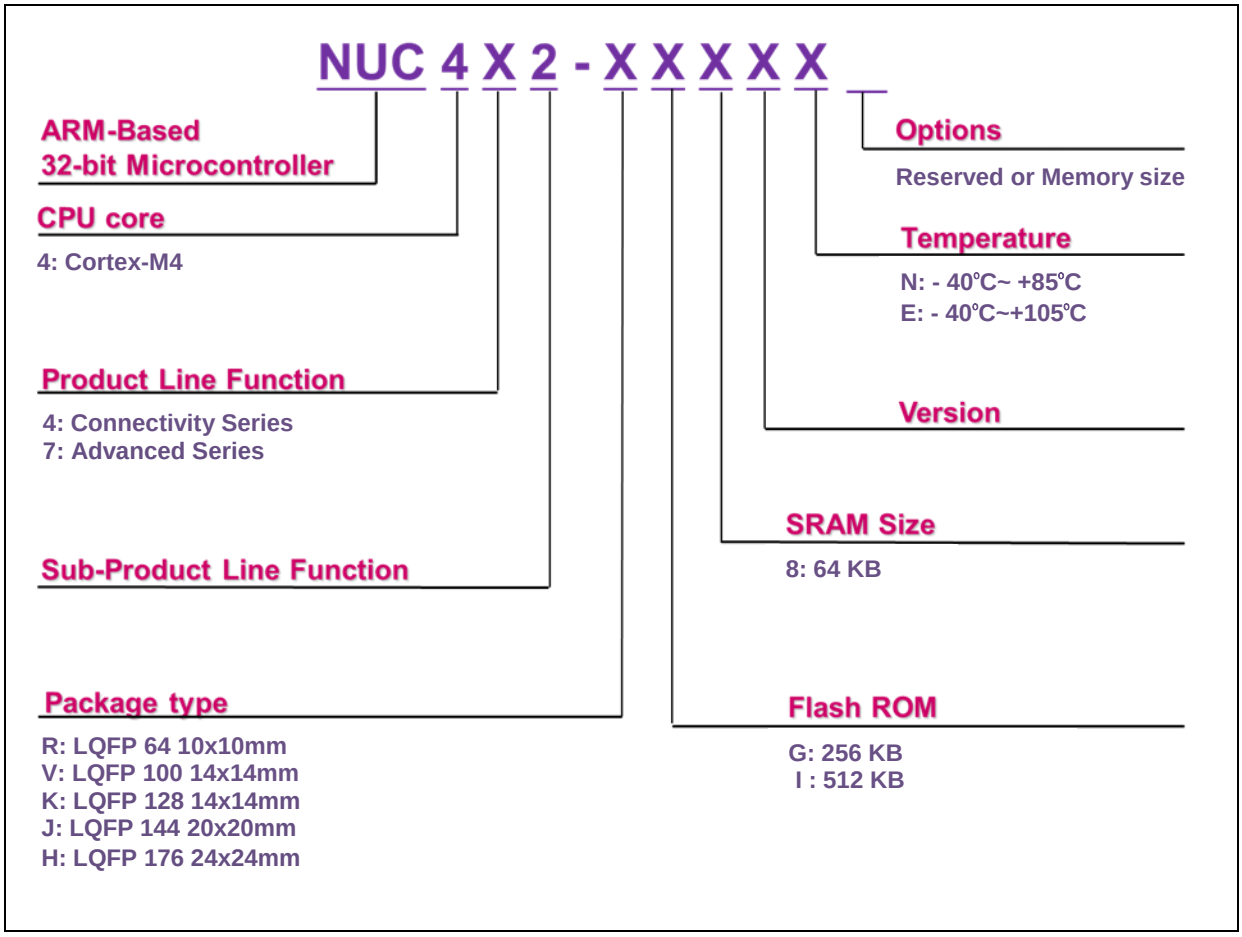


Figure 4.1-1 NuMicro™ NUC442 Series Selection Code

4.2 Pin Configuration

4.2.1 NuMicro™ NUC442 Pin Diagrams

4.2.1.1 NuMicro™ NUC442Rxxxx LQFP 64-pin

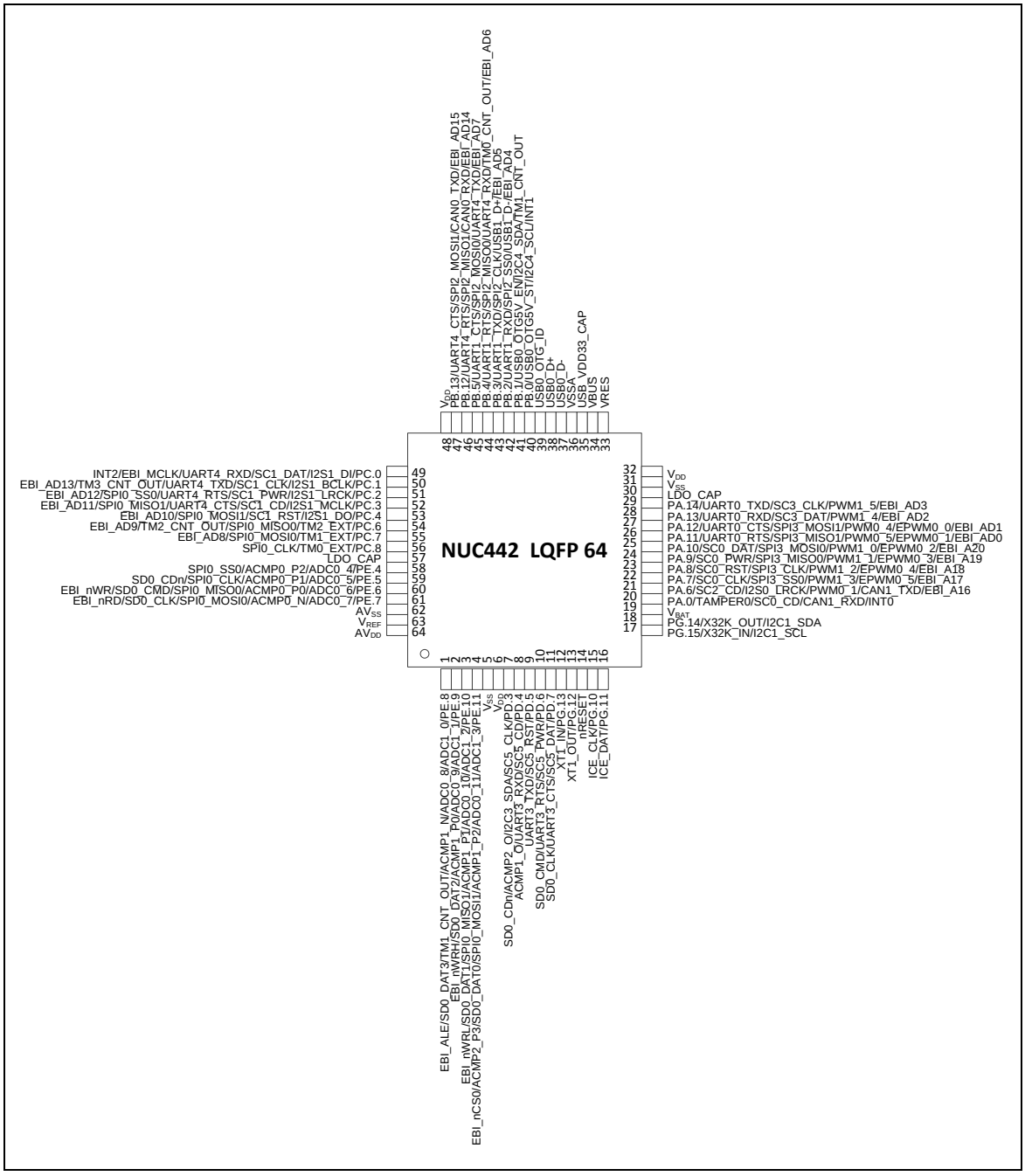


Figure 4.2-1 NuMicro™ NUC442Rxxxx LQFP 64-pin Diagram

4.2.1.2 NuMicro™ NUC442Vxxxx LQFP 100-pin

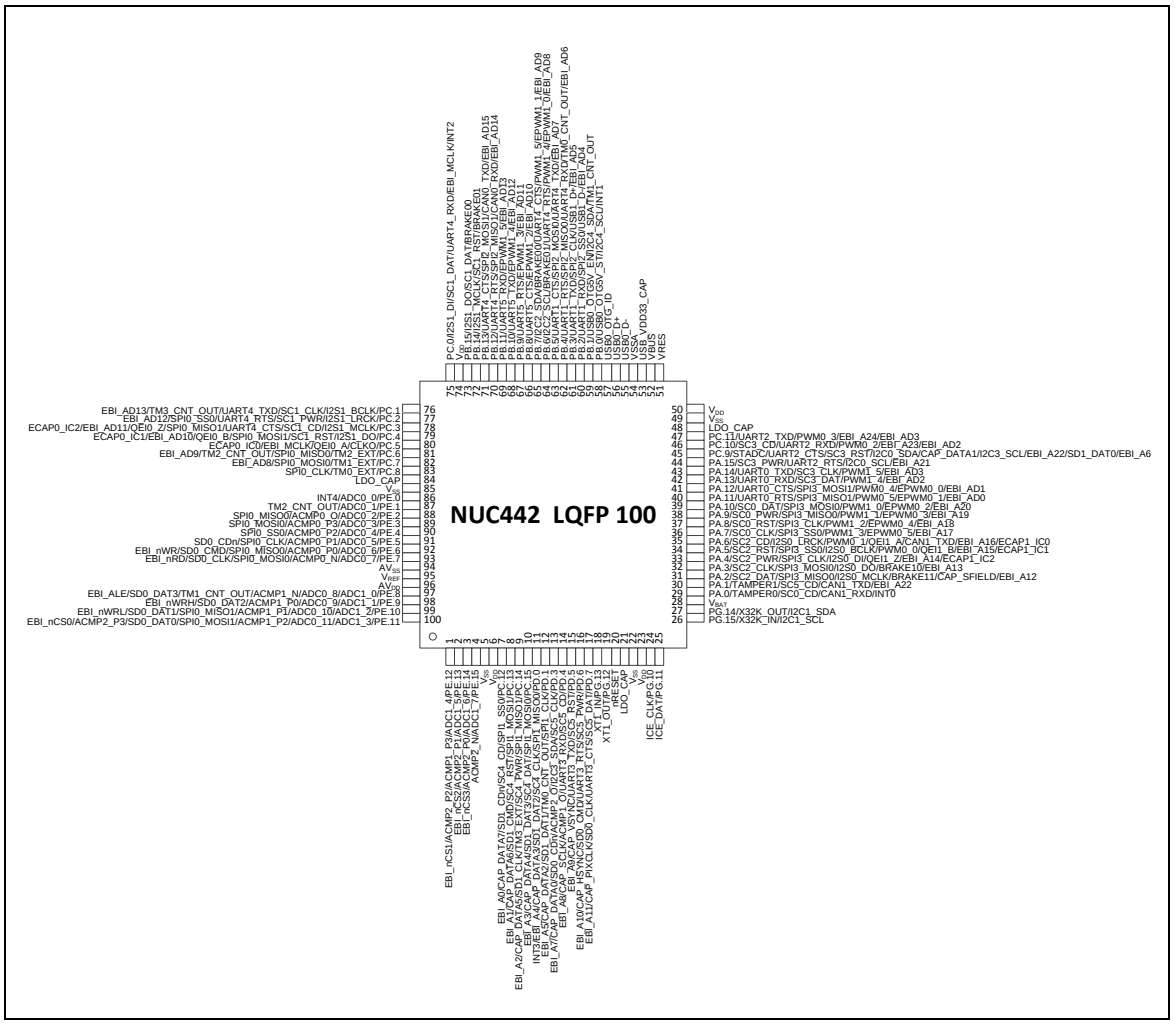


Figure 4.2-2 NuMicro™ NUC442Vxxxx LQFP 100-pin Diagram

4.2.1.3 NuMicro™ NUC442Kxxxx LQFP 128-pin

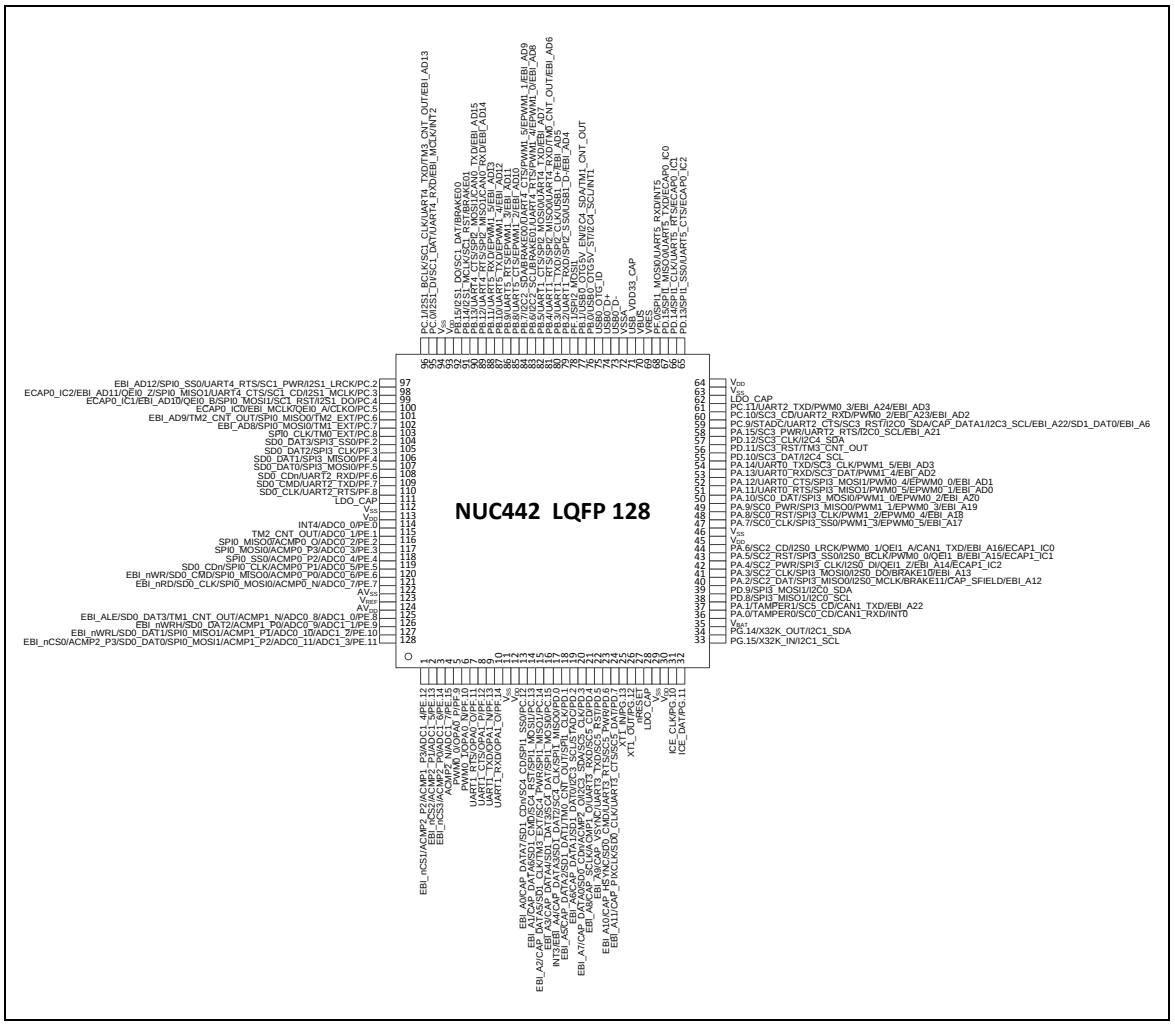


Figure 4.2-3 NuMicro™ NUC442Kxxxx LQFP 128-pin Diagram

4.2.1.4 NuMicro™ NUC442Jxxxx LQFP 144-pin

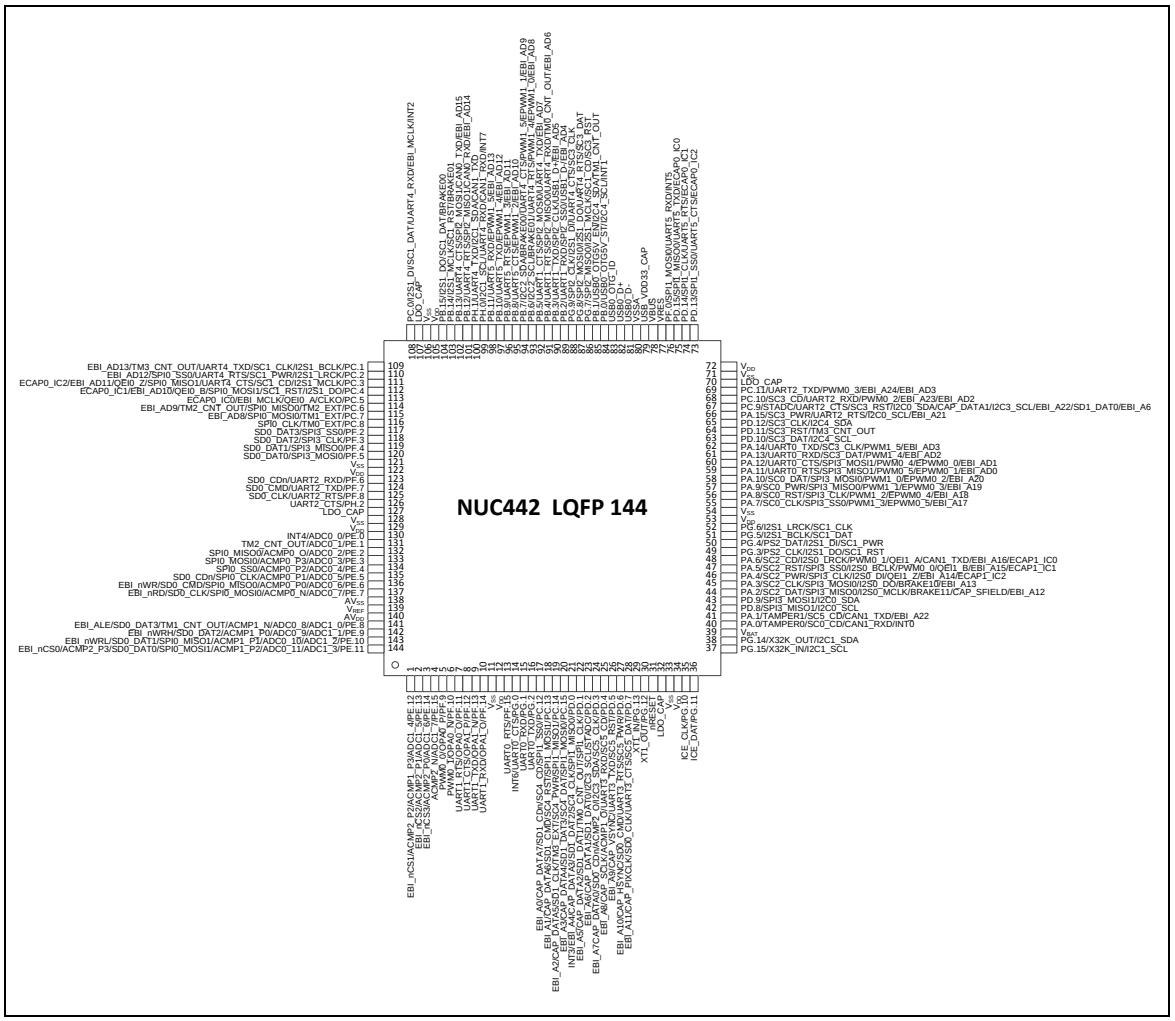


Figure 4.2-4 NuMicro™ NUC442Jxxxx LQFP 144-pin Diagram

4.3 Pin Description

4.3.1 NuMicro™ NUC442 Package LQFP 64-pin Description

MFP = Multi-function pin.

Pin No.	Pin Name	Type	MFP*	Description
1	PE.8	I/O	MFP0	General purpose digital I/O pin.
	ADC1_0	A	MPF1	ADC1 analog input.
	ADC0_8	A	MPF1	ADC0 analog input.
	ACMP1_N	A	MPF2	Analog comparator1 negative input pin.
	TM1_CNT_OUT	I/O	MPF3	Timer1 event counter input/toggle output.
	SD0_DAT3	I/O	MPF4	SD mode #0 data line bit 3.
	EBI_ALE	O	MPF7	EBI address latch enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
2	PE.9	I/O	MFP0	General purpose digital I/O pin.
	ADC1_1	A	MPF1	ADC1 analog input.
	ADC0_9	A	MPF1	ADC0 analog input.
	ACMP1_P0	A	MPF2	Analog comparator1 positive input pin.
	SD0_DAT2	I/O	MPF4	SD mode #0 data line bit 2.
	EBI_nWRH	O	MPF7	EBI write enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
3	PE.10	I/O	MFP0	General purpose digital I/O pin.
	ADC1_2	A	MPF1	ADC1 analog input.
	ADC0_10	A	MPF1	ADC0 analog input.
	ACMP1_P1	A	MPF2	Analog comparator1 positive input pin.
	SPI0_MISO1	I/O	MPF3	2nd SPI0 MISO (Master In, Slave Out) pin.
	SD0_DAT1	I/O	MPF4	SD mode #0 data line bit 1.
	EBI_nWRL	O	MPF7	EBI write enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.

4	PE.11	I/O	MFP0	General purpose digital I/O pin.
	ADC1_3	A	MPF1	ADC1 analog input.
	ADC0_11	A	MPF1	ADC0 analog input.
	ACMP1_P2	A	MPF2	Analog comparator1 positive input pin.
	SPI0_MOSI1	I/O	MPF3	2nd SPI0 MOSI (Master Out, Slave In) pin.
	SD0_DAT0	I/O	MPF4	SD mode #0 data line bit 0.
	ACMP2_P3	A	MPF5	Analog comparator2 positive input pin.
	EBI_nCS0	O	MPF7	EBI chip select 0 enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
5	V_{SS}	P	MFP0	Ground pin for digital circuit.
6	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
7	PD.3	I/O	MFP0	General purpose digital I/O pin.
	SC5_CLK	O	MPF1	SmartCard5 clock pin.
	I2C3_SDA	I/O	MPF2	I2C3 data input/output pin.
	ACMP2_O	O	MPF3	Analog comparator2 output .
	SD0_CDn	I	MPF4	SD mode #0 – card detect
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
8	PD.4	I/O	MFP0	General purpose digital I/O pin.
	SC5_CD	I	MPF1	SmartCard5 card detect pin.
	UART3_RXD	I	MPF2	Data receiver input pin for UART3.
	ACMP1_O	O	MPF3	Analog comparator1 output .
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
9	PD.5	I/O	MFP0	General purpose digital I/O pin.
	SC5_RST	O	MPF1	SmartCard5 reset pin.
	UART3_TXD	O	MPF2	Data transmitter output pin for UART3.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.

10	PD.6	I/O	MFP0	General purpose digital I/O pin.
	SC5_PWR	O	MPF1	SmartCard5 power pin.
	UART3_RTS	O	MPF2	Request to Send output pin for UART3.
	SD0_CMD	I/O	MPF4	SD mode #0 – command/response
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
11	PD.7	I/O	MFP0	General purpose digital I/O pin.
	SC5_DAT	I/O	MPF1	SmartCard5 data pin.
	UART3_CTS	I	MPF2	Clear to Send input pin for UART3.
	SD0_CLK	O	MPF4	SD mode #0– clock.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
12	PG.13	I/O	MFP0	General purpose digital I/O pin.
	XT1_IN	I	MPF1	External 4~24 MHz (high-speed) crystal input pin.
13	PG.12	I/O	MFP0	General purpose digital I/O pin.
	XT1_OUT	O	MPF1	External 4~24 MHz (high-speed) crystal output pin.
14	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
15	PG.10	I/O	MFP0	General purpose digital I/O pin.
	ICE_CLK	I	MPF1	Serial wired debugger clock pin
16	PG.11	I/O	MFP0	General purpose digital I/O pin.
	ICE_DAT	I/O	MPF1	Serial wired debugger data pin
17	PG.15	I/O	MFP0	General purpose digital I/O pin.
	X32K_IN	I	MPF1	External 32.768 kHz (low-speed) crystal input pin.
	I2C1_SCL	I/O	MPF3	I2C1 clock pin.
18	PG.14	I/O	MFP0	General purpose digital I/O pin.
	X32K_OUT	O	MPF1	External 32.768 kHz (low-speed) crystal output pin.
	I2C1_SDA	I/O	MPF3	I2C1 data input/output pin.
19	V_{BAT}	P	MFP0	Battery power input pin.

20	PA.0	I/O	MFP0	General purpose digital I/O pin.
	TAMPER0	I/O	MPF1	Tamper detect pin 0.
	SC0_CD	I	MPF2	SmartCard0 card detect pin.
	CAN1_RXD	I	MPF3	CAN bus receiver1 input.
	INT0	I	MPF8	External interrupt0 input pin.
21	PA.6	I/O	MFP0	General purpose digital I/O pin.
	SC2_CD	I	MPF1	SmartCard2 card detect pin.
	I2S0_LRCK	O	MPF3	I2S0 left right channel clock.
	PWM0_1	I/O	MPF4	PWM0_1 output/capture input.
	CAN1_TXD	I	MPF6	CAN bus transmitter1 input.
	EBI_A16	O	MPF7	EBI address bus bit16.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
22	PA.7	I/O	MFP0	General purpose digital I/O pin.
	SC0_CLK	O	MPF2	SmartCard0 clock pin.
	SPI3_SS0	I/O	MPF3	General purpose digital I/O pin.
	PWM1_3	I/O	MPF4	PWM1_3 output/capture input.
	EPWM0_5	I/O	MPF5	PWM0_5 output/capture input.
	EBI_A17	O	MPF7	EBI address bus bit17.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
23	PA.8	I/O	MFP0	General purpose digital I/O pin.
	SC0_RST	O	MPF2	SmartCard0 reset pin.
	SPI3_CLK	O	MPF3	SPI3 serial clock pin.
	PWM1_2	I/O	MPF4	PWM1_2 output/capture input.
	EPWM0_4	I/O	MPF5	PWM0_4 output/capture input.
	EBI_A18	O	MPF7	EBI address bus bit18.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.

24	PA.9	I/O	MFP0	General purpose digital I/O pin.
	SC0_PWR	O	MPF2	SmartCard0 power pin.
	SPI3_MISO0	I/O	MPF3	1st SPI3 MISO (Master In, Slave Out) pin.
	PWM1_1	I/O	MPF4	PWM1_1 output/capture input.
	EPWM0_3	I/O	MPF5	PWM0_3 output/capture input.
	EBI_A19	O	MPF7	EBI address bus bit19.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
25	PA.10	I/O	MFP0	General purpose digital I/O pin.
	SC0_DAT	I/O	MPF2	SmartCard0 data pin.
	SPI3_MOSI0	I/O	MPF3	1st SPI3 MOSI (Master Out, Slave In) pin.
	PWM1_0	I/O	MPF4	PWM1_0 output/capture input.
	EPWM0_2	I/O	MPF5	PWM0_2 output/capture input.
	EBI_A20	O	MPF7	EBI address bus bit20.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
26	PA.11	I/O	MFP0	General purpose digital I/O pin.
	UART0_RTS	O	MPF1	Request to Send output pin for UART0.
	SPI3_MISO1	I/O	MPF3	2nd SPI3 MISO (Master In, Slave Out) pin.
	PWM0_5	I/O	MPF4	PWM0_5 output/capture input.
	EPWM0_1	I/O	MPF5	PWM0_1 output/capture input.
	EBI_AD0	O	MPF7	EBI address/data bus bit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
27	PA.12	I/O	MFP0	General purpose digital I/O pin.
	UART0_CTS	I	MPF1	Clear to Send input pin for UART0.
	SPI3_MOSI1	I/O	MPF3	2nd SPI3 MOSI (Master Out, Slave In) pin.
	PWM0_4	I/O	MPF4	PWM0_4 output/capture input.
	EPWM0_0	I/O	MPF5	PWM0_0 output/capture input.

	EBI_AD1	O	MPF7	EBI address/data bus bit 1.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
28	PA.13	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MPF1	Data receiver input pin for UART0.
	SC3_DAT	I/O	MPF3	SmartCard3 data pin.
	PWM1_4	I/O	MPF4	PWM1_4 output/capture input.
	EBI_AD2	O	MPF7	EBI address/data bus bit 2.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
29	PA.14	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MPF1	Data transmitter output pin for UART0.
	SC3_CLK	O	MPF3	SmartCard3 clock pin.
	PWM1_5	I/O	MPF4	PWM1_5 output/capture input.
	EBI_AD3	O	MPF7	EBI address/data bus bit 3.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
30	LDO_CAP	P	MFP0	LDO output pin. Note: This pin needs to be connected with a 1uF capacitor.
31	V_{SS}	P	MFP0	Ground pin for digital circuit.
32	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
33	VRES	A	MFP0	USB PHY VRES ground input pin. Add an 8.2K ohm resistor to VSSA.
34	VBUS	A	MFP0	USB PHY VBUS power input pin.
35	USB_VDD33_CAP	P	MFP0	Internal power regulator output 3.3V decoupling pin.
36	VSSA	P	MFP0	Ground pin for digital circuit. Add a Feritte Bead to digital ground V_{SS}.
37	USB0_D-	A	MFP0	USB0 differential signal D-.
38	USB0_D+	A	MFP0	USB0 differential signal D+.
39	USB0_OTG_ID	I	MFP0	USB0 OTG ID pin.

40	PB.0	I/O	MFP0	General purpose digital I/O pin.
	USB0_OTG5V_ST	I	MPF1	USB0 external VBUS regulator status
	I2C4_SCL	I/O	MPF2	I2C4 clock pin.
	INT1	I	MPF8	External interrupt1 input pin.
41	PB.1	I/O	MFP0	General purpose digital I/O pin.
	USB0_OTG5V_EN	O	MPF1	USB0 external VBUS regulator enable
	I2C4_SDA	I/O	MPF2	I2C4 data input/output pin.
	TM1_CNT_OUT	I/O	MPF3	Timer1 event counter input/toggle output.
42	PB.2	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MPF1	Data receiver input pin for UART1.
	SPI2_SS0	I/O	MPF2	General purpose digital I/O pin.
	USB1_D-	A	MPF3	USB1 differential signal D-.
	EBI_AD4	O	MPF7	EBI address/data bus bit 4.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
43	PB.3	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MPF1	Data transmitter output pin for UART1.
	SPI2_CLK	O	MPF2	SPI2 serial clock pin.
	USB1_D+	A	MPF3	USB1 differential signal D+.
	EBI_AD5	O	MPF7	EBI address/data bus bit 5.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
44	PB.4	I/O	MFP0	General purpose digital I/O pin.
	UART1_RTS	O	MPF1	Request to Send output pin for UART1.
	SPI2_MISO0	I/O	MPF2	1st SPI2 MISO (Master In, Slave Out) pin.
	UART4_RXD	I	MPF3	Data receiver input pin for UART4.
	TM0_CNT_OUT	I/O	MPF4	Timer0 event counter input/toggle output.
	EBI_AD6	O	MPF7	EBI address/data bus bit 6.

	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
45	PB.5	I/O	MFP0	General purpose digital I/O pin.
	UART1_CTS	I	MPF1	Clear to Send input pin for UART1.
	SPI2_MOSI0	I/O	MPF2	1st SPI2 MOSI (Master Out, Slave In) pin.
	UART4_TXD	O	MPF3	Data transmitter output pin for UART4.
	EBI_AD7	O	MPF7	EBI address/data bus bit 7.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
46	PB.12	I/O	MFP0	General purpose digital I/O pin.
	UART4_RTS	O	MPF1	Request to Send output pin for UART4.
	SPI2_MISO1	I/O	MPF2	2nd SPI2 MISO (Master In, Slave Out) pin.
	CAN0_RXD	I	MPF3	CAN bus receiver0 input.
	EBI_AD14	O	MPF7	EBI address/data bus bit 14.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
47	PB.13	I/O	MFP0	General purpose digital I/O pin.
	UART4_CTS	I	MPF1	Clear to Send input pin for UART4.
	SPI2_MOSI1	I/O	MPF2	2nd SPI2 MOSI (Master Out, Slave In) pin.
	CAN0_TXD	I	MPF3	CAN bus transmitter0 input.
	EBI_AD15	O	MPF7	EBI address/data bus bit 15.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
48	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
49	PC.0	I/O	MFP0	General purpose digital I/O pin.
	I2S1_DI	I	MPF1	I2S1 data input.
	SC1_DAT	I/O	MPF2	SmartCard1 data pin.
	UART4_RXD	I	MPF3	Data receiver input pin for UART4.
	EBI_MCLK	O	MPF7	EBI interface clock output pin.
	INT2	I	MPF8	External interrupt2 input pin.

	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
50	PC.1	I/O	MFP0	General purpose digital I/O pin.
	I2S1_BCLK	O	MPF1	I2S1 bit clock pin.
	SC1_CLK	O	MPF2	SmartCard1 clock pin.
	UART4_TXD	O	MPF3	Data transmitter output pin for UART4.
	TM3_CNT_OUT	I/O	MPF5	Timer3 event counter input/toggle output.
	EBI_AD13	O	MPF7	EBI address/data bus bit 13.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
51	PC.2	I/O	MFP0	General purpose digital I/O pin.
	I2S1_LRCK	O	MPF1	I2S1 left right channel clock.
	SC1_PWR	O	MPF2	SmartCard1 power pin.
	UART4_RTS	O	MPF3	Request to Send output pin for UART4.
	SPI0_SS0	I/O	MPF4	General purpose digital I/O pin.
	EBI_AD12	O	MPF7	EBI address/data bus bit 12.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
52	PC.3	I/O	MFP0	General purpose digital I/O pin.
	I2S1_MCLK	O	MPF1	I2S1 master clock output pin.
	SC1_CD	I	MPF2	SmartCard1 card detect pin.
	UART4_CTS	I	MPF3	Clear to Send input pin for UART4.
	SPI0_MISO1	I/O	MPF4	2nd SPI0 MISO (Master In, Slave Out) pin.
	EBI_AD11	O	MPF7	EBI address/data bus bit 11.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
53	PC.4	I/O	MFP0	General purpose digital I/O pin.
	I2S1_DO	O	MPF1	I2S1 data output.
	SC1_RST	O	MPF2	SmartCard1 reset pin.
	SPI0_MOSI1	I/O	MPF4	2nd SPI0 MOSI (Master Out, Slave In) pin.

	EBI_AD10	O	MPF7	EBI address/data bus bit 10.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
54	PC.6	I/O	MFP0	General purpose digital I/O pin.
	TM2_EXT	I	MPF1	Timer2 external counter input
	SPI0_MISO0	I/O	MPF4	1st SPI0 MISO (Master In, Slave Out) pin.
	TM2_CNT_OUT	I/O	MPF5	Timer2 event counter input/toggle output.
	EBI_AD9	O	MPF7	EBI address/data bus bit 9.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
55	PC.7	I/O	MFP0	General purpose digital I/O pin.
	TM1_EXT	I	MPF1	Timer1 external counter input
	SPI0_MOSI0	I/O	MPF4	1st SPI0 MOSI (Master Out, Slave In) pin.
	EBI_AD8	O	MPF7	EBI address/data bus bit 8.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
56	PC.8	I/O	MFP0	General purpose digital I/O pin.
	TM0_EXT	I	MPF1	Timer0 external counter input
	SPI0_CLK	O	MPF4	SPI0 serial clock pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
57	LDO_CAP	P	MFP0	LDO output pin. Note: This pin needs to be connected with a 1uF capacitor.
58	PE.4	I/O	MFP0	General purpose digital I/O pin.
	ADC0_4	A	MPF1	ADC0 analog input.
	ACMP0_P2	A	MPF2	Analog comparator0 positive input pin.
	SPI0_SS0	I/O	MPF3	General purpose digital I/O pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
59	PE.5	I/O	MFP0	General purpose digital I/O pin.
	ADC0_5	A	MPF1	ADC0 analog input.

	ACMP0_P1	A	MPF2	Analog comparator0 positive input pin.
	SPI0_CLK	O	MPF3	SPI0 serial clock pin.
	SD0_CDn	I	MPF4	SD mode #0 – card detect
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
60	PE.6	I/O	MFP0	General purpose digital I/O pin.
	ADC0_6	A	MPF1	ADC0 analog input.
	ACMP0_P0	A	MPF2	Analog comparator0 positive input pin.
	SPI0_MISO0	I/O	MPF3	1st SPI0 MISO (Master In, Slave Out) pin.
	SD0_CMD	I/O	MPF4	SD mode #0 – command/response
	EBI_nWR	O	MPF7	EBI write enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
61	PE.7	I/O	MFP0	General purpose digital I/O pin.
	ADC0_7	A	MPF1	ADC0 analog input.
	ACMP0_N	A	MPF2	Analog comparator0 negative input pin.
	SPI0_MOSI0	I/O	MPF3	1st SPI0 MOSI (Master Out, Slave In) pin.
	SD0_CLK	O	MPF4	SD mode #0 – clock.
	EBI_nRD	O	MPF7	EBI read enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
62	AV_{SS}	P	MFP0	Ground pin for digital circuit.
63	V_{REF}	A	MFP0	Voltage reference input for ADC. Note: This pin needs to be connected with 0.1uF/10uF capacitors.
64	AV_{DD}	P	MFP0	Power supply for internal analog circuit.

Note: Pin Type I = Digital Input, O = Digital Output; A = Analog Pin; P = Power Pin;

4.3.2 NuMicro™ NUC442 Package LQFP 100-pin Description

MFP = Multi-function pin.

Pin No.	Pin Name	Type	MFP*	Description
1	PE.12	I/O	MFP0	General purpose digital I/O pin.
	ADC1_4	A	MPF1	ADC1 analog input.
	ACMP1_P3	A	MPF2	Analog comparator1 positive input pin.
	ACMP2_P2	A	MPF3	Analog comparator2 positive input pin.
	EBI_nCS1	O	MPF7	EBI chip select 1 enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
2	PE.13	I/O	MFP0	General purpose digital I/O pin.
	ADC1_5	A	MPF1	ADC1 analog input.
	ACMP2_P1	A	MPF3	Analog comparator2 positive input pin.
	EBI_nCS2	O	MPF7	EBI chip select 2 enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
3	PE.14	I/O	MFP0	General purpose digital I/O pin.
	ADC1_6	A	MPF1	ADC1 analog input.
	ACMP2_P0	A	MPF3	Analog comparator2 positive input pin.
	EBI_nCS3	O	MPF7	EBI chip select 3 enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
4	PE.15	I/O	MFP0	General purpose digital I/O pin.
	ADC1_7	A	MPF1	ADC1 analog input.
	ACMP2_N	A	MPF3	Analog comparator2 negative input pin.
5	V_{SS}	P	MFP0	Ground pin for digital circuit.
6	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
7	PC.12	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS0	I/O	MPF1	1st SPI1 slave select pin..

	SC4_CD	I	MPF2	SmartCard4 card detect pin.
	SD1_CDn	I	MPF4	SD mode #1 – card detect
	CAP_DATA7	I	MPF5	Image data input bus bit 7.
	EBI_A0	O	MPF7	EBI address bus bit0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
8	PC.13	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI1	I/O	MPF1	2nd SPI1 MOSI (Master Out, Slave In) pin.
	SC4_RST	O	MPF2	SmartCard4 reset pin.
	SD1_CMD	I/O	MPF4	SD mode #1 – command/response
	CAP_DATA6	I	MPF5	Image data input bus bit 6.
	EBI_A1	O	MPF7	EBI address bus bit1.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
9	PC.14	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO1	I/O	MPF1	2nd SPI1 MISO (Master In, Slave Out) pin.
	SC4_PWR	O	MPF2	SmartCard4 power pin.
	TM3_EXT	I	MPF3	Timer3 external counter input
	SD1_CLK	O	MPF4	SD mode #1 – clock.
	CAP_DATA5	I	MPF5	Image data input bus bit 5.
	EBI_A2	O	MPF7	EBI address bus bit2.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
10	PC.15	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI0	I/O	MPF1	1st SPI1 MOSI (Master Out, Slave In) pin.
	SC4_DAT	I/O	MPF2	SmartCard4 data pin.
	SD1_DAT3	I/O	MPF4	SD mode #1 data line bit 3.
	CAP_DATA4	I	MPF5	Image data input bus bit 4.
	EBI_A3	O	MPF7	EBI address bus bit3.

	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
11	PD.0	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO0	I/O	MPF1	1st SPI1 MISO (Master In, Slave Out) pin.
	SC4_CLK	O	MPF2	SmartCard4 clock pin.
	SD1_DAT2	I/O	MPF4	SD mode #1 data line bit 2.
	CAP_DATA3	I	MPF5	Image data input bus bit 3.
	EBI_A4	O	MPF7	EBI address bus bit4.
	INT3	I	MPF8	External interrupt3 input pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
12	PD.1	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	O	MPF1	SPI1 serial clock pin.
	TM0_CNT_OUT	I/O	MPF3	Timer0 event counter input/toggle output.
	SD1_DAT1	I/O	MPF4	SD mode #1 data line bit 1.
	CAP_DATA2	I	MPF5	Image data input bus bit 2.
	EBI_A5	O	MPF7	EBI address bus bit5.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
13	PD.3	I/O	MFP0	General purpose digital I/O pin.
	SC5_CLK	O	MPF1	SmartCard5 clock pin.
	I2C3_SDA	I/O	MPF2	I2C3 data input/output pin.
	ACMP2_O	O	MPF3	Analog comparator2 output.
	SD0_CDn	I	MPF4	SD mode #0 – card detect
	CAP_DATA0	I	MPF5	Image data input bus bit 0.
	EBI_A7	O	MPF7	EBI address bus bit7.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
14	PD.4	I/O	MFP0	General purpose digital I/O pin.
	SC5_CD	I	MPF1	SmartCard5 card detect pin.

	UART3_RXD	I	MPF2	Data receiver input pin for UART3.
	ACMP1_O	O	MPF3	Analog comparator1 output.
	CAP_SCLK	O	MPF5	Image capture interface sensor clock pin.
	EBI_A8	O	MPF7	EBI address bus bit8.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
15	PD.5	I/O	MFP0	General purpose digital I/O pin.
	SC5_RST	O	MPF1	SmartCard5 reset pin.
	UART3_TXD	O	MPF2	Data transmitter output pin for UART3.
	CAP_VSYNC	I	MPF5	Image capture interface VSYNC input pin.
	EBI_A9	O	MPF7	EBI address bus bit9.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
16	PD.6	I/O	MFP0	General purpose digital I/O pin.
	SC5_PWR	O	MPF1	SmartCard5 power pin.
	UART3_RTS	O	MPF2	Request to Send output pin for UART3.
	SD0_CMD	I/O	MPF4	SD mode #0 – command/response
	CAP_HSYNC	I	MPF5	Image capture interface HSYNC input pin.
	EBI_A10	O	MPF7	EBI address bus bit10.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
17	PD.7	I/O	MFP0	General purpose digital I/O pin.
	SC5_DAT	I/O	MPF1	SmartCard5 data pin.
	UART3_CTS	I	MPF2	Clear to Send input pin for UART3.
	SD0_CLK	O	MPF4	SD mode #0 – clock.
	CAP_PIXCLK	I	MPF5	Image capture interface pix clock input pin.
	EBI_A11	O	MPF7	EBI address bus bit11.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
18	PG.13	I/O	MFP0	General purpose digital I/O pin.

	XT1_IN	I	MPF1	External 4~24 MHz (high-speed) crystal input pin.
19	PG.12	I/O	MFP0	General purpose digital I/O pin.
	XT1_OUT	O	MPF1	External 4~24 MHz (high-speed) crystal output pin.
20	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
21	LDO_CAP	P	MFP0	LDO output pin. Note: This pin needs to be connected with a 1uF capacitor.
22	V_{SS}	P	MFP0	Ground pin for digital circuit.
23	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
24	PG.10	I/O	MFP0	General purpose digital I/O pin.
	ICE_CLK	I	MPF1	Serial wired debugger clock pin
25	PG.11	I/O	MFP0	General purpose digital I/O pin.
	ICE_DAT	I/O	MPF1	Serial wired debugger data pin
26	PG.15	I/O	MFP0	General purpose digital I/O pin.
	X32K_IN	I	MPF1	External 32.768 kHz (low-speed) crystal input pin.
	I2C1_SCL	I/O	MPF3	I2C1 clock pin.
27	PG.14	I/O	MFP0	General purpose digital I/O pin.
	X32K_OUT	O	MPF1	External 32.768 kHz (low-speed) crystal output pin.
	I2C1_SDA	I/O	MPF3	I2C1 data input/output pin.
28	V_{BAT}	P	MFP0	Battery power input pin.
29	PA.0	I/O	MFP0	General purpose digital I/O pin.
	TAMPER0	I/O	MPF1	Tamper detect pin 0.
	SC0_CD	I	MPF2	SmartCard0 card detect pin.
	CAN1_RXD	I	MPF3	CAN bus receiver1 input.
	INT0	I	MPF8	External interrupt0 input pin.
30	PA.1	I/O	MFP0	General purpose digital I/O pin.
	TAMPER1	I/O	MPF1	Tamper detect pin 1.

	SC5_CD	I	MPF2	SmartCard5 card detect pin.
	CAN1_TXD	I	MPF3	CAN bus transmitter1 input.
	EBI_A22	O	MPF7	EBI address bus bit22.
31	PA.2	I/O	MFP0	General purpose digital I/O pin.
	SC2_DAT	I/O	MPF1	SmartCard2 data pin.
	SPI3_MISO0	I/O	MPF2	1st SPI3 MISO (Master In, Slave Out) pin.
	I2S0_MCLK	O	MPF3	I2S0 master clock output pin.
	BRAKE11	I	MPF4	Brake input pin 1 of EPWM0.
	CAP_SFIELD	I	MPF5	Video input interface SFIELD input pin.
	EBI_A12	O	MPF7	EBI address bus bit12.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
32	PA.3	I/O	MFP0	General purpose digital I/O pin.
	SC2_CLK	O	MPF1	SmartCard2 clock pin.
	SPI3_MOSI0	I/O	MPF2	1st SPI3 MOSI (Master Out, Slave In) pin.
	I2S0_DO	O	MPF3	I2S0 data output.
	BRAKE10	I	MPF4	Brake input pin 0 of EPWM0.
	EBI_A13	O	MPF7	EBI address bus bit13.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
33	PA.4	I/O	MFP0	General purpose digital I/O pin.
	SC2_PWR	O	MPF1	SmartCard2 power pin.
	SPI3_CLK	O	MPF2	SPI3 serial clock pin.
	I2S0_DI	I	MPF3	I2S0 data input.
	QEI1_Z	I	MPF5	Quadrature encoder phase Z input of QEI Unit 1.
	EBI_A14	O	MPF7	EBI address bus bit14.
	ECAP1_IC2	I	MPF8	Input 2 of enhanced capture unit 1.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.

34	PA.5	I/O	MFP0	General purpose digital I/O pin.
	SC2_RST	O	MPF1	SmartCard2 reset pin.
	SPI3_SS0	I/O	MPF2	General purpose digital I/O pin.
	I2S0_BCLK	O	MPF3	I2S0 bit clock pin.
	PWM0_0	I/O	MPF4	PWM0_0 output/capture input.
	QEI1_B	I	MPF5	Quadrature encoder phase B input of QEI Unit 1.
	EBI_A15	O	MPF7	EBI address bus bit15.
	ECAP1_IC1	I	MPF8	Input 1 of enhanced capture unit 1.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
35	PA.6	I/O	MFP0	General purpose digital I/O pin.
	SC2_CD	I	MPF1	SmartCard2 card detect pin.
	I2S0_LRCK	O	MPF3	I2S0 left right channel clock.
	PWM0_1	I/O	MPF4	PWM0_1 output/capture input.
	QEI1_A	I	MPF5	Quadrature encoder phase A input of QEI Unit 1.
	CAN1_TXD	I	MPF6	CAN bus transmitter1 input.
	EBI_A16	O	MPF7	EBI address bus bit16.
	ECAP1_IC0	I	MPF8	Input 0 of enhanced capture unit 1.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
36	PA.7	I/O	MFP0	General purpose digital I/O pin.
	SC0_CLK	O	MPF2	SmartCard0 clock pin.
	SPI3_SS0	I/O	MPF3	General purpose digital I/O pin.
	PWM1_3	I/O	MPF4	PWM1_3 output/capture input.
	EPWM0_5	I/O	MPF5	PWM0_5 output/capture input.
	EBI_A17	O	MPF7	EBI address bus bit17.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
37	PA.8	I/O	MFP0	General purpose digital I/O pin.

	SC0_RST	O	MPF2	SmartCard0 reset pin.
	SPI3_CLK	O	MPF3	SPI3 serial clock pin.
	PWM1_2	I/O	MPF4	PWM1_2 output/capture input.
	EPWM0_4	I/O	MPF5	PWM0_4 output/capture input.
	EBI_A18	O	MPF7	EBI address bus bit18.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
38	PA.9	I/O	MFP0	General purpose digital I/O pin.
	SC0_PWR	O	MPF2	SmartCard0 power pin.
	SPI3_MISO0	I/O	MPF3	1st SPI3 MISO (Master In, Slave Out) pin.
	PWM1_1	I/O	MPF4	PWM1_1 output/capture input.
	EPWM0_3	I/O	MPF5	PWM0_3 output/capture input.
	EBI_A19	O	MPF7	EBI address bus bit19.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
39	PA.10	I/O	MFP0	General purpose digital I/O pin.
	SC0_DAT	I/O	MPF2	SmartCard0 data pin.
	SPI3_MOSI0	I/O	MPF3	1st SPI3 MOSI (Master Out, Slave In) pin.
	PWM1_0	I/O	MPF4	PWM1_0 output/capture input.
	EPWM0_2	I/O	MPF5	PWM0_2 output/capture input.
	EBI_A20	O	MPF7	EBI address bus bit20.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
40	PA.11	I/O	MFP0	General purpose digital I/O pin.
	UART0_RTS	O	MPF1	Request to Send output pin for UART0.
	SPI3_MISO1	I/O	MPF3	2nd SPI3 MISO (Master In, Slave Out) pin.
	PWM0_5	I/O	MPF4	PWM0_5 output/capture input.
	EPWM0_1	I/O	MPF5	PWM0_1 output/capture input.
	EBI_AD0	O	MPF7	EBI address/data bus bit 0.

	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
41	PA.12	I/O	MFP0	General purpose digital I/O pin.
	UART0_CTS	I	MPF1	Clear to Send input pin for UART0.
	SPI3_MOSI1	I/O	MPF3	2nd SPI3 MOSI (Master Out, Slave In) pin.
	PWM0_4	I/O	MPF4	PWM0_4 output/capture input.
	EPWM0_0	I/O	MPF5	PWM0_0 output/capture input.
	EBI_AD1	O	MPF7	EBI address/data bus bit 1.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
42	PA.13	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MPF1	Data receiver input pin for UART0.
	SC3_DAT	I/O	MPF3	SmartCard3 data pin.
	PWM1_4	I/O	MPF4	PWM1_4 output/capture input.
	EBI_AD2	O	MPF7	EBI address/data bus bit 2.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
43	PA.14	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MPF1	Data transmitter output pin for UART0.
	SC3_CLK	O	MPF3	SmartCard3 clock pin.
	PWM1_5	I/O	MPF4	PWM1_5 output/capture input.
	EBI_AD3	O	MPF7	EBI address/data bus bit 3.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
44	PA.15	I/O	MFP0	General purpose digital I/O pin.
	SC3_PWR	O	MPF1	SmartCard3 power pin.
	UART2_RTS	O	MPF2	Request to Send output pin for UART2.
	I2C0_SCL	I/O	MPF4	I2C0 clock pin.
	EBI_A21	O	MPF7	EBI address bus bit21.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.

45	PC.9	I/O	MFP0	General purpose digital I/O pin.
	STADC	A	MPF1	ADC analog input.
	UART2_CTS	I	MPF2	Clear to Send input pin for UART2.
	SC3_RST	O	MPF3	SmartCard3 reset pin.
	I2C0_SDA	I/O	MPF4	I2C0 data input/output pin.
	CAP_DATA1	I	MPF5	Image data input bus bit 1.
	I2C3_SCL	I/O	MPF6	I2C3 clock pin.
	EBI_A22	O	MPF7	EBI address bus bit22.
	SD1_DAT0	I/O	MPF8	SD mode #1 data line bit 0.
	EBI_A6	O	MPF9	EBI address bus bit6.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
46	PC.10	I/O	MFP0	General purpose digital I/O pin.
	SC3_CD	I	MPF1	SmartCard3 card detect pin.
	UART2_RXD	I	MPF2	Data receiver input pin for UART2.
	PWM0_2	I/O	MPF4	PWM0_2 output/capture input.
	EBI_A23	O	MPF6	EBI address bus bit23.
	EBI_AD2	O	MPF7	EBI address/data bus bit 2.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
47	PC.11	I/O	MFP0	General purpose digital I/O pin.
	UART2_TXD	O	MPF2	Data transmitter output pin for UART2.
	PWM0_3	I/O	MPF4	PWM0_3 output/capture input.
	EBI_A24	O	MPF6	EBI address bus bit24.
	EBI_AD3	O	MPF7	EBI address/data bus bit 3.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
48	LDO_CAP	P	MFP0	LDO output pin. Note: This pin needs to be connected with a 1uF capacitor.
49	V_{SS}	P	MFP0	Ground pin for digital circuit.

50	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
51	VRES	A	MFP0	USB PHY VRES ground input pin. Add an 8.2K ohm resistor to VSSA.
52	VBUS	A	MFP0	USB PHY VBUS power input pin.
53	USB_VDD33_CAP	P	MFP0	Internal power regulator output 3.3V decoupling pin.
54	VSSA	P	MFP0	Ground pin for digital circuit. Add a Feritte Bead to digital ground V_{SS}.
55	USB0_D-	A	MFP0	USB0 differential signal D-.
56	USB0_D+	A	MFP0	USB0 differential signal D+.
57	USB0_OTG_ID	I	MFP0	USB0 OTG ID pin.
58	PB.0	I/O	MFP0	General purpose digital I/O pin.
	USB0_OTG5V_ST	I	MPF1	USB0 external VBUS regulator status
	I2C4_SCL	I/O	MPF2	I2C4 clock pin.
	INT1	I	MPF8	External interrupt1 input pin.
59	PB.1	I/O	MFP0	General purpose digital I/O pin.
	USB0_OTG5V_EN	O	MPF1	USB0 external VBUS regulator enable
	I2C4_SDA	I/O	MPF2	I2C4 data input/output pin.
	TM1_CNT_OUT	I/O	MPF3	Timer1 event counter input/toggle output.
60	PB.2	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MPF1	Data receiver input pin for UART1.
	SPI2_SS0	I/O	MPF2	General purpose digital I/O pin.
	USB1_D-	A	MPF3	USB1 differential signal D-.
	EBI_AD4	O	MPF7	EBI address/data bus bit 4.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
61	PB.3	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MPF1	Data transmitter output pin for UART1.
	SPI2_CLK	O	MPF2	SPI2 serial clock pin.
	USB1_D+	A	MPF3	USB1 differential signal D+.

	EBI_AD5	O	MPF7	EBI address/data bus bit 5.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
62	PB.4	I/O	MFP0	General purpose digital I/O pin.
	UART1_RTS	O	MPF1	Request to Send output pin for UART1.
	SPI2_MISO0	I/O	MPF2	1st SPI2 MISO (Master In, Slave Out) pin.
	UART4_RXD	I	MPF3	Data receiver input pin for UART4.
	TM0_CNT_OUT	I/O	MPF4	Timer0 event counter input/toggle output.
	EBI_AD6	O	MPF7	EBI address/data bus bit 6.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
63	PB.5	I/O	MFP0	General purpose digital I/O pin.
	UART1_CTS	I	MPF1	Clear to Send input pin for UART1.
	SPI2_MOSI0	I/O	MPF2	1st SPI2 MOSI (Master Out, Slave In) pin.
	UART4_TXD	O	MPF3	Data transmitter output pin for UART4.
	EBI_AD7	O	MPF7	EBI address/data bus bit 7.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
64	PB.6	I/O	MFP0	General purpose digital I/O pin.
	I2C2_SCL	I/O	MPF1	I2C2 clock pin.
	BRAKE01	I	MPF2	Brake input pin 1 of EPWMB.
	UART4_RTS	O	MPF3	Request to Send output pin for UART4.
	PWM1_4	I/O	MPF4	PWM1_4 output/capture input.
	EPWM1_0	I/O	MPF5	PWM1_0 output/capture input.
	EBI_AD8	O	MPF7	EBI address/data bus bit 8.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
65	PB.7	I/O	MFP0	General purpose digital I/O pin.
	I2C2_SDA	I/O	MPF1	I2C2 data input/output pin.
	BRAKE00	I	MPF2	Brake input pin 0 of EPWMB.

	UART4_CTS	I	MPF3	Clear to Send input pin for UART4.
	PWM1_5	I/O	MPF4	PWM1_5 output/capture input.
	EPWM1_1	I/O	MPF5	PWM1_1 output/capture input.
	EBI_AD9	O	MPF7	EBI address/data bus bit 9.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
66	PB.8	I/O	MFP0	General purpose digital I/O pin.
	UART5_CTS	I	MPF1	Clear to Send input pin for UART5.
	EPWM1_2	I/O	MPF5	PWM1_2 output/capture input.
	EBI_AD10	O	MPF7	EBI address/data bus bit 10.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
67	PB.9	I/O	MFP0	General purpose digital I/O pin.
	UART5_RTS	O	MPF1	Request to Send output pin for UART5.
	EPWM1_3	I/O	MPF5	PWM1_3 output/capture input.
	EBI_AD11	O	MPF7	EBI address/data bus bit 11.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
68	PB.10	I/O	MFP0	General purpose digital I/O pin.
	UART5_TXD	O	MPF1	Data transmitter output pin for UART5.
	EPWM1_4	I/O	MPF5	PWM1_4 output/capture input.
	EBI_AD12	O	MPF7	EBI address/data bus bit 12.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
69	PB.11	I/O	MFP0	General purpose digital I/O pin.
	UART5_RXD	I	MPF1	Data receiver input pin for UART5.
	EPWM1_5	I/O	MPF5	PWM1_5 output/capture input.
	EBI_AD13	O	MPF7	EBI address/data bus bit 13.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
70	PB.12	I/O	MFP0	General purpose digital I/O pin.

	UART4_RTS	O	MPF1	Request to Send output pin for UART4.
	SPI2_MISO1	I/O	MPF2	2nd SPI2 MISO (Master In, Slave Out) pin.
	CAN0_RXD	I	MPF3	CAN bus receiver0 input.
	EBI_AD14	O	MPF7	EBI address/data bus bit 14.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
71	PB.13	I/O	MFP0	General purpose digital I/O pin.
	UART4_CTS	I	MPF1	Clear to Send input pin for UART4.
	SPI2_MOSI1	I/O	MPF2	2nd SPI2 MOSI (Master Out, Slave In) pin.
	CAN0_TXD	I	MPF3	CAN bus transmitter0 input.
	EBI_AD15	O	MPF7	EBI address/data bus bit 15.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
72	PB.14	I/O	MFP0	General purpose digital I/O pin.
	I2S1_MCLK	O	MPF1	I2S1 master clock output pin.
	SC1_RST	O	MPF2	SmartCard1 reset pin.
	BRAKE01	I	MPF4	Brake input pin 1 of EPWMB.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
73	PB.15	I/O	MFP0	General purpose digital I/O pin.
	I2S1_DO	O	MPF1	I2S1 data output.
	SC1_DAT	I/O	MPF2	SmartCard1 data pin.
	BRAKE00	I	MPF4	Brake input pin 0 of EPWMB.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
74	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
75	PC.0	I/O	MFP0	General purpose digital I/O pin.
	I2S1_DI	I	MPF1	I2S1 data input.
	SC1_DAT	I/O	MPF2	SmartCard1 data pin.
	UART4_RXD	I	MPF3	Data receiver input pin for UART4.

	EBI_MCLK	O	MPF7	EBI interface clock output pin.
	INT2	I	MPF8	External interrupt2 input pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
76	PC.1	I/O	MFP0	General purpose digital I/O pin.
	I2S1_BCLK	O	MPF1	I2S1 bit clock pin.
	SC1_CLK	O	MPF2	SmartCard1 clock pin.
	UART4_TXD	O	MPF3	Data transmitter output pin for UART4.
	TM3_CNT_OUT	I/O	MPF5	Timer3 event counter input/toggle output.
	EBI_AD13	O	MPF7	EBI address/data bus bit 13.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
77	PC.2	I/O	MFP0	General purpose digital I/O pin.
	I2S1_LRCK	O	MPF1	I2S1 left right channel clock.
	SC1_PWR	O	MPF2	SmartCard1 power pin.
	UART4_RTS	O	MPF3	Request to Send output pin for UART4.
	SPI0_SS0	I/O	MPF4	General purpose digital I/O pin.
	EBI_AD12	O	MPF7	EBI address/data bus bit 12.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
78	PC.3	I/O	MFP0	General purpose digital I/O pin.
	I2S1_MCLK	O	MPF1	I2S1 master clock output pin.
	SC1_CD	I	MPF2	SmartCard1 card detect pin.
	UART4_CTS	I	MPF3	Clear to Send input pin for UART4.
	SPI0_MISO1	I/O	MPF4	2nd SPI0 MISO (Master In, Slave Out) pin.
	QEI0_Z	I	MPF5	Quadrature encoder phase Z input of QEI Unit 0.
	EBI_AD11	O	MPF7	EBI address/data bus bit 11.
	ECAP0_IC2	O	MPF8	Input 2 of enhanced capture unit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.

79	PC.4	I/O	MFP0	General purpose digital I/O pin.
	I2S1_DO	O	MPF1	I2S1 data output.
	SC1_RST	O	MPF2	SmartCard1 reset pin.
	SPI0_MOSI1	I/O	MPF4	2nd SPI0 MOSI (Master Out, Slave In) pin.
	QEI0_B	I	MPF5	Quadrature encoder phase B input of QEI Unit 0.
	EBI_AD10	O	MPF7	EBI address/data bus bit 10.
	ECAP0_IC1	O	MPF8	Input 1 of enhanced capture unit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
80	PC.5	I/O	MFP0	General purpose digital I/O pin.
	CLKO	O	MFP1	Clock Output Pin.
	QEI0_A	I	MPF5	Quadrature encoder phase A input of QEI Unit 0.
	EBI_MCLK	O	MPF7	EBI interface clock output pin.
	ECAP0_IC0	O	MPF8	Input 0 of enhanced capture unit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
81	PC.6	I/O	MFP0	General purpose digital I/O pin.
	TM2_EXT	I	MPF1	Timer2 external counter input
	SPI0_MISO0	I/O	MPF4	1st SPI0 MISO (Master In, Slave Out) pin.
	TM2_CNT_OUT	I/O	MPF5	Timer2 event counter input/toggle output.
	EBI_AD9	O	MPF7	EBI address/data bus bit 9.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
82	PC.7	I/O	MFP0	General purpose digital I/O pin.
	TM1_EXT	I	MPF1	Timer1 external counter input
	SPI0_MOSI0	I/O	MPF4	1st SPI0 MOSI (Master Out, Slave In) pin.
	EBI_AD8	O	MPF7	EBI address/data bus bit 8.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
83	PC.8	I/O	MFP0	General purpose digital I/O pin.

	TM0_EXT	I	MPF1	Timer0 external counter input
	SPI0_CLK	O	MPF4	SPI0 serial clock pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
84	LDO_CAP	P	MFP0	LDO output pin. Note: This pin needs to be connected with a 1uF capacitor.
85	V_{SS}	P	MFP0	Ground pin for digital circuit.
86	PE.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_0	A	MPF1	ADC0 analog input.
	INT4	I	MPF8	External interrupt4 input pin.
87	PE.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_1	A	MPF1	ADC0 analog input.
	TM2_CNT_OUT	I/O	MPF3	Timer2 event counter input/toggle output.
88	PE.2	I/O	MFP0	General purpose digital I/O pin.
	ADC0_2	A	MPF1	ADC0 analog input.
	ACMP0_O	O	MPF2	Analog comparator0 output .
	SPI0_MISO0	I/O	MPF3	1st SPI0 MISO (Master In, Slave Out) pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
89	PE.3	I/O	MFP0	General purpose digital I/O pin.
	ADC0_3	A	MPF1	ADC0 analog input.
	ACMP0_P3	A	MPF2	Analog comparator0 positive input pin.
	SPI0_MOSI0	I/O	MPF3	1st SPI0 MOSI (Master Out, Slave In) pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
90	PE.4	I/O	MFP0	General purpose digital I/O pin.
	ADC0_4	A	MPF1	ADC0 analog input.
	ACMP0_P2	A	MPF2	Analog comparator0 positive input pin.
	SPI0_SS0	I/O	MPF3	General purpose digital I/O pin.

	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
91	PE.5	I/O	MFP0	General purpose digital I/O pin.
	ADC0_5	A	MPF1	ADC0 analog input.
	ACMP0_P1	A	MPF2	Analog comparator0 positive input pin.
	SPI0_CLK	O	MPF3	SPI0 serial clock pin.
	SD0_CDn	I	MPF4	SD mode #0 – card detect
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
92	PE.6	I/O	MFP0	General purpose digital I/O pin.
	ADC0_6	A	MPF1	ADC0 analog input.
	ACMP0_P0	A	MPF2	Analog comparator0 positive input pin.
	SPI0_MISO0	I/O	MPF3	1st SPI0 MISO (Master In, Slave Out) pin.
	SD0_CMD	I/O	MPF4	SD mode #0 – command/response
	EBI_nWR	O	MPF7	EBI write enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
93	PE.7	I/O	MFP0	General purpose digital I/O pin.
	ADC0_7	A	MPF1	ADC0 analog input.
	ACMP0_N	A	MPF2	Analog comparator0 negative input pin.
	SPI0_MOSI0	I/O	MPF3	1st SPI0 MOSI (Master Out, Slave In) pin.
	SD0_CLK	O	MPF4	SD mode #0 – clock.
	EBI_nRD	O	MPF7	EBI read enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
94	AV_{SS}	P	MFP0	Ground pin for digital circuit.
95	V_{REF}	A	MFP0	Voltage reference input for ADC. Note: This pin needs to be connected with 0.1uF/10uF capacitors.
96	AV_{DD}	P	MFP0	Power supply for internal analog circuit.
97	PE.8	I/O	MFP0	General purpose digital I/O pin.

	ADC1_0	A	MPF1	ADC1 analog input.
	ADC0_8	A	MPF1	ADC0 analog input.
	ACMP1_N	A	MPF2	Analog comparator1 negative input pin.
	TM1_CNT_OUT	I/O	MPF3	Timer1 event counter input/toggle output.
	SD0_DAT3	I/O	MPF4	SD mode #0 data line bit 3.
	EBI_ALE	O	MPF7	EBI address latch enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
98	PE.9	I/O	MFP0	General purpose digital I/O pin.
	ADC1_1	A	MPF1	ADC1 analog input.
	ADC0_9	A	MPF1	ADC0 analog input.
	ACMP1_P0	A	MPF2	Analog comparator1 positive input pin.
	SD0_DAT2	I/O	MPF4	SD mode #0 data line bit 2.
	EBI_nWRH	O	MPF7	EBI write enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
99	PE.10	I/O	MFP0	General purpose digital I/O pin.
	ADC1_2	A	MPF1	ADC1 analog input.
	ADC0_10	A	MPF1	ADC0 analog input.
	ACMP1_P1	A	MPF2	Analog comparator1 positive input pin.
	SPI0_MISO1	I/O	MPF3	2nd SPI0 MISO (Master In, Slave Out) pin.
	SD0_DAT1	I/O	MPF4	SD mode #0 data line bit 1.
	EBI_nWRL	O	MPF7	EBI write enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
100	PE.11	I/O	MFP0	General purpose digital I/O pin.
	ADC1_3	A	MPF1	ADC1 analog input.
	ADC0_11	A	MPF1	ADC0 analog input.
	ACMP1_P2	A	MPF2	Analog comparator1 positive input pin.

	SPI0_MOSI1	I/O	MPF3	2nd SPI0 MOSI (Master Out, Slave In) pin.
	SD0_DAT0	I/O	MPF4	SD mode #0 data line bit 0.
	ACMP2_P3	A	MPF5	Analog comparator2 positive input pin.
	EBI_nCS0	O	MPF7	EBI chip select 0 enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.

Note: Pin Type I = Digital Input, O = Digital Output; A = Analog Pin; P = Power Pin;

4.3.3 NuMicro™ NUC442 Package LQFP 128-pin Description

MFP = Multi-function pin.

Pin No.	Pin Name	Type	MFP*	Description
1	PE.12	I/O	MFP0	General purpose digital I/O pin.
	ADC1_4	A	MPF1	ADC1 analog input.
	ACMP1_P3	A	MPF2	Analog comparator1 positive input pin.
	ACMP2_P2	A	MPF3	Analog comparator2 positive input pin.
	EBI_nCS1	O	MPF7	EBI chip select 1 enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
2	PE.13	I/O	MFP0	General purpose digital I/O pin.
	ADC1_5	A	MPF1	ADC1 analog input.
	ACMP2_P1	A	MPF3	Analog comparator2 positive input pin.
	EBI_nCS2	O	MPF7	EBI chip select 2 enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
3	PE.14	I/O	MFP0	General purpose digital I/O pin.
	ADC1_6	A	MPF1	ADC1 analog input.
	ACMP2_P0	A	MPF3	Analog comparator2 positive input pin.
	EBI_nCS3	O	MPF7	EBI chip select 3 enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
4	PE.15	I/O	MFP0	General purpose digital I/O pin.
	ADC1_7	A	MPF1	ADC1 analog input.
	ACMP2_N	A	MPF3	Analog comparator2 negative input pin.
5	PF.9	I/O	MFP0	General purpose digital I/O pin.
	OPA0_P	I/O	MPF1	General purpose digital I/O pin.
	PWM0_0	I/O	MPF4	PWM0_0 output/capture input.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.

6	PF.10	I/O	MFP0	General purpose digital I/O pin.
	OPA0_N	I/O	MPF1	General purpose digital I/O pin.
	PWM0_1	I/O	MPF4	PWM0_1 output/capture input.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
7	PF.11	I/O	MFP0	General purpose digital I/O pin.
	OPA0_O	O	MPF1	Operational amplifier output pin
	UART1_RTS	O	MPF2	Request to Send output pin for UART1.
8	PF.12	I/O	MFP0	General purpose digital I/O pin.
	OPA1_P	I/O	MPF1	General purpose digital I/O pin.
	UART1_CTS	I	MPF2	Clear to Send input pin for UART1.
9	PF.13	I/O	MFP0	General purpose digital I/O pin.
	OPA1_N	I/O	MPF1	General purpose digital I/O pin.
	UART1_TXD	O	MPF2	Data transmitter output pin for UART1.
10	PF.14	I/O	MFP0	General purpose digital I/O pin.
	OPA1_O	O	MPF1	Operational amplifier output pin
	UART1_RXD	I	MPF2	Data receiver input pin for UART1.
11	V_{SS}	P	MFP0	Ground pin for digital circuit.
12	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
13	PC.12	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS0	I/O	MPF1	1st SPI1 slave select pin..
	SC4_CD	I	MPF2	SmartCard4 card detect pin.
	SD1_CDn	I	MPF4	SD mode #1 – card detect
	CAP_DATA7	I	MPF5	Image data input bus bit 7.
	EBI_A0	O	MPF7	EBI address bus bit0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
14	PC.13	I/O	MFP0	General purpose digital I/O pin.

	SPI1_MOSI1	I/O	MPF1	2nd SPI1 MOSI (Master Out, Slave In) pin.
	SC4_RST	O	MPF2	SmartCard4 reset pin.
	SD1_CMD	I/O	MPF4	SD mode #1 – command/response
	CAP_DATA6	I	MPF5	Image data input bus bit 6.
	EBI_A1	O	MPF7	EBI address bus bit1.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
15	PC.14	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO1	I/O	MPF1	2nd SPI1 MISO (Master In, Slave Out) pin.
	SC4_PWR	O	MPF2	SmartCard4 power pin.
	TM3_EXT	I	MPF3	Timer3 external counter input
	SD1_CLK	O	MPF4	SD mode #1– clock.
	CAP_DATA5	I	MPF5	Image data input bus bit 5.
	EBI_A2	O	MPF7	EBI address bus bit2.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
16	PC.15	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI0	I/O	MPF1	1st SPI1 MOSI (Master Out, Slave In) pin.
	SC4_DAT	I/O	MPF2	SmartCard4 data pin.
	SD1_DAT3	I/O	MPF4	SD mode #1 data line bit 3.
	CAP_DATA4	I	MPF5	Image data input bus bit 4.
	EBI_A3	O	MPF7	EBI address bus bit3.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
17	PD.0	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO0	I/O	MPF1	1st SPI1 MISO (Master In, Slave Out) pin.
	SC4_CLK	O	MPF2	SmartCard4 clock pin.
	SD1_DAT2	I/O	MPF4	SD mode #1 data line bit 2;
	CAP_DATA3	I	MPF5	Image data input bus bit 3.

	EBI_A4	O	MPF7	EBI address bus bit4.
	INT3	I	MPF8	External interrupt3 input pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
18	PD.1	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	O	MPF1	SPI1 serial clock pin.
	TM0_CNT_OUT	I/O	MPF3	Timer0 event counter inpu/toggle output.
	SD1_DAT1	I/O	MPF4	SD mode #1 data line bit 1.
	CAP_DATA2	I	MPF5	Image data input bus bit 2.
	EBI_A5	O	MPF7	EBI address bus bit5.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
19	PD.2	I/O	MFP0	General purpose digital I/O pin.
	STADC	A	MPF1	ADC analog input.
	I2C3_SCL	I/O	MPF2	I2C3 clock pin.
	SD1_DAT0	I/O	MPF4	SD mode #1 data line bit 0.
	CAP_DATA1	I	MPF5	Image data input bus bit 1.
	EBI_A6	O	MPF7	EBI address bus bit6.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
20	PD.3	I/O	MFP0	General purpose digital I/O pin.
	SC5_CLK	O	MPF1	SmartCard5 clock pin.
	I2C3_SDA	I/O	MPF2	I2C3 data input/output pin.
	ACMP2_O	O	MPF3	Analog comparator2 output .
	SD0_CDn	I	MPF4	SD mode #0 – card detect
	CAP_DATA0	I	MPF5	Image data input bus bit 0.
	EBI_A7	O	MPF7	EBI address bus bit7.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
21	PD.4	I/O	MFP0	General purpose digital I/O pin.

	SC5_CD	I	MPF1	SmartCard5 card detect pin.
	UART3_RXD	I	MPF2	Data receiver input pin for UART3.
	ACMP1_O	O	MPF3	Analog comparator1 output .
	CAP_SCLK	O	MPF5	Image capture interface sensor clock pin.
	EBI_A8	O	MPF7	EBI address bus bit8.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
22	PD.5	I/O	MFP0	General purpose digital I/O pin.
	SC5_RST	O	MPF1	SmartCard5 reset pin.
	UART3_TXD	O	MPF2	Data transmitter output pin for UART3.
	CAP_VSYNC	I	MPF5	Image capture interface VSYNC input pin.
	EBI_A9	O	MPF7	EBI address bus bit9.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
23	PD.6	I/O	MFP0	General purpose digital I/O pin.
	SC5_PWR	O	MPF1	SmartCard5 power pin.
	UART3_RTS	O	MPF2	Request to Send output pin for UART3.
	SD0_CMD	I/O	MPF4	SD mode #0 – command/response
	CAP_HSYNC	I	MPF5	Image capture interface HSYNC input pin.
	EBI_A10	O	MPF7	EBI address bus bit10.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
24	PD.7	I/O	MFP0	General purpose digital I/O pin.
	SC5_DAT	I/O	MPF1	SmartCard5 data pin.
	UART3_CTS	I	MPF2	Clear to Send input pin for UART3.
	SD0_CLK	O	MPF4	SD mode #0 – clock.
	CAP_PIXCLK	I	MPF5	Image capture interface pix clock input pin.
	EBI_A11	O	MPF7	EBI address bus bit11.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.

25	PG.13	I/O	MFP0	General purpose digital I/O pin.
	XT1_IN	I	MPF1	External 4~24 MHz (high-speed) crystal input pin.
26	PG.12	I/O	MFP0	General purpose digital I/O pin.
	XT1_OUT	O	MPF1	External 4~24 MHz (high-speed) crystal output pin.
27	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
28	LDO_CAP	P	MFP0	LDO output pin. Note: This pin needs to be connected with a 1uF capacitor.
29	V_{SS}	P	MFP0	Ground pin for digital circuit.
30	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
31	PG.10	I/O	MFP0	General purpose digital I/O pin.
	ICE_CLK	I	MPF1	Serial wired debugger clock pin
32	PG.11	I/O	MFP0	General purpose digital I/O pin.
	ICE_DAT	I/O	MPF1	Serial wired debugger data pin
33	PG.15	I/O	MFP0	General purpose digital I/O pin.
	X32K_IN	I	MPF1	External 32.768 kHz (low-speed) crystal input pin.
	I2C1_SCL	I/O	MPF3	I2C1 clock pin.
34	PG.14	I/O	MFP0	General purpose digital I/O pin.
	X32K_OUT	O	MPF1	External 32.768 kHz (low-speed) crystal output pin.
	I2C1_SDA	I/O	MPF3	I2C1 data input/output pin.
35	V_{BAT}	P	MFP0	Battery power input pin.
36	PA.0	I/O	MFP0	General purpose digital I/O pin.
	TAMPER0	I/O	MPF1	Tamper detect pin 0.
	SC0_CD	I	MPF2	SmartCard0 card detect pin.
	CAN1_RXD	I	MPF3	CAN bus receiver1 input.
	INT0	I	MPF8	External interrupt0 input pin.
37	PA.1	I/O	MFP0	General purpose digital I/O pin.

	TAMPER1	I/O	MPF1	Tamper detect pin 1.
	SC5_CD	I	MPF2	SmartCard5 card detect pin.
	CAN1_TXD	I	MPF3	CAN bus transmitter1 input.
	EBI_A22	O	MPF7	EBI address bus bit22.
38	PD.8	I/O	MFP0	General purpose digital I/O pin.
	SPI3_MISO1	I/O	MPF1	2nd SPI3 MISO (Master In, Slave Out) pin.
	I2C0_SCL	I/O	MPF2	I2C0 clock pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
39	PD.9	I/O	MFP0	General purpose digital I/O pin.
	SPI3_MOSI1	I/O	MPF1	2nd SPI3 MOSI (Master Out, Slave In) pin.
	I2C0_SDA	I/O	MPF2	I2C0 data input/output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
40	PA.2	I/O	MFP0	General purpose digital I/O pin.
	SC2_DAT	I/O	MPF1	SmartCard2 data pin.
	SPI3_MISO0	I/O	MPF2	1st SPI3 MISO (Master In, Slave Out) pin.
	I2S0_MCLK	O	MPF3	I2S0 master clock output pin.
	BRAKE11	I	MPF4	Brake input pin 1 of EPWM0_.
	CAP_SFIELD	I	MPF5	Video input interface SFIELD input pin.
	EBI_A12	O	MPF7	EBI address bus bit12.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
41	PA.3	I/O	MFP0	General purpose digital I/O pin.
	SC2_CLK	O	MPF1	SmartCard2 clock pin.
	SPI3_MOSI0	I/O	MPF2	1st SPI3 MOSI (Master Out, Slave In) pin.
	I2S0_DO	O	MPF3	I2S0 data output.
	BRAKE10	I	MPF4	Brake input pin 0 of EPWM0_.
	EBI_A13	O	MPF7	EBI address bus bit13.

	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
42	PA.4	I/O	MFP0	General purpose digital I/O pin.
	SC2_PWR	O	MPF1	SmartCard2 power pin.
	SPI3_CLK	O	MPF2	SPI3 serial clock pin.
	I2S0_DI	I	MPF3	I2S0 data input.
	QEI1_Z	I	MPF5	Quadrature encoder phase Z input of QEI Unit 1.
	EBI_A14	O	MPF7	EBI address bus bit14.
	ECAP1_IC2	I	MPF8	Input 2 of enhanced capture unit 1.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
43	PA.5	I/O	MFP0	General purpose digital I/O pin.
	SC2_RST	O	MPF1	SmartCard2 reset pin.
	SPI3_SS0	I/O	MPF2	General purpose digital I/O pin.
	I2S0_BCLK	O	MPF3	I2S0 bit clock pin.
	PWM0_0	I/O	MPF4	PWM0_0 output/capture input.
	QEI1_B	I	MPF5	Quadrature encoder phase B input of QEI Unit 1.
	EBI_A15	O	MPF7	EBI address bus bit15.
	ECAP1_IC1	I	MPF8	Input 1 of enhanced capture unit 1.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
44	PA.6	I/O	MFP0	General purpose digital I/O pin.
	SC2_CD	I	MPF1	SmartCard2 card detect pin.
	I2S0_LRCK	O	MPF3	I2S0 left right channel clock.
	PWM0_1	I/O	MPF4	PWM0_1 output/capture input.
	QEI1_A	I	MPF5	Quadrature encoder phase A input of QEI Unit 1.
	CAN1_TXD	I	MPF6	CAN bus transmitter1 input.
	EBI_A16	O	MPF7	EBI address bus bit16.
	ECAP1_IC0	I	MPF8	Input 0 of enhanced capture unit 1.

	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
45	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
46	V_{SS}	P	MFP0	Ground pin for digital circuit.
47	PA.7	I/O	MFP0	General purpose digital I/O pin.
	SC0_CLK	O	MPF2	SmartCard0 clock pin.
	SPI3_SS0	I/O	MPF3	General purpose digital I/O pin.
	PWM1_3	I/O	MPF4	PWM1_3 output/capture input.
	EPWM0_5	I/O	MPF5	PWM0_5 output/capture input.
	EBI_A17	O	MPF7	EBI address bus bit17.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
48	PA.8	I/O	MFP0	General purpose digital I/O pin.
	SC0_RST	O	MPF2	SmartCard0 reset pin.
	SPI3_CLK	O	MPF3	SPI3 serial clock pin.
	PWM1_2	I/O	MPF4	PWM1_2 output/capture input.
	EPWM0_4	I/O	MPF5	PWM0_4 output/capture input.
	EBI_A18	O	MPF7	EBI address bus bit18.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
49	PA.9	I/O	MFP0	General purpose digital I/O pin.
	SC0_PWR	O	MPF2	SmartCard0 power pin.
	SPI3_MISO0	I/O	MPF3	1st SPI3 MISO (Master In, Slave Out) pin.
	PWM1_1	I/O	MPF4	PWM1_1 output/capture input.
	EPWM0_3	I/O	MPF5	PWM0_3 output/capture input.
	EBI_A19	O	MPF7	EBI address bus bit19.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
50	PA.10	I/O	MFP0	General purpose digital I/O pin.
	SC0_DAT	I/O	MPF2	SmartCard0 data pin.

	SPI3_MOSI0	I/O	MPF3	1st SPI3 MOSI (Master Out, Slave In) pin.
	PWM1_0	I/O	MPF4	PWM1_0 output/capture input.
	EPWM0_2	I/O	MPF5	PWM0_2 output/capture input.
	EBI_A20	O	MPF7	EBI address bus bit20.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
51	PA.11	I/O	MFP0	General purpose digital I/O pin.
	UART0_RTS	O	MPF1	Request to Send output pin for UART0.
	SPI3_MISO1	I/O	MPF3	2nd SPI3 MISO (Master In, Slave Out) pin.
	PWM0_5	I/O	MPF4	PWM0_5 output/capture input.
	EPWM0_1	I/O	MPF5	PWM0_1 output/capture input.
	EBI_AD0	O	MPF7	EBI address/data bus bit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
52	PA.12	I/O	MFP0	General purpose digital I/O pin.
	UART0_CTS	I	MPF1	Clear to Send input pin for UART0.
	SPI3_MOSI1	I/O	MPF3	2nd SPI3 MOSI (Master Out, Slave In) pin.
	PWM0_4	I/O	MPF4	PWM0_4 output/capture input.
	EPWM0_0	I/O	MPF5	PWM0_0 output/capture input.
	EBI_AD1	O	MPF7	EBI address/data bus bit 1.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
53	PA.13	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MPF1	Data receiver input pin for UART0.
	SC3_DAT	I/O	MPF3	SmartCard3 data pin.
	PWM1_4	I/O	MPF4	PWM1_4 output/capture input.
	EBI_AD2	O	MPF7	EBI address/data bus bit 2.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
54	PA.14	I/O	MFP0	General purpose digital I/O pin.

	UART0_TXD	O	MPF1	Data transmitter output pin for UART0.
	SC3_CLK	O	MPF3	SmartCard3 clock pin.
	PWM1_5	I/O	MPF4	PWM1_5 output/capture input.
	EBI_AD3	O	MPF7	EBI address/data bus bit 3.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
55	PD.10	I/O	MFP0	General purpose digital I/O pin.
	SC3_DAT	I/O	MPF1	SmartCard3 data pin.
	I2C4_SCL	I/O	MPF2	I2C4 clock pin.
56	PD.11	I/O	MFP0	General purpose digital I/O pin.
	SC3_RST	O	MPF1	SmartCard3 reset pin.
	TM3_CNT_OUT	I/O	MPF3	Timer3 event counter input//toggle output.
57	PD.12	I/O	MFP0	General purpose digital I/O pin.
	SC3_CLK	O	MPF1	SmartCard3 clock pin.
	I2C4_SDA	I/O	MPF2	I2C4 data input/output pin.
58	PA.15	I/O	MFP0	General purpose digital I/O pin.
	SC3_PWR	O	MPF1	SmartCard3 power pin.
	UART2_RTS	O	MPF2	Request to Send output pin for UART2.
	I2C0_SCL	I/O	MPF4	I2C0 clock pin.
	EBI_A21	O	MPF7	EBI address bus bit21.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
59	PC.9	I/O	MFP0	General purpose digital I/O pin.
	STADC	A	MPF1	ADC analog input.
	UART2_CTS	I	MPF2	Clear to Send input pin for UART2.
	SC3_RST	O	MPF3	SmartCard3 reset pin.
	I2C0_SDA	I/O	MPF4	I2C0 data input/output pin.
	CAP_DATA1	I	MPF5	Image data input bus bit 1.
	I2C3_SCL	I/O	MPF6	I2C3 clock pin.

	EBI_A22	O	MPF7	EBI address bus bit22.
	SD1_DAT0	I/O	MPF8	SD mode #1 data line bit 0.
	EBI_A6	O	MPF9	EBI address bus bit6.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
60	PC.10	I/O	MFP0	General purpose digital I/O pin.
	SC3_CD	I	MPF1	SmartCard3 card detect pin.
	UART2_RXD	I	MPF2	Data receiver input pin for UART2.
	PWM0_2	I/O	MPF4	PWM0_2 output/capture input.
	EBI_A23	O	MPF6	EBI address bus bit23.
	EBI_AD2	O	MPF7	EBI address/data bus bit 2.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
61	PC.11	I/O	MFP0	General purpose digital I/O pin.
	UART2_TXD	O	MPF2	Data transmitter output pin for UART2.
	PWM0_3	I/O	MPF4	PWM0_3 output/capture input.
	EBI_A24	O	MPF6	EBI address bus bit24.
	EBI_AD3	O	MPF7	EBI address/data bus bit 3.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
62	LDO_CAP	P	MFP0	LDO output pin. Note: This pin needs to be connected with a 1uF capacitor.
63	V_{SS}	P	MFP0	Ground pin for digital circuit.
64	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
65	PD.13	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS0	I/O	MPF1	1st SPI1 slave select pin..
	UART5_CTS	I	MPF2	Clear to Send input pin for UART5.
	ECAP0_IC2	O	MPF3	Input 2 of enhanced capture unit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.

66	PD.14	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	O	MPF1	SPI1 serial clock pin.
	UART5_RTS	O	MPF2	Request to Send output pin for UART5.
	ECAP0_IC1	O	MPF3	Input 1 of enhanced capture unit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
67	PD.15	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO0	I/O	MPF1	1st SPI1 MISO (Master In, Slave Out) pin.
	UART5_TXD	O	MPF2	Data transmitter output pin for UART5.
	ECAP0_IC0	O	MPF3	Input 0 of enhanced capture unit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
68	PF.0	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI0	I/O	MPF1	1st SPI1 MOSI (Master Out, Slave In) pin.
	UART5_RXD	I	MPF2	Data receiver input pin for UART5.
	INT5	I	MPF8	External interrupt5 input pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
69	VRES	A	MFP0	USB PHY VRES ground input pin. Add an 8.2K ohm resistor to VSSA.
70	VBUS	A	MFP0	USB PHY VBUS power input pin.
71	USB_VDD33_CAP	P	MFP0	Internal power regulator output 3.3V decoupling pin.
72	VSSA	P	MFP0	Ground pin for digital circuit. Add a Feritte Bead to digital ground V_{SS}.
73	USB0_D-	A	MFP0	USB0 differential signal D-.
74	USB0_D+	A	MFP0	USB0 differential signal D+.
75	USB0_OTG_ID	I	MFP0	USB0 OTG ID pin.
76	PB.0	I/O	MFP0	General purpose digital I/O pin.
	USB0_OTG5V_ST	I	MPF1	USB0 external VBUS regulator status
	I2C4_SCL	I/O	MPF2	I2C4 clock pin.

	INT1	I	MPF8	External interrupt1 input pin.
77	PB.1	I/O	MFP0	General purpose digital I/O pin.
	USB0_OTG5V_EN	O	MPF1	USB0 external VBUS regulator enable
	I2C4_SDA	I/O	MPF2	I2C4 data input/output pin.
	TM1_CNT_OUT	I/O	MPF3	Timer1 event counter input/toggle output.
78	PF.1	I/O	MFP0	General purpose digital I/O pin.
	SPI2_MOSI1	I/O	MPF1	2nd SPI2 MOSI (Master Out, Slave In) pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
79	PB.2	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MPF1	Data receiver input pin for UART1.
	SPI2_SS0	I/O	MPF2	General purpose digital I/O pin.
	USB1_D-	A	MPF3	USB1 differential signal D-.
	EBI_AD4	O	MPF7	EBI address/data bus bit 4.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
80	PB.3	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MPF1	Data transmitter output pin for UART1.
	SPI2_CLK	O	MPF2	SPI2 serial clock pin.
	USB1_D+	A	MPF3	USB1 differential signal D+.
	EBI_AD5	O	MPF7	EBI address/data bus bit 5.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
81	PB.4	I/O	MFP0	General purpose digital I/O pin.
	UART1_RTS	O	MPF1	Request to Send output pin for UART1.
	SPI2_MISO0	I/O	MPF2	1st SPI2 MISO (Master In, Slave Out) pin.
	UART4_RXD	I	MPF3	Data receiver input pin for UART4.
	TM0_CNT_OUT	I/O	MPF4	Timer0 event counter input/toggle output.
	EBI_AD6	O	MPF7	EBI address/data bus bit 6.

	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
82	PB.5	I/O	MFP0	General purpose digital I/O pin.
	UART1_CTS	I	MPF1	Clear to Send input pin for UART1.
	SPI2_MOSI0	I/O	MPF2	1st SPI2 MOSI (Master Out, Slave In) pin.
	UART4_TXD	O	MPF3	Data transmitter output pin for UART4.
	EBI_AD7	O	MPF7	EBI address/data bus bit 7.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
83	PB.6	I/O	MFP0	General purpose digital I/O pin.
	I2C2_SCL	I/O	MPF1	I2C2 clock pin.
	BRAKE01	I	MPF2	Brake input pin 1 of EPWMB.
	UART4_RTS	O	MPF3	Request to Send output pin for UART4.
	PWM1_4	I/O	MPF4	PWM1_4 output/capture input.
	EPWM1_0	I/O	MPF5	PWM1_0 output/capture input.
	EBI_AD8	O	MPF7	EBI address/data bus bit 8.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
84	PB.7	I/O	MFP0	General purpose digital I/O pin.
	I2C2_SDA	I/O	MPF1	I2C2 data input/output pin.
	BRAKE00	I	MPF2	Brake input pin 0 of EPWMB.
	UART4_CTS	I	MPF3	Clear to Send input pin for UART4.
	PWM1_5	I/O	MPF4	PWM1_5 output/capture input.
	EPWM1_1	I/O	MPF5	PWM1_1 output/capture input.
	EBI_AD9	O	MPF7	EBI address/data bus bit 9.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
85	PB.8	I/O	MFP0	General purpose digital I/O pin.
	UART5_CTS	I	MPF1	Clear to Send input pin for UART5.
	EPWM1_2	I/O	MPF5	PWM1_2 output/capture input.

	EBI_AD10	O	MPF7	EBI address/data bus bit 10.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
86	PB.9	I/O	MFP0	General purpose digital I/O pin.
	UART5_RTS	O	MPF1	Request to Send output pin for UART5.
	EPWM1_3	I/O	MPF5	PWM1_3 output/capture input.
	EBI_AD11	O	MPF7	EBI address/data bus bit 11.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
87	PB.10	I/O	MFP0	General purpose digital I/O pin.
	UART5_TXD	O	MPF1	Data transmitter output pin for UART5.
	EPWM1_4	I/O	MPF5	PWM1_4 output/capture input.
	EBI_AD12	O	MPF7	EBI address/data bus bit 12.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
88	PB.11	I/O	MFP0	General purpose digital I/O pin.
	UART5_RXD	I	MPF1	Data receiver input pin for UART5.
	EPWM1_5	I/O	MPF5	PWM1_5 output/capture input.
	EBI_AD13	O	MPF7	EBI address/data bus bit 13.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
89	PB.12	I/O	MFP0	General purpose digital I/O pin.
	UART4_RTS	O	MPF1	Request to Send output pin for UART4.
	SPI2_MISO1	I/O	MPF2	2nd SPI2 MISO (Master In, Slave Out) pin.
	CAN0_RXD	I	MPF3	CAN bus receiver0 input.
	EBI_AD14	O	MPF7	EBI address/data bus bit 14.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
90	PB.13	I/O	MFP0	General purpose digital I/O pin.
	UART4_CTS	I	MPF1	Clear to Send input pin for UART4.
	SPI2_MOSI1	I/O	MPF2	2nd SPI2 MOSI (Master Out, Slave In) pin.

	CAN0_TXD	I	MPF3	CAN bus transmitter0 input.
	EBI_AD15	O	MPF7	EBI address/data bus bit 15.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
91	PB.14	I/O	MFP0	General purpose digital I/O pin.
	I2S1_MCLK	O	MPF1	I2S1 master clock output pin.
	SC1_RST	O	MPF2	SmartCard1 reset pin.
	BRAKE01	I	MPF4	Brake input pin 1 of EPWMB.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
92	PB.15	I/O	MFP0	General purpose digital I/O pin.
	I2S1_DO	O	MPF1	I2S1 data output.
	SC1_DAT	I/O	MPF2	SmartCard1 data pin.
	BRAKE00	I	MPF4	Brake input pin 0 of EPWMB.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
93	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
94	V_{SS}	P	MFP0	Ground pin for digital circuit.
95	PC.0	I/O	MFP0	General purpose digital I/O pin.
	I2S1_DI	I	MPF1	I2S1 data input.
	SC1_DAT	I/O	MPF2	SmartCard1 data pin.
	UART4_RXD	I	MPF3	Data receiver input pin for UART4.
	EBI_MCLK	O	MPF7	EBI interface clock output pin.
	INT2	I	MPF8	External interrupt2 input pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
96	PC.1	I/O	MFP0	General purpose digital I/O pin.
	I2S1_BCLK	O	MPF1	I2S1 bit clock pin.
	SC1_CLK	O	MPF2	SmartCard1 clock pin.
	UART4_TXD	O	MPF3	Data transmitter output pin for UART4.

	TM3_CNT_OUT	I/O	MPF5	Timer3 event counter input/toggle output.
	EBI_AD13	O	MPF7	EBI address/data bus bit 13.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
97	PC.2	I/O	MFP0	General purpose digital I/O pin.
	I2S1_LRCK	O	MPF1	I2S1 left right channel clock.
	SC1_PWR	O	MPF2	SmartCard1 power pin.
	UART4_RTS	O	MPF3	Request to Send output pin for UART4.
	SPI0_SS0	I/O	MPF4	General purpose digital I/O pin.
	EBI_AD12	O	MPF7	EBI address/data bus bit 12.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
98	PC.3	I/O	MFP0	General purpose digital I/O pin.
	I2S1_MCLK	O	MPF1	I2S1 master clock output pin.
	SC1_CD	I	MPF2	SmartCard1 card detect pin.
	UART4_CTS	I	MPF3	Clear to Send input pin for UART4.
	SPI0_MISO1	I/O	MPF4	2nd SPI0 MISO (Master In, Slave Out) pin.
	QEI0_Z	I	MPF5	Quadrature encoder phase Z input of QEI Unit 0.
	EBI_AD11	O	MPF7	EBI address/data bus bit 11.
	ECAP0_IC2	O	MPF8	Input 2 of enhanced capture unit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
99	PC.4	I/O	MFP0	General purpose digital I/O pin.
	I2S1_DO	O	MPF1	I2S1 data output.
	SC1_RST	O	MPF2	SmartCard1 reset pin.
	SPI0_MOSI1	I/O	MPF4	2nd SPI0 MOSI (Master Out, Slave In) pin.
	QEI0_B	I	MPF5	Quadrature encoder phase B input of QEI Unit 0.
	EBI_AD10	O	MPF7	EBI address/data bus bit 10.
	ECAP0_IC1	O	MPF8	Input 1 of enhanced capture unit 0.

	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
100	PC.5	I/O	MFP0	General purpose digital I/O pin.
	CLKO	O	MFP1	Clock Output Pin.
	QEI0_A	I	MPF5	Quadrature encoder phase A input of QEI Unit 0.
	EBI_MCLK	O	MPF7	EBI interface clock output pin.
	ECAP0_IC0	O	MPF8	Input 0 of enhanced capture unit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
101	PC.6	I/O	MFP0	General purpose digital I/O pin.
	TM2_EXT	I	MPF1	Timer2 external counter input
	SPI0_MISO0	I/O	MPF4	1st SPI0 MISO (Master In, Slave Out) pin.
	TM2_CNT_OUT	I/O	MPF5	Timer2 event counter input/toggle output.
	EBI_AD9	O	MPF7	EBI address/data bus bit 9.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
102	PC.7	I/O	MFP0	General purpose digital I/O pin.
	TM1_EXT	I	MPF1	Timer1 external counter input
	SPI0_MOSI0	I/O	MPF4	1st SPI0 MOSI (Master Out, Slave In) pin.
	EBI_AD8	O	MPF7	EBI address/data bus bit 8.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
103	PC.8	I/O	MFP0	General purpose digital I/O pin.
	TM0_EXT	I	MPF1	Timer0 external counter input
	SPI0_CLK	O	MPF4	SPI0 serial clock pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
104	PF.2	I/O	MFP0	General purpose digital I/O pin.
	SPI3_SS0	I/O	MPF1	General purpose digital I/O pin.
	SD0_DAT3	I/O	MPF4	SD mode #0 data line bit 3.

	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
105	PF.3	I/O	MFP0	General purpose digital I/O pin.
	SPI3_CLK	O	MPF1	SPI3 serial clock pin.
	SD0_DAT2	I/O	MPF4	SD mode #0 data line bit 2.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
106	PF.4	I/O	MFP0	General purpose digital I/O pin.
	SPI3_MISO0	I/O	MPF1	1st SPI3 MISO (Master In, Slave Out) pin.
	SD0_DAT1	I/O	MPF4	SD mode #0 data line bit 1.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
107	PF.5	I/O	MFP0	General purpose digital I/O pin.
	SPI3_MOSI0	I/O	MPF1	1st SPI3 MOSI (Master Out, Slave In) pin.
	SD0_DAT0	I/O	MPF4	SD mode #0 data line bit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
108	PF.6	I/O	MFP0	General purpose digital I/O pin.
	UART2_RXD	I	MPF1	Data receiver input pin for UART2.
	SD0_CDn	I	MPF4	SD mode #0 – card detect
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
109	PF.7	I/O	MFP0	General purpose digital I/O pin.
	UART2_TXD	O	MPF1	Data transmitter output pin for UART2.
	SD0_CMD	I/O	MPF4	SD mode #0 – command/response
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
110	PF.8	I/O	MFP0	General purpose digital I/O pin.
	UART2_RTS	O	MPF1	Request to Send output pin for UART2.
	SD0_CLK	O	MPF4	SD mode #0 – clock.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.

111	LDO_CAP	P	MFP0	LDO output pin. Note: This pin needs to be connected with a 1uF capacitor.
112	V_{SS}	P	MFP0	Ground pin for digital circuit.
113	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
114	PE.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_0	A	MPF1	ADC0 analog input.
	INT4	I	MPF8	External interrupt4 input pin.
115	PE.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_1	A	MPF1	ADC0 analog input.
	TM2_CNT_OUT	I/O	MPF3	Timer2 event counter input/toggle output.
116	PE.2	I/O	MFP0	General purpose digital I/O pin.
	ADC0_2	A	MPF1	ADC0 analog input.
	ACMP0_O	O	MPF2	Analog comparator0 output .
	SPI0_MISO0	I/O	MPF3	1st SPI0 MISO (Master In, Slave Out) pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
117	PE.3	I/O	MFP0	General purpose digital I/O pin.
	ADC0_3	A	MPF1	ADC0 analog input.
	ACMP0_P3	A	MPF2	Analog comparator0 positive input pin.
	SPI0_MOSI0	I/O	MPF3	1st SPI0 MOSI (Master Out, Slave In) pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
118	PE.4	I/O	MFP0	General purpose digital I/O pin.
	ADC0_4	A	MPF1	ADC0 analog input.
	ACMP0_P2	A	MPF2	Analog comparator0 positive input pin.
	SPI0_SS0	I/O	MPF3	General purpose digital I/O pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
119	PE.5	I/O	MFP0	General purpose digital I/O pin.

	ADC0_5	A	MPF1	ADC0 analog input.
	ACMP0_P1	A	MPF2	Analog comparator0 positive input pin.
	SPI0_CLK	O	MPF3	SPI0 serial clock pin.
	SD0_CDn	I	MPF4	SD mode #0 – card detect
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
120	PE.6	I/O	MFP0	General purpose digital I/O pin.
	ADC0_6	A	MPF1	ADC0 analog input.
	ACMP0_P0	A	MPF2	Analog comparator0 positive input pin.
	SPI0_MISO0	I/O	MPF3	1st SPI0 MISO (Master In, Slave Out) pin.
	SD0_CMD	I/O	MPF4	SD mode #0 – command/response
	EBI_nWR	O	MPF7	EBI write enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
121	PE.7	I/O	MFP0	General purpose digital I/O pin.
	ADC0_7	A	MPF1	ADC0 analog input.
	ACMP0_N	A	MPF2	Analog comparator0 negative input pin.
	SPI0_MOSI0	I/O	MPF3	1st SPI0 MOSI (Master Out, Slave In) pin.
	SD0_CLK	O	MPF4	SD mode #0– clock.
	EBI_nRD	O	MPF7	EBI read enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
122	AV_{SS}	P	MFP0	Ground pin for digital circuit.
123	V_{REF}	A	MFP0	Voltage reference input for ADC. Note: This pin needs to be connected with 0.1uF/10uF capacitors.
124	AV_{DD}	P	MFP0	Power supply for internal analog circuit.
125	PE.8	I/O	MFP0	General purpose digital I/O pin.
	ADC1_0	A	MPF1	ADC1 analog input.
	ADC0_8	A	MPF1	ADC0 analog input.
	ACMP1_N	A	MPF2	Analog comparator1 negative input pin.

	TM1_CNT_OUT	I/O	MPF3	Timer1 event counter input/toggle output.
	SD0_DAT3	I/O	MPF4	SD mode #0 data line bit 3.
	EBI_ALE	O	MPF7	EBI address latch enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
126	PE.9	I/O	MFP0	General purpose digital I/O pin.
	ADC1_1	A	MPF1	ADC1 analog input.
	ADC0_9	A	MPF1	ADC0 analog input.
	ACMP1_P0	A	MPF2	Analog comparator1 positive input pin.
	SD0_DAT2	I/O	MPF4	SD mode #0 data line bit 2.
	EBI_nWRH	O	MPF7	EBI write enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
127	PE.10	I/O	MFP0	General purpose digital I/O pin.
	ADC1_2	A	MPF1	ADC1 analog input.
	ADC0_10	A	MPF1	ADC0 analog input.
	ACMP1_P1	A	MPF2	Analog comparator1 positive input pin.
	SPI0_MISO1	I/O	MPF3	2nd SPI0 MISO (Master In, Slave Out) pin.
	SD0_DAT1	I/O	MPF4	SD mode #0 data line bit 1.
	EBI_nWRL	O	MPF7	EBI write enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
128	PE.11	I/O	MFP0	General purpose digital I/O pin.
	ADC1_3	A	MPF1	ADC1 analog input.
	ADC0_11	A	MPF1	ADC0 analog input.
	ACMP1_P2	A	MPF2	Analog comparator1 positive input pin.
	SPI0_MOSI1	I/O	MPF3	2nd SPI0 MOSI (Master Out, Slave In) pin.
	SD0_DAT0	I/O	MPF4	SD mode #0 data line bit 0.
	ACMP2_P3	A	MPF5	Analog comparator2 positive input pin.

	EBI_nCS0	O	MPF7	EBI chip select 0 enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.

Note: Pin Type I = Digital Input, O = Digital Output; A = Analog Pin; P = Power Pin;

4.3.4 NuMicro™ NUC442 Package LQFP 144-pin Description

MFP = Multi-function pin.

Pin No.	Pin Name	Type	MFP*	Description
1	PE.12	I/O	MFP0	General purpose digital I/O pin.
	ADC1_4	A	MPF1	ADC1 analog input.
	ACMP1_P3	A	MPF2	Analog comparator1 positive input pin.
	ACMP2_P2	A	MPF3	Analog comparator2 positive input pin.
	EBI_nCS1	O	MPF7	EBI chip select 1 enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
2	PE.13	I/O	MFP0	General purpose digital I/O pin.
	ADC1_5	A	MPF1	ADC1 analog input.
	ACMP2_P1	A	MPF3	Analog comparator2 positive input pin.
	EBI_nCS2	O	MPF7	EBI chip select 2 enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
3	PE.14	I/O	MFP0	General purpose digital I/O pin.
	ADC1_6	A	MPF1	ADC1 analog input.
	ACMP2_P0	A	MPF3	Analog comparator2 positive input pin.
	EBI_nCS3	O	MPF7	EBI chip select 3 enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
4	PE.15	I/O	MFP0	General purpose digital I/O pin.
	ADC1_7	A	MPF1	ADC1 analog input.
	ACMP2_N	A	MPF3	Analog comparator2 negative input pin.
5	PF.9	I/O	MFP0	General purpose digital I/O pin.
	OPA0_P	I/O	MPF1	General purpose digital I/O pin.
	PWM0_0	I/O	MPF4	PWM0_0 output/capture input.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.

6	PF.10	I/O	MFP0	General purpose digital I/O pin.
	OPA0_N	I/O	MPF1	General purpose digital I/O pin.
	PWM0_1	I/O	MPF4	PWM0_1 output/capture input.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
7	PF.11	I/O	MFP0	General purpose digital I/O pin.
	OPA0_O	O	MPF1	Operational amplifier output pin
	UART1_RTS	O	MPF2	Request to Send output pin for UART1.
8	PF.12	I/O	MFP0	General purpose digital I/O pin.
	OPA1_P	I/O	MPF1	General purpose digital I/O pin.
	UART1_CTS	I	MPF2	Clear to Send input pin for UART1.
9	PF.13	I/O	MFP0	General purpose digital I/O pin.
	OPA1_N	I/O	MPF1	General purpose digital I/O pin.
	UART1_TXD	O	MPF2	Data transmitter output pin for UART1.
10	PF.14	I/O	MFP0	General purpose digital I/O pin.
	OPA1_O	O	MPF1	Operational amplifier output pin
	UART1_RXD	I	MPF2	Data receiver input pin for UART1.
11	V_{SS}	P	MFP0	Ground pin for digital circuit.
12	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
13	PF.15	I/O	MFP0	General purpose digital I/O pin.
	UART0_RTS	O	MPF1	Request to Send output pin for UART0.
14	PG.0	I/O	MFP0	General purpose digital I/O pin.
	UART0_CTS	I	MPF1	Clear to Send input pin for UART0.
	INT6	I	MPF8	External interrupt6 input pin.
15	PG.1	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MPF1	Data receiver input pin for UART0.
16	PG.2	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MPF1	Data transmitter output pin for UART0.

17	PC.12	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS0	I/O	MPF1	1st SPI1 slave select pin..
	SC4_CD	I	MPF2	SmartCard4 card detect pin.
	SD1_CDn	I	MPF4	SD mode #1 – card detect
	CAP_DATA7	I	MPF5	Image data input bus bit 7.
	EBI_A0	O	MPF7	EBI address bus bit0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
18	PC.13	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI1	I/O	MPF1	2nd SPI1 MOSI (Master Out, Slave In) pin.
	SC4_RST	O	MPF2	SmartCard4 reset pin.
	SD1_CMD	I/O	MPF4	SD mode #1 – command/response
	CAP_DATA6	I	MPF5	Image data input bus bit 6.
	EBI_A1	O	MPF7	EBI address bus bit1.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
19	PC.14	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO1	I/O	MPF1	2nd SPI1 MISO (Master In, Slave Out) pin.
	SC4_PWR	O	MPF2	SmartCard4 power pin.
	TM3_EXT	I	MPF3	Timer3 external counter input
	SD1_CLK	O	MPF4	SD mode #1– clock.
	CAP_DATA5	I	MPF5	Image data input bus bit 5.
	EBI_A2	O	MPF7	EBI address bus bit2.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
20	PC.15	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI0	I/O	MPF1	1st SPI1 MOSI (Master Out, Slave In) pin.
	SC4_DAT	I/O	MPF2	SmartCard4 data pin.
	SD1_DAT3	I/O	MPF4	SD mode #1 data line bit 3;

	CAP_DATA4	I	MPF5	Image data input bus bit 4.
	EBI_A3	O	MPF7	EBI address bus bit3.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
21	PD.0	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO0	I/O	MPF1	1st SPI1 MISO (Master In, Slave Out) pin.
	SC4_CLK	O	MPF2	SmartCard4 clock pin.
	SD1_DAT2	I/O	MPF4	SD mode #1 data line bit 2;
	CAP_DATA3	I	MPF5	Image data input bus bit 3.
	EBI_A4	O	MPF7	EBI address bus bit4.
	INT3	I	MPF8	External interrupt3 input pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
22	PD.1	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	O	MPF1	SPI1 serial clock pin.
	TM0_CNT_OUT	I/O	MPF3	Timer0 event counter input/toggle output.
	SD1_DAT1	I/O	MPF4	SD mode #1 data line bit 1;
	CAP_DATA2	I	MPF5	Image data input bus bit 2.
	EBI_A5	O	MPF7	EBI address bus bit5.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
23	PD.2	I/O	MFP0	General purpose digital I/O pin.
	STADC	A	MPF1	ADC analog input.
	I2C3_SCL	I/O	MPF2	I2C3 clock pin.
	SD1_DAT0	I/O	MPF4	SD mode #1 data line bit 0.
	CAP_DATA1	I	MPF5	Image data input bus bit 1.
	EBI_A6	O	MPF7	EBI address bus bit6.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
24	PD.3	I/O	MFP0	General purpose digital I/O pin.

	SC5_CLK	O	MPF1	SmartCard5 clock pin.
	I2C3_SDA	I/O	MPF2	I2C3 data input/output pin.
	ACMP2_O	O	MPF3	Analog comparator2 output .
	SD0_CDn	I	MPF4	SD mode #0 – card detect
	CAP_DATA0	I	MPF5	Image data input bus bit 0.
	EBI_A7	O	MPF7	EBI address bus bit7.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
25	PD.4	I/O	MFP0	General purpose digital I/O pin.
	SC5_CD	I	MPF1	SmartCard5 card detect pin.
	UART3_RXD	I	MPF2	Data receiver input pin for UART3.
	ACMP1_O	O	MPF3	Analog comparator1 output.
	CAP_SCLK	O	MPF5	Image capture interface sensor clock pin.
	EBI_A8	O	MPF7	EBI address bus bit8.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
26	PD.5	I/O	MFP0	General purpose digital I/O pin.
	SC5_RST	O	MPF1	SmartCard5 reset pin.
	UART3_TXD	O	MPF2	Data transmitter output pin for UART3.
	CAP_VSYNC	I	MPF5	Image capture interface VSYNC input pin.
	EBI_A9	O	MPF7	EBI address bus bit9.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
27	PD.6	I/O	MFP0	General purpose digital I/O pin.
	SC5_PWR	O	MPF1	SmartCard5 power pin.
	UART3_RTS	O	MPF2	Request to Send output pin for UART3.
	SD0_CMD	I/O	MPF4	SD mode #0 – command/response
	CAP_HSYNC	I	MPF5	Image capture interface HSYNC input pin.
	EBI_A10	O	MPF7	EBI address bus bit10.

	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
28	PD.7	I/O	MFP0	General purpose digital I/O pin.
	SC5_DAT	I/O	MPF1	SmartCard5 data pin.
	UART3_CTS	I	MPF2	Clear to Send input pin for UART3.
	SD0_CLK	O	MPF4	SD mode #0 – clock.
	CAP_PIXCLK	I	MPF5	Image capture interface pix clock input pin.
	EBI_A11	O	MPF7	EBI address bus bit11.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
29	PG.13	I/O	MFP0	General purpose digital I/O pin.
	XT1_IN	I	MPF1	External 4~24 MHz (high-speed) crystal input pin.
30	PG.12	I/O	MFP0	General purpose digital I/O pin.
	XT1_OUT	O	MPF1	External 4~24 MHz (high-speed) crystal output pin.
31	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
32	LDO_CAP	P	MFP0	LDO output pin. Note: This pin needs to be connected with a 1uF capacitor.
33	V_{SS}	P	MFP0	Ground pin for digital circuit.
34	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
35	PG.10	I/O	MFP0	General purpose digital I/O pin.
	ICE_CLK	I	MPF1	Serial wired debugger clock pin
36	PG.11	I/O	MFP0	General purpose digital I/O pin.
	ICE_DAT	I/O	MPF1	Serial wired debugger data pin
37	PG.15	I/O	MFP0	General purpose digital I/O pin.
	X32K_IN	I	MPF1	External 32.768 kHz (low-speed) crystal input pin.
	I2C1_SCL	I/O	MPF3	I2C1 clock pin.
38	PG.14	I/O	MFP0	General purpose digital I/O pin.
	X32K_OUT	O	MPF1	External 32.768 kHz (low-speed) crystal output pin.

	I2C1_SDA	I/O	MPF3	I2C1 data input/output pin.
39	V_{BAT}	P	MFP0	Battery power input pin.
40	PA.0	I/O	MFP0	General purpose digital I/O pin.
	TAMPER0	I/O	MPF1	Tamper detect pin 0.
	SC0_CD	I	MPF2	SmartCard0 card detect pin.
	CAN1_RXD	I	MPF3	CAN bus receiver1 input.
	INT0	I	MPF8	External interrupt0 input pin.
41	PA.1	I/O	MFP0	General purpose digital I/O pin.
	TAMPER1	I/O	MPF1	Tamper detect pin 1.
	SC5_CD	I	MPF2	SmartCard5 card detect pin.
	CAN1_TXD	I	MPF3	CAN bus transmitter1 input.
	EBI_A22	O	MPF7	EBI address bus bit22.
42	PD.8	I/O	MFP0	General purpose digital I/O pin.
	SPI3_MISO1	I/O	MPF1	2nd SPI3 MISO (Master In, Slave Out) pin.
	I2C0_SCL	I/O	MPF2	I2C0 clock pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
43	PD.9	I/O	MFP0	General purpose digital I/O pin.
	SPI3_MOSI1	I/O	MPF1	2nd SPI3 MOSI (Master Out, Slave In) pin.
	I2C0_SDA	I/O	MPF2	I2C0 data input/output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
44	PA.2	I/O	MFP0	General purpose digital I/O pin.
	SC2_DAT	I/O	MPF1	SmartCard2 data pin.
	SPI3_MISO0	I/O	MPF2	1st SPI3 MISO (Master In, Slave Out) pin.
	I2S0_MCLK	O	MPF3	I2S0 master clock output pin.
	BRAKE11	I	MPF4	Brake input pin 1 of EPWMA.
	CAP_SFIELD	I	MPF5	Video input interface SFIELD input pin.
	EBI_A12	O	MPF7	EBI address bus bit12.

	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
45	PA.3	I/O	MFP0	General purpose digital I/O pin.
	SC2_CLK	O	MPF1	SmartCard2 clock pin.
	SPI3_MOSI0	I/O	MPF2	1st SPI3 MOSI (Master Out, Slave In) pin.
	I2S0_DO	O	MPF3	I2S0 data output.
	BRAKE10	I	MPF4	Brake input pin 0 of EPWMA.
	EBI_A13	O	MPF7	EBI address bus bit13.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
46	PA.4	I/O	MFP0	General purpose digital I/O pin.
	SC2_PWR	O	MPF1	SmartCard2 power pin.
	SPI3_CLK	O	MPF2	SPI3 serial clock pin.
	I2S0_DI	I	MPF3	I2S0 data input.
	QEI1_Z	I	MPF5	Quadrature encoder phase Z input of QEI Unit 1.
	EBI_A14	O	MPF7	EBI address bus bit14.
	ECAP1_IC2	I	MPF8	Input 2 of enhanced capture unit 1.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
47	PA.5	I/O	MFP0	General purpose digital I/O pin.
	SC2_RST	O	MPF1	SmartCard2 reset pin.
	SPI3_SS0	I/O	MPF2	General purpose digital I/O pin.
	I2S0_BCLK	O	MPF3	I2S0 bit clock pin.
	PWM0_0	I/O	MPF4	PWM0_0 output/capture input.
	QEI1_B	I	MPF5	Quadrature encoder phase B input of QEI Unit 1.
	EBI_A15	O	MPF7	EBI address bus bit15.
	ECAP1_IC1	I	MPF8	Input 1 of enhanced capture unit 1.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
48	PA.6	I/O	MFP0	General purpose digital I/O pin.

	SC2_CD	I	MPF1	SmartCard2 card detect pin.
	I2S0_LRCK	O	MPF3	I2S0 left right channel clock.
	PWM0_1	I/O	MPF4	PWM0_1 output/capture input.
	QEI1_A	I	MPF5	Quadrature encoder phase A input of QEI Unit 1.
	CAN1_TXD	I	MPF6	CAN bus transmitter1 input.
	EBI_A16	O	MPF7	EBI address bus bit16.
	ECAP1_IC0	I	MPF8	Input 0 of enhanced capture unit 1.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
49	PG.3	I/O	MFP0	General purpose digital I/O pin.
	PS2_CLK	O	MPF1	PS2 clock pin.
	I2S1_DO	O	MPF2	I2S1 data output.
	SC1_RST	O	MPF3	SmartCard1 reset pin.
50	PG.4	I/O	MFP0	General purpose digital I/O pin.
	PS2_DAT	I/O	MPF1	PS2 data pin.
	I2S1_DI	I	MPF2	I2S1 data input.
	SC1_PWR	O	MPF3	SmartCard1 power pin.
51	PG.5	I/O	MFP0	General purpose digital I/O pin.
	I2S1_BCLK	O	MPF2	I2S1 bit clock pin.
	SC1_DAT	I/O	MPF3	SmartCard1 data pin.
52	PG.6	I/O	MFP0	General purpose digital I/O pin.
	I2S1_LRCK	O	MPF2	I2S1 left right channel clock.
	SC1_CLK	O	MPF3	SmartCard1 clock pin.
53	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
54	V_{SS}	P	MFP0	Ground pin for digital circuit.
55	PA.7	I/O	MFP0	General purpose digital I/O pin.
	SC0_CLK	O	MPF2	SmartCard0 clock pin.
	SPI3_SS0	I/O	MPF3	General purpose digital I/O pin.

	PWM1_3	I/O	MPF4	PWM1_3 output/capture input.
	EPWM0_5	I/O	MPF5	PWM0_5 output/capture input.
	EBI_A17	O	MPF7	EBI address bus bit17.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
56	PA.8	I/O	MFP0	General purpose digital I/O pin.
	SC0_RST	O	MPF2	SmartCard0 reset pin.
	SPI3_CLK	O	MPF3	SPI3 serial clock pin.
	PWM1_2	I/O	MPF4	PWM1_2 output/capture input.
	EPWM0_4	I/O	MPF5	PWM0_4 output/capture input.
	EBI_A18	O	MPF7	EBI address bus bit18.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
57	PA.9	I/O	MFP0	General purpose digital I/O pin.
	SC0_PWR	O	MPF2	SmartCard0 power pin.
	SPI3_MISO0	I/O	MPF3	1st SPI3 MISO (Master In, Slave Out) pin.
	PWM1_1	I/O	MPF4	PWM1_1 output/capture input.
	EPWM0_3	I/O	MPF5	PWM0_3 output/capture input.
	EBI_A19	O	MPF7	EBI address bus bit19.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
58	PA.10	I/O	MFP0	General purpose digital I/O pin.
	SC0_DAT	I/O	MPF2	SmartCard0 data pin.
	SPI3_MOSI0	I/O	MPF3	1st SPI3 MOSI (Master Out, Slave In) pin.
	PWM1_0	I/O	MPF4	PWM1_0 output/capture input.
	EPWM0_2	I/O	MPF5	PWM0_2 output/capture input.
	EBI_A20	O	MPF7	EBI address bus bit20.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
59	PA.11	I/O	MFP0	General purpose digital I/O pin.

	UART0_RTS	O	MPF1	Request to Send output pin for UART0.
	SPI3_MISO1	I/O	MPF3	2nd SPI3 MISO (Master In, Slave Out) pin.
	PWM0_5	I/O	MPF4	PWM0_5 output/capture input.
	EPWM0_1	I/O	MPF5	PWM0_1 output/capture input.
	EBI_AD0	O	MPF7	EBI address/data bus bit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
60	PA.12	I/O	MFP0	General purpose digital I/O pin.
	UART0_CTS	I	MPF1	Clear to Send input pin for UART0.
	SPI3_MOSI1	I/O	MPF3	2nd SPI3 MOSI (Master Out, Slave In) pin.
	PWM0_4	I/O	MPF4	PWM0_4 output/capture input.
	EPWM0_0	I/O	MPF5	PWM0_0 output/capture input.
	EBI_AD1	O	MPF7	EBI address/data bus bit 1.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
61	PA.13	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MPF1	Data receiver input pin for UART0.
	SC3_DAT	I/O	MPF3	SmartCard3 data pin.
	PWM1_4	I/O	MPF4	PWM1_4 output/capture input.
	EBI_AD2	O	MPF7	EBI address/data bus bit 2.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
62	PA.14	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MPF1	Data transmitter output pin for UART0.
	SC3_CLK	O	MPF3	SmartCard3 clock pin.
	PWM1_5	I/O	MPF4	PWM1_5 output/capture input.
	EBI_AD3	O	MPF7	EBI address/data bus bit 3.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
63	PD.10	I/O	MFP0	General purpose digital I/O pin.

	SC3_DAT	I/O	MPF1	SmartCard3 data pin.
	I2C4_SCL	I/O	MPF2	I2C4 clock pin.
64	PD.11	I/O	MFP0	General purpose digital I/O pin.
	SC3_RST	O	MPF1	SmartCard3 reset pin.
	TM3_CNT_OUT	I/O	MPF3	Timer3 event counter input/toggle output.
65	PD.12	I/O	MFP0	General purpose digital I/O pin.
	SC3_CLK	O	MPF1	SmartCard3 clock pin.
	I2C4_SDA	I/O	MPF2	I2C4 data input/output pin.
66	PA.15	I/O	MFP0	General purpose digital I/O pin.
	SC3_PWR	O	MPF1	SmartCard3 power pin.
	UART2_RTS	O	MPF2	Request to Send output pin for UART2.
	I2C0_SCL	I/O	MPF4	I2C0 clock pin.
	EBI_A21	O	MPF7	EBI address bus bit21.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
67	PC.9	I/O	MFP0	General purpose digital I/O pin.
	STADC	A	MPF1	ADC analog input.
	UART2_CTS	I	MPF2	Clear to Send input pin for UART2.
	SC3_RST	O	MPF3	SmartCard3 reset pin.
	I2C0_SDA	I/O	MPF4	I2C0 data input/output pin.
	CAP_DATA1	I	MPF5	Image data input bus bit 1.
	I2C3_SCL	I/O	MPF6	I2C3 clock pin.
	EBI_A22	O	MPF7	EBI address bus bit22.
	SD1_DAT0	I/O	MPF8	SD mode #1 data line bit 0.
	EBI_A6	O	MPF9	EBI address bus bit6.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
68	PC.10	I/O	MFP0	General purpose digital I/O pin.
	SC3_CD	I	MPF1	SmartCard3 card detect pin.

	UART2_RXD	I	MPF2	Data receiver input pin for UART2.
	PWM0_2	I/O	MPF4	PWM0_2 output/capture input.
	EBI_A23	O	MPF6	EBI address bus bit23.
	EBI_AD2	O	MPF7	EBI address/data bus bit 2.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
69	PC.11	I/O	MFP0	General purpose digital I/O pin.
	UART2_TXD	O	MPF2	Data transmitter output pin for UART2.
	PWM0_3	I/O	MPF4	PWM0_3 output/capture input.
	EBI_A24	O	MPF6	EBI address bus bit24.
	EBI_AD3	O	MPF7	EBI address/data bus bit 3.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
70	LDO_CAP	P	MFP0	LDO output pin. Note: This pin needs to be connected with a 1uF capacitor.
71	V_{SS}	P	MFP0	Ground pin for digital circuit.
72	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
73	PD.13	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS0	I/O	MPF1	1st SPI1 slave select pin.
	UART5_CTS	I	MPF2	Clear to Send input pin for UART5.
	ECAP0_IC2	O	MPF3	Input 2 of enhanced capture unit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
74	PD.14	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	O	MPF1	SPI1 serial clock pin.
	UART5_RTS	O	MPF2	Request to Send output pin for UART5.
	ECAP0_IC1	O	MPF3	Input 1 of enhanced capture unit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
75	PD.15	I/O	MFP0	General purpose digital I/O pin.

	SPI1_MISO0	I/O	MPF1	1st SPI1 MISO (Master In, Slave Out) pin.
	UART5_TXD	O	MPF2	Data transmitter output pin for UART5.
	ECAP0_IC0	O	MPF3	Input 0 of enhanced capture unit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
76	PF.0	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI0	I/O	MPF1	1st SPI1 MOSI (Master Out, Slave In) pin.
	UART5_RXD	I	MPF2	Data receiver input pin for UART5.
	INT5	I	MPF8	External interrupt5 input pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
77	VRES	A	MFP0	USB PHY VRES ground input pin. Add an 8.2K ohm resistor to VSSA.
78	VBUS	A	MFP0	USB PHY VBUS power input pin.
79	USB_VDD33_CAP	P	MFP0	Internal power regulator output 3.3V decoupling pin.
80	VSSA	P	MFP0	Ground pin for digital circuit. Add a Feritte Bead to digital ground V_{SS}.
81	USB0_D-	A	MFP0	USB0 differential signal D-.
82	USB0_D+	A	MFP0	USB0 differential signal D+.
83	USB0_OTG_ID	I	MFP0	USB0 OTG ID pin.
84	PB.0	I/O	MFP0	General purpose digital I/O pin.
	USB0_OTG5V_ST	I	MPF1	USB0 external VBUS regulator status
	I2C4_SCL	I/O	MPF2	I2C4 clock pin.
	INT1	I	MPF8	External interrupt1 input pin.
85	PB.1	I/O	MFP0	General purpose digital I/O pin.
	USB0_OTG5V_EN	O	MPF1	USB0 external VBUS regulator enabled
	I2C4_SDA	I/O	MPF2	I2C4 data input/output pin.
	TM1_CNT_OUT	I/O	MPF3	Timer1 event counter input/toggle output.
86	PG.7	I/O	MFP0	General purpose digital I/O pin.
	SPI2_MISO0	I/O	MPF1	1st SPI2 MISO (Master In, Slave Out) pin.

	I2S1_MCLK	O	MPF2	I2S1 master clock output pin.
	SC1_CD	I	MPF3	SmartCard1 card detect pin.
	SC3_RST	O	MPF4	SmartCard3 reset pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
87	PG.8	I/O	MFP0	General purpose digital I/O pin.
	SPI2_MOSI0	I/O	MPF1	1st SPI2 MOSI (Master Out, Slave In) pin.
	I2S1_DO	O	MPF2	I2S1 data output.
	UART4_RTS	O	MPF3	Request to Send output pin for UART4.
	SC3_DAT	I/O	MPF4	SmartCard3 data pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
88	PG.9	I/O	MFP0	General purpose digital I/O pin.
	SPI2_CLK	O	MPF1	SPI2 serial clock pin.
	I2S1_DI	I	MPF2	I2S1 data input.
	UART4_CTS	I	MPF3	Clear to Send input pin for UART4.
	SC3_CLK	O	MPF4	SmartCard3 clock pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
89	PB.2	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MPF1	Data receiver input pin for UART1.
	SPI2_SS0	I/O	MPF2	General purpose digital I/O pin.
	USB1_D-	A	MPF3	USB1 differential signal D-.
	EBI_AD4	O	MPF7	EBI address/data bus bit 4.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
90	PB.3	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MPF1	Data transmitter output pin for UART1.
	SPI2_CLK	O	MPF2	SPI2 serial clock pin.
	USB1_D+	A	MPF3	USB1 differential signal D+.

	EBI_AD5	O	MPF7	EBI address/data bus bit 5.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
91	PB.4	I/O	MFP0	General purpose digital I/O pin.
	UART1_RTS	O	MPF1	Request to Send output pin for UART1.
	SPI2_MISO0	I/O	MPF2	1st SPI2 MISO (Master In, Slave Out) pin.
	UART4_RXD	I	MPF3	Data receiver input pin for UART4.
	TM0_CNT_OUT	I/O	MPF4	Timer0 event counter input/toggle output.
	EBI_AD6	O	MPF7	EBI address/data bus bit 6.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
92	PB.5	I/O	MFP0	General purpose digital I/O pin.
	UART1_CTS	I	MPF1	Clear to Send input pin for UART1.
	SPI2_MOSI0	I/O	MPF2	1st SPI2 MOSI (Master Out, Slave In) pin.
	UART4_TXD	O	MPF3	Data transmitter output pin for UART4.
	EBI_AD7	O	MPF7	EBI address/data bus bit 7.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
93	PB.6	I/O	MFP0	General purpose digital I/O pin.
	I2C2_SCL	I/O	MPF1	I2C2 clock pin.
	BRAKE01	I	MPF2	Brake input pin 1 of EPWMB.
	UART4_RTS	O	MPF3	Request to Send output pin for UART4.
	PWM1_4	I/O	MPF4	PWM1_4 output/capture input.
	EPWM1_0	I/O	MPF5	PWM1_0 output/capture input.
	EBI_AD8	O	MPF7	EBI address/data bus bit 8.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
94	PB.7	I/O	MFP0	General purpose digital I/O pin.
	I2C2_SDA	I/O	MPF1	I2C2 data input/output pin.
	BRAKE00	I	MPF2	Brake input pin 0 of EPWMB.

	UART4_CTS	I	MPF3	Clear to Send input pin for UART4.
	PWM1_5	I/O	MPF4	PWM1_5 output/capture input.
	EPWM1_1	I/O	MPF5	PWM1_1 output/capture input.
	EBI_AD9	O	MPF7	EBI address/data bus bit 9.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
95	PB.8	I/O	MFP0	General purpose digital I/O pin.
	UART5_CTS	I	MPF1	Clear to Send input pin for UART5.
	EPWM1_2	I/O	MPF5	PWM1_2 output/capture input.
	EBI_AD10	O	MPF7	EBI address/data bus bit 10.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
96	PB.9	I/O	MFP0	General purpose digital I/O pin.
	UART5_RTS	O	MPF1	Request to Send output pin for UART5.
	EPWM1_3	I/O	MPF5	PWM1_3 output/capture input.
	EBI_AD11	O	MPF7	EBI address/data bus bit 11.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
97	PB.10	I/O	MFP0	General purpose digital I/O pin.
	UART5_TXD	O	MPF1	Data transmitter output pin for UART5.
	EPWM1_4	I/O	MPF5	PWM1_4 output/capture input.
	EBI_AD12	O	MPF7	EBI address/data bus bit 12.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
98	PB.11	I/O	MFP0	General purpose digital I/O pin.
	UART5_RXD	I	MPF1	Data receiver input pin for UART5.
	EPWM1_5	I/O	MPF5	PWM1_5 output/capture input.
	EBI_AD13	O	MPF7	EBI address/data bus bit 13.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
99	PH.0	I/O	MFP0	General purpose digital I/O pin.

	I2C1_SCL	I/O	MPF1	I2C1 clock pin.
	UART4_RXD	I	MPF2	Data receiver input pin for UART4.
	CAN1_RXD	I	MPF3	CAN bus receiver1 input.
	INT7	I	MPF8	External interrupt7 input pin.
100	PH.1	I/O	MFP0	General purpose digital I/O pin.
	UART4_TXD	O	MPF1	Data transmitter output pin for UART4.
	I2C1_SDA	I/O	MPF2	I2C1 data input/output pin.
	CAN1_TXD	I	MPF3	CAN bus transmitter1 input.
101	PB.12	I/O	MFP0	General purpose digital I/O pin.
	UART4_RTS	O	MPF1	Request to Send output pin for UART4.
	SPI2_MISO1	I/O	MPF2	2nd SPI2 MISO (Master In, Slave Out) pin.
	CAN0_RXD	I	MPF3	CAN bus receiver0 input.
	EBI_AD14	O	MPF7	EBI address/data bus bit 14.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
102	PB.13	I/O	MFP0	General purpose digital I/O pin.
	UART4_CTS	I	MPF1	Clear to Send input pin for UART4.
	SPI2_MOSI1	I/O	MPF2	2nd SPI2 MOSI (Master Out, Slave In) pin.
	CAN0_TXD	I	MPF3	CAN bus transmitter0 input.
	EBI_AD15	O	MPF7	EBI address/data bus bit 15.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
103	PB.14	I/O	MFP0	General purpose digital I/O pin.
	I2S1_MCLK	O	MPF1	I2S1 master clock output pin.
	SC1_RST	O	MPF2	SmartCard1 reset pin.
	BRAKE01	I	MPF4	Brake input pin 1 of EPWMB.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
104	PB.15	I/O	MFP0	General purpose digital I/O pin.

	I2S1_DO	O	MPF1	I2S1 data output.
	SC1_DAT	I/O	MPF2	SmartCard1 data pin.
	BRAKE00	I	MPF4	Brake input pin 0 of EPWMB.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
105	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
106	V_{SS}	P	MFP0	Ground pin for digital circuit.
107	LDO_CAP	P	MFP0	LDO output pin. Note: This pin needs to be connected with a 1uF capacitor.
108	PC.0	I/O	MFP0	General purpose digital I/O pin.
	I2S1_DI	I	MPF1	I2S1 data input.
	SC1_DAT	I/O	MPF2	SmartCard1 data pin.
	UART4_RXD	I	MPF3	Data receiver input pin for UART4.
	EBI_MCLK	O	MPF7	EBI interface clock output pin.
	INT2	I	MPF8	External interrupt2 input pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
109	PC.1	I/O	MFP0	General purpose digital I/O pin.
	I2S1_BCLK	O	MPF1	I2S1 bit clock pin.
	SC1_CLK	O	MPF2	SmartCard1 clock pin.
	UART4_TXD	O	MPF3	Data transmitter output pin for UART4.
	TM3_CNT_OUT	I/O	MPF5	Timer3 event counter input/toggle output.
	EBI_AD13	O	MPF7	EBI address/data bus bit 13.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
110	PC.2	I/O	MFP0	General purpose digital I/O pin.
	I2S1_LRCK	O	MPF1	I2S1 left right channel clock.
	SC1_PWR	O	MPF2	SmartCard1 power pin.
	UART4_RTS	O	MPF3	Request to Send output pin for UART4.

	SPI0_SS0	I/O	MPF4	General purpose digital I/O pin.
	EBI_AD12	O	MPF7	EBI address/data bus bit 12.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
111	PC.3	I/O	MFP0	General purpose digital I/O pin.
	I2S1_MCLK	O	MPF1	I2S1 master clock output pin.
	SC1_CD	I	MPF2	SmartCard1 card detect pin.
	UART4_CTS	I	MPF3	Clear to Send input pin for UART4.
	SPI0_MISO1	I/O	MPF4	2nd SPI0 MISO (Master In, Slave Out) pin.
	QEI0_Z	I	MPF5	Quadrature encoder phase Z input of QEI Unit 0.
	EBI_AD11	O	MPF7	EBI address/data bus bit 11.
	ECAP0_IC2	O	MPF8	Input 2 of enhanced capture unit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
112	PC.4	I/O	MFP0	General purpose digital I/O pin.
	I2S1_DO	O	MPF1	I2S1 data output.
	SC1_RST	O	MPF2	SmartCard1 reset pin.
	SPI0_MOSI1	I/O	MPF4	2nd SPI0 MOSI (Master Out, Slave In) pin.
	QEI0_B	I	MPF5	Quadrature encoder phase B input of QEI Unit 0.
	EBI_AD10	O	MPF7	EBI address/data bus bit 10.
	ECAP0_IC1	O	MPF8	Input 1 of enhanced capture unit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
113	PC.5	I/O	MFP0	General purpose digital I/O pin.
	CLKO	O	MFP1	Clock Output Pin.
	QEI0_A	I	MPF5	Quadrature encoder phase A input of QEI Unit 0.
	EBI_MCLK	O	MPF7	EBI interface clock output pin.
	ECAP0_IC0	O	MPF8	Input 0 of enhanced capture unit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.

114	PC.6	I/O	MFP0	General purpose digital I/O pin.
	TM2_EXT	I	MPF1	Timer2 external counter input
	SPI0_MISO0	I/O	MPF4	1st SPI0 MISO (Master In, Slave Out) pin.
	TM2_CNT_OUT	I/O	MPF5	Timer2 event counter input/toggle output.
	EBI_AD9	O	MPF7	EBI address/data bus bit 9.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
115	PC.7	I/O	MFP0	General purpose digital I/O pin.
	TM1_EXT	I	MPF1	Timer1 external counter input
	SPI0_MOSI0	I/O	MPF4	1st SPI0 MOSI (Master Out, Slave In) pin.
	EBI_AD8	O	MPF7	EBI address/data bus bit 8.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
116	PC.8	I/O	MFP0	General purpose digital I/O pin.
	TM0_EXT	I	MPF1	Timer0 external counter input
	SPI0_CLK	O	MPF4	SPI0 serial clock pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
117	PF.2	I/O	MFP0	General purpose digital I/O pin.
	SPI3_SS0	I/O	MPF1	General purpose digital I/O pin.
	SD0_DAT3	I/O	MPF4	SD mode #0 data line bit 3.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
118	PF.3	I/O	MFP0	General purpose digital I/O pin.
	SPI3_CLK	O	MPF1	SPI3 serial clock pin.
	SD0_DAT2	I/O	MPF4	SD mode #0 data line bit 2.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
119	PF.4	I/O	MFP0	General purpose digital I/O pin.
	SPI3_MISO0	I/O	MPF1	1st SPI3 MISO (Master In, Slave Out) pin.
	SD0_DAT1	I/O	MPF4	SD mode #0 data line bit 1.

	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
120	PF.5	I/O	MFP0	General purpose digital I/O pin.
	SPI3_MOSI0	I/O	MPF1	1st SPI3 MOSI (Master Out, Slave In) pin.
	SD0_DAT0	I/O	MPF4	SD mode #0 data line bit 0.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
121	V_{SS}	P	MFP0	Ground pin for digital circuit.
122	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
123	PF.6	I/O	MFP0	General purpose digital I/O pin.
	UART2_RXD	I	MPF1	Data receiver input pin for UART2.
	SD0_CDn	I	MPF4	SD mode #0 – card detect
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
124	PF.7	I/O	MFP0	General purpose digital I/O pin.
	UART2_TXD	O	MPF1	Data transmitter output pin for UART2.
	SD0_CMD	I/O	MPF4	SD mode #0 – command/response
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
125	PF.8	I/O	MFP0	General purpose digital I/O pin.
	UART2_RTS	O	MPF1	Request to Send output pin for UART2.
	SD0_CLK	O	MPF4	SD mode #0– clock.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
126	PH.2	I/O	MFP0	General purpose digital I/O pin.
	UART2_CTS	I	MPF1	Clear to Send input pin for UART2.
127	LDO_CAP	P	MFP0	LDO output pin. Note: This pin needs to be connected with a 1uF capacitor.
128	V_{SS}	P	MFP0	Ground pin for digital circuit.
129	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.

130	PE.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_0	A	MPF1	ADC0 analog input.
	INT4	I	MPF8	External interrupt4 input pin.
131	PE.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_1	A	MPF1	ADC0 analog input.
	TM2_CNT_OUT	I/O	MPF3	Timer2 event counter input/toggle output.
132	PE.2	I/O	MFP0	General purpose digital I/O pin.
	ADC0_2	A	MPF1	ADC0 analog input.
	ACMP0_O	O	MPF2	Analog comparator0 output .
	SPI0_MISO0	I/O	MPF3	1st SPI0 MISO (Master In, Slave Out) pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
133	PE.3	I/O	MFP0	General purpose digital I/O pin.
	ADC0_3	A	MPF1	ADC0 analog input.
	ACMP0_P3	A	MPF2	Analog comparator0 positive input pin.
	SPI0_MOSI0	I/O	MPF3	1st SPI0 MOSI (Master Out, Slave In) pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
134	PE.4	I/O	MFP0	General purpose digital I/O pin.
	ADC0_4	A	MPF1	ADC0 analog input.
	ACMP0_P2	A	MPF2	Analog comparator0 positive input pin.
	SPI0_SS0	I/O	MPF3	General purpose digital I/O pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
135	PE.5	I/O	MFP0	General purpose digital I/O pin.
	ADC0_5	A	MPF1	ADC0 analog input.
	ACMP0_P1	A	MPF2	Analog comparator0 positive input pin.
	SPI0_CLK	O	MPF3	SPI0 serial clock pin.
	SD0_CDn	I	MPF4	SD mode #0 – card detect

	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
136	PE.6	I/O	MFP0	General purpose digital I/O pin.
	ADC0_6	A	MPF1	ADC0 analog input.
	ACMP0_P0	A	MPF2	Analog comparator0 positive input pin.
	SPI0_MISO0	I/O	MPF3	1st SPI0 MISO (Master In, Slave Out) pin.
	SD0_CMD	I/O	MPF4	SD mode #0 – command/response
	EBI_nWR	O	MPF7	EBI write enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
137	PE.7	I/O	MFP0	General purpose digital I/O pin.
	ADC0_7	A	MPF1	ADC0 analog input.
	ACMP0_N	A	MPF2	Analog comparator0 negative input pin.
	SPI0_MOSI0	I/O	MPF3	1st SPI0 MOSI (Master Out, Slave In) pin.
	SD0_CLK	O	MPF4	SD mode #0– clock.
	EBI_nRD	O	MPF7	EBI read enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
138	AV_{SS}	P	MFP0	Ground pin for digital circuit.
139	V_{REF}	A	MFP0	Voltage reference input for ADC. Note: This pin needs to be connected with 0.1uF/10uF capacitors.
140	AV_{DD}	P	MFP0	Power supply for internal analog circuit.
141	PE.8	I/O	MFP0	General purpose digital I/O pin.
	ADC1_0	A	MPF1	ADC1 analog input.
	ADC0_8	A	MPF1	ADC0 analog input.
	ACMP1_N	A	MPF2	Analog comparator1 negative input pin.
	TM1_CNT_OUT	I/O	MPF3	Timer1 event counter input/toggle output.
	SD0_DAT3	I/O	MPF4	SD mode #0 data line bit 3.
	EBI_ALE	O	MPF7	EBI address latch enable output pin.

	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
142	PE.9	I/O	MFP0	General purpose digital I/O pin.
	ADC1_1	A	MPF1	ADC1 analog input.
	ADC0_9	A	MPF1	ADC0 analog input.
	ACMP1_P0	A	MPF2	Analog comparator1 positive input pin.
	SD0_DAT2	I/O	MPF4	SD mode #0 data line bit 2.
	EBI_nWRH	O	MPF7	EBI write enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
143	PE.10	I/O	MFP0	General purpose digital I/O pin.
	ADC1_2	A	MPF1	ADC1 analog input.
	ADC0_10	A	MPF1	ADC0 analog input.
	ACMP1_P1	A	MPF2	Analog comparator1 positive input pin.
	SPI0_MISO1	I/O	MPF3	2nd SPI0 MISO (Master In, Slave Out) pin.
	SD0_DAT1	I/O	MPF4	SD mode #0 data line bit 1.
	EBI_nWRL	O	MPF7	EBI write enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.
144	PE.11	I/O	MFP0	General purpose digital I/O pin.
	ADC1_3	A	MPF1	ADC1 analog input.
	ADC0_11	A	MPF1	ADC0 analog input.
	ACMP1_P2	A	MPF2	Analog comparator1 positive input pin.
	SPI0_MOSI1	I/O	MPF3	2nd SPI0 MOSI (Master Out, Slave In) pin.
	SD0_DAT0	I/O	MPF4	SD mode #0 data line bit 0.
	ACMP2_P3	A	MPF5	Analog comparator2 positive input pin.
	EBI_nCS0	O	MPF7	EBI chip select 0 enable output pin.
	HS		Slew	This pad is embedded with “Slew Rate Control” capability.

Note: Pin Type I = Digital Input, O = Digital Output; A = Analog Pin; P = Power Pin

4.3.5 Summary GPIO Multi-function Pin Description

MFP* = Multi-function pin. (Reference section 6.2.5 of TRM)

MFP 0	MPF1	MPF2	MPF3	MPF4	MPF5	MPF6	MPF7	MPF8	MPF9	Other	Slew
PA.0	TAMPER0	SC0_CD	CAN1_RXD					INT0			
PA.1	TAMPER1	SC5_CD	CAN1_TXD				EBI_A22				
PA.2	SC2_DAT	SPI3_MISO0	I2S0_MCLK	BRAKE11	CAP_SFIELD		EBI_A12				HS
PA.3	SC2_CLK	SPI3_MOSI0	I2S0_DO	BRAKE10			EBI_A13				HS
PA.4	SC2_PWR	SPI3_CLK	I2S0_DI		QEI1_Z		EBI_A14	ECAP1_IC2			HS
PA.5	SC2_RST	SPI3_SS0	I2S0_BCLK	PWM0_0	QEI1_B		EBI_A15	ECAP1_IC1			HS
PA.6	SC2_CD		I2S0_LRCK	PWM0_1	QEI1_A	CAN1_TXD	EBI_A16	ECAP1_IC0			HS
PA.7		SC0_CLK	SPI3_SS0	PWM1_3	EPWM0_5		EBI_A17				HS
PA.8		SC0_RST	SPI3_CLK	PWM1_2	EPWM0_4		EBI_A18				HS
PA.9		SC0_PWR	SPI3_MISO0	PWM1_1	EPWM0_3		EBI_A19				HS
PA.10		SC0_DAT	SPI3_MOSI0	PWM1_0	EPWM0_2		EBI_A20				HS
PA.11	UART0_RTS		SPI3_MISO1	PWM0_5	EPWM0_1		EBI_AD0				HS
PA.12	UART0_CTS		SPI3_MOSI1	PWM0_4	EPWM0_0		EBI_AD1				HS
PA.13	UART0_RXD		SC3_DAT	PWM1_4			EBI_AD2				HS
PA.14	UART0_TXD		SC3_CLK	PWM1_5			EBI_AD3				HS
PA.15	SC3_PWR	UART2_RTS		I2C0_SCL			EBI_A21				HS
PB.0	USB0_OTG5V_ST	I2C4_SCL						INT1			
PB.1	USB0_OTG5V_EN	I2C4_SDA	TM1_CNT_OUT								
PB.2	UART1_RXD	SPI2_SS0	USB1_D-				EBI_AD4				HS
PB.3	UART1_TXD	SPI2_CLK	USB1_D+				EBI_AD5				HS
PB.4	UART1_RTS	SPI2_MISO0	UART4_RXD	TM0_CNT_OUT			EBI_AD6				HS
PB.5	UART1_CTS	SPI2_MOSI0	UART4_TXD				EBI_AD7				HS
PB.6	I2C2_SCL	BRAKE01	UART4_RTS	PWM1_4	EPWM1_0		EBI_AD8				HS

PB.7	I2C2_SDA	BRAKE00	UART4_CTS	PWM1_5	EPWM1_1		EBI_AD9				HS
PB.8	UART5_CTS				EPWM1_2		EBI_AD10				HS
PB.9	UART5_RTS				EPWM1_3		EBI_AD11				HS
PB.10	UART5_TXD				EPWM1_4		EBI_AD12				HS
PB.11	UART5_RXD				EPWM1_5		EBI_AD13				HS
PB.12	UART4_RTS	SPI2_MISO1	CAN0_RXD				EBI_AD14				HS
PB.13	UART4_CTS	SPI2_MOSI1	CAN0_TXD				EBI_AD15				HS
PB.14	I2S1_MCLK	SC1_RST		BRAKE01							HS
PB.15	I2S1_DO	SC1_DAT		BRAKE00							HS
PC.0	I2S1_DI	SC1_DAT	UART4_RXD				EBI_MCLK	INT2			HS
PC.1	I2S1_BCLK	SC1_CLK	UART4_TXD		TM3_CNT_OUT		EBI_AD13				HS
PC.2	I2S1_LRCK	SC1_PWR	UART4_RTS	SPI0_SS0			EBI_AD12				HS
PC.3	I2S1_MCLK	SC1_CD	UART4_CTS	SPI0_MISO1	QEI0_Z		EBI_AD11	ECAP0_IC2			HS
PC.4	I2S1_DO	SC1_RST		SPI0_MOSI1	QEI0_B		EBI_AD10	ECAP0_IC1			HS
PC.5	CLKO				QEI0_A		EBI_MCLK	ECAP0_IC0			HS
PC.6	TM2_EXT			SPI0_MISO0	TM2_CNT_OUT		EBI_AD9				HS
PC.7	TM1_EXT			SPI0_MOSI0			EBI_AD8				HS
PC.8	TM0_EXT			SPI0_CLK							HS
PC.9	STADC	UART2_CTS	SC3_RST	I2C0_SDA	CAP_DATA1	I2C3_SCL	EBI_A22	SD1_DAT0	EBI_A6		HS
PC.10	SC3_CD	UART2_RXD		PWM0_2		EBI_A23	EBI_AD2				HS
PC.11		UART2_TXD		PWM0_3		EBI_A24	EBI_AD3				HS
PC.12	SPI1_SS0	SC4_CD		SD1_CDn	CAP_DATA7		EBI_A0				HS
PC.13	SPI1_MOSI1	SC4_RST		SD1_CMD	CAP_DATA6		EBI_A1				HS
PC.14	SPI1_MISO1	SC4_PWR	TM3_EXT	SD1_CLK	CAP_DATA5		EBI_A2				HS

PC.15	SPI1_MOSI0	SC4_DAT		SD1_DAT3	CAP_DATA4		EBI_A3				HS
PD.0	SPI1_MISO0	SC4_CLK		SD1_DAT2	CAP_DATA3		EBI_A4	INT3			HS
PD.1	SPI1_CLK		TM0_CNT_OUT	SD1_DAT1	CAP_DATA2		EBI_A5				HS
PD.2	STADC	I2C3_SCL		SD1_DAT0	CAP_DATA1		EBI_A6				HS
PD.3	SC5_CLK	I2C3_SDA	ACMP2_O	SD0_CDn	CAP_DATA0		EBI_A7				HS
PD.4	SC5_CD	UART3_RXD	ACMP1_O		CAP_SCLK		EBI_A8				HS
PD.5	SC5_RST	UART3_TXD			CAP_VSYNC		EBI_A9				HS
PD.6	SC5_PWR	UART3_RTS		SD0_CMD	CAP_HSYNC		EBI_A10				HS
PD.7	SC5_DAT	UART3_CTS		SD0_CLK	CAP_PIXCLK		EBI_A11				HS
PD.8	SPI3_MISO1	I2C0_SCL									HS
PD.9	SPI3_MOSI1	I2C0_SDA									HS
PD.10	SC3_DAT	I2C4_SCL									
PD.11	SC3_RST		TM3_CNT_OUT								
PD.12	SC3_CLK	I2C4_SDA									
PD.13	SPI1_SS0	UART5_CTS	ECAP0_IC2								HS
PD.14	SPI1_CLK	UART5_RTS	ECAP0_IC1								HS
PD.15	SPI1_MISO0	UART5_TXD	ECAP0_IC0								HS
PE.0	ADC0_0							INT4			
PE.1	ADC0_1		TM2_CNT_OUT								
PE.2	ADC0_2	ACMP0_O	SPI0_MISO0								HS
PE.3	ADC0_3	ACMP0_P3	SPI0_MOSI0								HS
PE.4	ADC0_4	ACMP0_P2	SPI0_SS0								HS
PE.5	ADC0_5	ACMP0_P1	SPI0_CLK	SD0_CDn							HS
PE.6	ADC0_6	ACMP0_P0	SPI0_MISO0	SD0_CMD			EBI_nWR				HS
PE.7	ADC0_7	ACMP0_N	SPI0_MOSI0	SD0_CLK			EBI_nRD				HS

PE.8	ADC1_0/ ADC0_8	ACMP1_N	TM1_CNT_OUT	SD0_DAT3			EBI_ALE				HS
PE.9	ADC1_1/ADC0_9	ACMP1_P0		SD0_DAT2			EBI_nWRH				HS
PE.10	ADC1_2/ADC0_10	ACMP1_P1	SPI0_MISO1	SD0_DAT1			EBI_nWRL				HS
PE.11	ADC1_3/ADC0_11	ACMP1_P2	SPI0_MOSI1	SD0_DAT0	ACMP2_P3		EBI_nCS0				HS
PE.12	ADC1_4	ACMP1_P3	ACMP2_P2				EBI_nCS1				HS
PE.13	ADC1_5		ACMP2_P1				EBI_nCS2				HS
PE.14	ADC1_6		ACMP2_P0				EBI_nCS3				HS
PE.15	ADC1_7		ACMP2_N								
PF.0	SPI1_MOSI0	UART5_RXD						INT5			HS
PF.1	SPI2_MOSI1										HS
PF.2	SPI3_SS0			SD0_DAT3							HS
PF.3	SPI3_CLK			SD0_DAT2							HS
PF.4	SPI3_MISO0			SD0_DAT1							HS
PF.5	SPI3_MOSI0			SD0_DAT0							HS
PF.6	UART2_RXD			SD0_CDn							HS
PF.7	UART2_TXD			SD0_CMD							HS
PF.8	UART2_RTS			SD0_CLK							HS
PF.9	OPA0_P			PWM0_0							HS
PF.10	OPA0_N			PWM0_1							HS
PF.11	OPA0_O	UART1_RTS									
PF.12	OPA1_P	UART1_CTS									
PF.13	OPA1_N	UART1_TXD									
PF.14	OPA1_O	UART1_RXD									
PF.15	UART0_RTS										
PG.0	UART0_CTS							INT6			
PG.1	UART0_RXD										

PG.2	UART0_TXD										
PG.3	PS2_CLK	I2S1_DO	SC1_RST								
PG.4	PS2_DAT	I2S1_DI	SC1_PWR								
PG.5		I2S1_BCLK	SC1_DAT								
PG.6		I2S1_LRCK	SC1_CLK								
PG.7	SPI2_MISO0	I2S1_MCLK	SC1_CD	SC3_RST							HS
PG.8	SPI2_MOSI0	I2S1_DO	UART4_RTS	SC3_DAT							HS
PG.9	SPI2_CLK	I2S1_DI	UART4_CTS	SC3_CLK							HS
PG.10	ICE_CLK										
PG.11	ICE_DAT										
PG.12	XT1_OUT										
PG.13	XT1_IN										
PG.14	X32K_OUT		I2C1_SDA								
PG.15	X32K_IN		I2C1_SCL								
PH.0	I2C1_SCL	UART4_RXD	CAN1_RXD					INT7			
PH.1	UART4_TXD	I2C1_SDA	CAN1_TXD								
PH.2	UART2_CTS										
PH.3	I2C3_SCL										
PH.4	I2C3_SDA										
PH.5	SPI2_SS0										HS
PH.6	SPI2_CLK										HS
PH.7	SPI2_MISO0										HS
PH.8	SPI2_MOSI0										HS
PH.9	SPI2_MISO1										HS
PH.10	SPI2_MOSI1										HS
PH.11	UART3_RXD										
PH.12	UART3_TXD										
PH.13	UART3_RTS										

PH.14	UART3_CTS										
PH.15		SC5_CLK									
PI.0		SC5_RST									
PI.1		SC5_PWR									
PI.2	SC5_DAT										
PI.3	SPI3_SS0										HS
PI.4	SPI3_CLK										HS
PI.5	SPI3_MISO0										HS
PI.6	SPI3_MOSI0										HS
PI.7	I2C2_SCL	SPI3_MISO1									HS
PI.8	I2C2_SDA	SPI3_MOSI1									HS
PI.9				I2C4_SCL							
PI.10											
PI.11	SPI2_SS0	I2S1_BCLK	I2C4_SCL	SC3_PWR							HS
PI.12	SPI2_MISO1	I2S1_LRCK	I2C4_SDA	SC3_CD							
PI.13											
PI.14											
PI.15											

Note: PA.0* = TAMPER0 PA.1* = TAMPER1

4.3.6 Summary Function Pin Description

Group	Pin Name	GPIO	*MFP	Type	Description
ACMP0	ACMP0_N	PE.7	MPF2	A	Analog comparator0 negative input pin.
ACMP0	ACMP0_O	PE.2	MPF2	O	Analog comparator0 output.
ACMP0	ACMP0_P0	PE.6	MPF2	A	Analog comparator0 positive input pin.
ACMP0	ACMP0_P1	PE.5	MPF2	A	Analog comparator0 positive input pin.
ACMP0	ACMP0_P2	PE.4	MPF2	A	Analog comparator0 positive input pin.
ACMP0	ACMP0_P3	PE.3	MPF2	A	Analog comparator0 positive input pin.
ACMP1	ACMP1_N	PE.8	MPF2	A	Analog comparator1 negative input pin.
ACMP1	ACMP1_O	PD.4	MPF3	O	Analog comparator1 output.
ACMP1	ACMP1_P0	PE.9	MPF2	A	Analog comparator1 positive input pin.
ACMP1	ACMP1_P1	PE.10	MPF2	A	Analog comparator1 positive input pin.
ACMP1	ACMP1_P2	PE.11	MPF2	A	Analog comparator1 positive input pin.
ACMP1	ACMP1_P3	PE.12	MPF2	A	Analog comparator1 positive input pin.
ACMP2	ACMP2_N	PE.15	MPF3	A	Analog comparator2 negative input pin.
ACMP2	ACMP2_O	PD.3	MPF3	O	Analog comparator2 output.
ACMP2	ACMP2_P0	PE.14	MPF3	A	Analog comparator2 positive input pin.
ACMP2	ACMP2_P1	PE.13	MPF3	A	Analog comparator2 positive input pin.
ACMP2	ACMP2_P2	PE.12	MPF3	A	Analog comparator2 positive input pin.
ACMP2	ACMP2_P3	PE.11	MPF5	A	Analog comparator2 positive input pin.
ADC0	ADC0_0	PE.0	MPF1	A	ADC0 analog input.
ADC0	ADC0_1	PE.1	MPF1	A	ADC0 analog input.
ADC0	ADC0_10	PE.10	MPF1	A	ADC0 analog input.
ADC0	ADC0_11	PE.11	MPF1	A	ADC0 analog input.
ADC0	ADC0_2	PE.2	MPF1	A	ADC0 analog input.
ADC0	ADC0_3	PE.3	MPF1	A	ADC0 analog input.
ADC0	ADC0_4	PE.4	MPF1	A	ADC0 analog input.
ADC0	ADC0_5	PE.5	MPF1	A	ADC0 analog input.
ADC0	ADC0_6	PE.6	MPF1	A	ADC0 analog input.
ADC0	ADC0_7	PE.7	MPF1	A	ADC0 analog input.
ADC0	ADC0_8	PE.8	MPF1	A	ADC0 analog input.
ADC0	ADC0_9	PE.9	MPF1	A	ADC0 analog input.
ADC0	STADC	PD.2	MPF1	A	ADC analog input.
ADC1	ADC1_0	PE.8	MPF1	A	ADC1 analog input.
ADC1	ADC1_1	PE.9	MPF1	A	ADC1 analog input.

ADC1	ADC1_2	PE.10	MPF1	A	ADC1 analog input.
ADC1	ADC1_3	PE.11	MPF1	A	ADC1 analog input.
ADC1	ADC1_4	PE.12	MPF1	A	ADC1 analog input.
ADC1	ADC1_5	PE.13	MPF1	A	ADC1 analog input.
ADC1	ADC1_6	PE.14	MPF1	A	ADC1 analog input.
ADC1	ADC1_7	PE.15	MPF1	A	ADC1 analog input.
BPWMA	PWM0_0	PA.5	MPF4	I/O	PWM0_0 output/capture input.
BPWMA	PWM0_0	PF.9	MPF4	I/O	PWM0_0 output/capture input.
BPWMA	PWM0_1	PA.6	MPF4	I/O	PWM0_1 output/capture input.
BPWMA	PWM0_1	PF.10	MPF4	I/O	PWM0_1 output/capture input.
BPWMA	PWM0_2	PC.10	MPF4	I/O	PWM0_2 output/capture input.
BPWMA	PWM0_3	PC.11	MPF4	I/O	PWM0_3 output/capture input.
BPWMA	PWM0_4	PA.12	MPF4	I/O	PWM0_4 output/capture input.
BPWMA	PWM0_5	PA.11	MPF4	I/O	PWM0_5 output/capture input.
BPWMB	PWM1_0	PA.10	MPF4	I/O	PWM1_0 output/capture input.
BPWMB	PWM1_1	PA.9	MPF4	I/O	PWM1_1 output/capture input.
BPWMB	PWM1_2	PA.8	MPF4	I/O	PWM1_2 output/capture input.
BPWMB	PWM1_3	PA.7	MPF4	I/O	PWM1_3 output/capture input.
BPWMB	PWM1_4	PA.13	MPF4	I/O	PWM1_4 output/capture input.
BPWMB	PWM1_4	PB.6	MPF4	I/O	PWM1_4 output/capture input.
BPWMB	PWM1_5	PA.14	MPF4	I/O	PWM1_5 output/capture input.
BPWMB	PWM1_5	PB.7	MPF4	I/O	PWM1_5 output/capture input.
BRAKE	BRAKE00	PB.7	MPF2	I	Brake input pin 0 of EPWMB.
BRAKE	BRAKE00	PB.15	MPF4	I	Brake input pin 0 of EPWMB.
BRAKE	BRAKE01	PB.6	MPF2	I	Brake input pin 1 of EPWMB.
BRAKE	BRAKE01	PB.14	MPF4	I	Brake input pin 1 of EPWMB.
BRAKE	BRAKE10	PA.3	MPF4	I	Brake input pin 0 of EPWMA.
BRAKE	BRAKE11	PA.2	MPF4	I	Brake input pin 1 of EPWMA.
CAN0	CAN0_RXD	PB.12	MPF3	I	CAN bus receiver0 input.
CAN0	CAN0_TXD	PB.13	MPF3	I	CAN bus transmitter0 input.
CAN1	CAN1_RXD	PA.0	MPF3	I	CAN bus receiver1 input.
CAN1	CAN1_RXD	PH.0	MPF3	I	CAN bus receiver1 input.
CAN1	CAN1_TXD	PA.1	MPF3	I	CAN bus transmitter1 input.
CAN1	CAN1_TXD	PA.6	MPF6	I	CAN bus transmitter1 input.
CAN1	CAN1_TXD	PH.1	MPF3	I	CAN bus transmitter1 input.

CLKO	CLKO	PC.5	MPF1	O	Clock Output Pin.
EBI	EBI_A0	PC.12	MPF7	O	EBI address bus bit0.
EBI	EBI_A1	PC.13	MPF7	O	EBI address bus bit1.
EBI	EBI_A10	PD.6	MPF7	O	EBI address bus bit10.
EBI	EBI_A11	PD.7	MPF7	O	EBI address bus bit11.
EBI	EBI_A12	PA.2	MPF7	O	EBI address bus bit12.
EBI	EBI_A13	PA.3	MPF7	O	EBI address bus bit13.
EBI	EBI_A14	PA.4	MPF7	O	EBI address bus bit14.
EBI	EBI_A15	PA.5	MPF7	O	EBI address bus bit15.
EBI	EBI_A16	PA.6	MPF7	O	EBI address bus bit16.
EBI	EBI_A17	PA.7	MPF7	O	EBI address bus bit17.
EBI	EBI_A18	PA.8	MPF7	O	EBI address bus bit18.
EBI	EBI_A19	PA.9	MPF7	O	EBI address bus bit19.
EBI	EBI_A2	PC.14	MPF7	O	EBI address bus bit2.
EBI	EBI_A20	PA.10	MPF7	O	EBI address bus bit20.
EBI	EBI_A21	PA.15	MPF7	O	EBI address bus bit21.
EBI	EBI_A22	PC.9	MPF7	O	EBI address bus bit22.
EBI	EBI_A23	PC.10	MPF6	O	EBI address bus bit23.
EBI	EBI_A24	PC.11	MPF6	O	EBI address bus bit24.
EBI	EBI_A3	PC.15	MPF7	O	EBI address bus bit3.
EBI	EBI_A4	PD.0	MPF7	O	EBI address bus bit4.
EBI	EBI_A5	PD.1	MPF7	O	EBI address bus bit5.
EBI	EBI_A6	PD.2	MPF7	O	EBI address bus bit6.
EBI	EBI_A7	PD.3	MPF7	O	EBI address bus bit7.
EBI	EBI_A8	PD.4	MPF7	O	EBI address bus bit8.
EBI	EBI_A9	PD.5	MPF7	O	EBI address bus bit9.
EBI	EBI_AD0	PA.11	MPF7	O	EBI address/data bus bit 0.
EBI	EBI_AD1	PA.12	MPF7	O	EBI address/data bus bit 1.
EBI	EBI_AD10	PB.8	MPF7	O	EBI address/data bus bit 10.
EBI	EBI_AD10	PC.4	MPF7	O	EBI address/data bus bit 10.
EBI	EBI_AD11	PB.9	MPF7	O	EBI address/data bus bit 11.
EBI	EBI_AD11	PC.3	MPF7	O	EBI address/data bus bit 11.
EBI	EBI_AD12	PB.10	MPF7	O	EBI address/data bus bit 12.
EBI	EBI_AD12	PC.2	MPF7	O	EBI address/data bus bit 12.
EBI	EBI_AD13	PB.11	MPF7	O	EBI address/data bus bit 13.

EBI	EBI_AD13	PC.1	MPF7	O	EBI address/data bus bit 13.
EBI	EBI_AD14	PB.12	MPF7	O	EBI address/data bus bit 14.
EBI	EBI_AD15	PB.13	MPF7	O	EBI address/data bus bit 15.
EBI	EBI_AD2	PA.13	MPF7	O	EBI address/data bus bit 2.
EBI	EBI_AD3	PA.14	MPF7	O	EBI address/data bus bit 3.
EBI	EBI_AD4	PB.2	MPF7	O	EBI address/data bus bit 4.
EBI	EBI_AD5	PB.5	MPF7	O	EBI address/data bus bit 5.
EBI	EBI_AD6	PB.4	MPF7	O	EBI address/data bus bit 6.
EBI	EBI_AD7	PB.5	MPF7	O	EBI address/data bus bit 7.
EBI	EBI_AD8	PB.6	MPF7	O	EBI address/data bus bit 8.
EBI	EBI_AD8	PC.7	MPF7	O	EBI address/data bus bit 8.
EBI	EBI_AD9	PB.7	MPF7	O	EBI address/data bus bit 9.
EBI	EBI_AD9	PC.6	MPF7	O	EBI address/data bus bit 9.
EBI	EBI_ALE	PE.8	MPF7	O	EBI address latch enable output pin.
EBI	EBI_MCLK	PC.0	MPF7	O	EBI interface clock output pin.
EBI	EBI_nCS0	PE.11	MPF7	O	EBI chip select 0 enable output pin.
EBI	EBI_nCS1	PE.12	MPF7	O	EBI chip select 1 enable output pin.
EBI	EBI_nCS2	PE.13	MPF7	O	EBI chip select 2 enable output pin.
EBI	EBI_nCS3	PE.14	MPF7	O	EBI chip select 3 enable output pin.
EBI	EBI_nRD	PE.7	MPF7	O	EBI read enable output pin.
EBI	EBI_nWR	PE.6	MPF7	O	EBI write enable output pin.
EBI	EBI_nWRH	PE.9	MPF7	O	EBI write enable output pin.
EBI	EBI_nWRL	PE.10	MPF7	O	EBI write enable output pin.
ECAP0	ECAP0_IC0	PC.5	MPF8	I	Input 0 of enhanced capture unit 0.
ECAP0	ECAP0_IC0	PD.15	MPF3	I	Input 0 of enhanced capture unit 0.
ECAP0	ECAP0_IC1	PC.4	MPF8	I	Input 1 of enhanced capture unit 0.
ECAP0	ECAP0_IC1	PD.14	MPF3	I	Input 1 of enhanced capture unit 0.
ECAP0	ECAP0_IC2	PC.3	MPF8	I	Input 2 of enhanced capture unit 0.
ECAP0	ECAP0_IC2	PD.13	MPF3	I	Input 2 of enhanced capture unit 0.
ECAP1	ECAP1_IC0	PA.6	MPF8	I	Input 0 of enhanced capture unit 1.
ECAP1	ECAP1_IC1	PA.5	MPF8	I	Input 1 of enhanced capture unit 1.
ECAP1	ECAP1_IC2	PA.4	MPF8	I	Input 2 of enhanced capture unit 1.
EPWMA	EPWM0_0	PA.12	MPF5	I/O	PWM0_0 output/capture input.
EPWMA	EPWM0_1	PA.11	MPF5	I/O	PWM0_1 output/capture input.
EPWMA	EPWM0_2	PA.10	MPF5	I/O	PWM0_2 output/capture input.

EPWMA	EPWM0_3	PA.9	MPF5	I/O	PWM0_3 output/capture input.
EPWMA	EPWM0_4	PA.8	MPF5	I/O	PWM0_4 output/capture input.
EPWMA	EPWM0_5	PA.7	MPF5	I/O	PWM0_5 output/capture input.
EPWMB	EPWM1_0	PB.6	MPF5	I/O	PWM1_0 output/capture input.
EPWMB	EPWM1_1	PB.7	MPF5	I/O	PWM1_1 output/capture input.
EPWMB	EPWM1_2	PB.8	MPF5	I/O	PWM1_2 output/capture input.
EPWMB	EPWM1_3	PB.9	MPF5	I/O	PWM1_3 output/capture input.
EPWMB	EPWM1_4	PB.10	MPF5	I/O	PWM1_4 output/capture input.
EPWMB	EPWM1_5	PB.11	MPF5	I/O	PWM1_5 output/capture input.
I2C0	I2C0_SCL	PA.15	MPF4	I/O	I2C0 clock pin.
I2C0	I2C0_SCL	PD.8	MPF2	I/O	I2C0 clock pin.
I2C0	I2C0_SDA	PC.9	MPF4	I/O	I2C0 data input/output pin.
I2C0	I2C0_SDA	PD.9	MPF2	I/O	I2C0 data input/output pin.
I2C1	I2C1_SCL	PG.15	MPF3	I/O	I2C1 clock pin.
I2C1	I2C1_SCL	PH.0	MPF1	I/O	I2C1 clock pin.
I2C1	I2C1_SDA	PG.14	MPF3	I/O	I2C1 data input/output pin.
I2C1	I2C1_SDA	PH.1	MPF2	I/O	I2C1 data input/output pin.
I2C2	I2C2_SCL	PB.6	MPF1	I/O	I2C2 clock pin.
I2C2	I2C2_SCL	PI.7	MPF1	I/O	I2C2 clock pin.
I2C2	I2C2_SDA	PB.7	MPF1	I/O	I2C2 data input/output pin.
I2C2	I2C2_SDA	PI.8	MPF1	I/O	I2C2 data input/output pin.
I2C3	I2C3_SCL	PD.2	MPF2	I/O	I2C3 clock pin.
I2C3	I2C3_SCL	PH.3	MPF1	I/O	I2C3 clock pin.
I2C3	I2C3_SDA	PD.3	MPF2	I/O	I2C3 data input/output pin.
I2C3	I2C3_SDA	PH.4	MPF1	I/O	I2C3 data input/output pin.
I2C4	I2C4_SCL	PB.0	MPF2	I/O	I2C4 clock pin.
I2C4	I2C4_SCL	PD.10	MPF2	I/O	I2C4 clock pin.
I2C4	I2C4_SCL	PI.11	MPF3	I/O	I2C4 clock pin.
I2C4	I2C4_SDA	PB.1	MPF2	I/O	I2C4 data input/output pin.
I2C4	I2C4_SDA	PD.12	MPF2	I/O	I2C4 data input/output pin.
I2C4	I2C4_SDA	PI.12	MPF3	I/O	I2C4 data input/output pin.
I2S0	I2S0_BCLK	PA.5	MPF3	O	I2S0 bit clock pin.
I2S0	I2S0_DI	PA.4	MPF3	I	I2S0 data input.
I2S0	I2S0_DO	PA.3	MPF3	O	I2S0 data output.
I2S0	I2S0_LRCK	PA.6	MPF3	O	I2S0 left right channel clock.

I2S0	I2S0_MCLK	PA.2	MPF3	O	I2S0 master clock output pin.
I2S1	I2S1_BCLK	PC.1	MPF1	O	I2S1 bit clock pin.
I2S1	I2S1_BCLK	PG.5	MPF2	O	I2S1 bit clock pin.
I2S1	I2S1_BCLK	PI.11	MPF2	O	I2S1 bit clock pin.
I2S1	I2S1_DI	PC.0	MPF1	I	I2S1 data input.
I2S1	I2S1_DI	PG.4	MPF2	I	I2S1 data input.
I2S1	I2S1_DI	PG.9	MPF2	I	I2S1 data input.
I2S1	I2S1_DO	PB.15	MPF1	O	I2S1 data output.
I2S1	I2S1_DO	PC.4	MPF1	O	I2S1 data output.
I2S1	I2S1_DO	PG.3	MPF2	O	I2S1 data output.
I2S1	I2S1_DO	PG.8	MPF2	O	I2S1 data output.
I2S1	I2S1_LRCK	PC.2	MPF1	O	I2S1 left right channel clock.
I2S1	I2S1_LRCK	PG.6	MPF2	O	I2S1 left right channel clock.
I2S1	I2S1_LRCK	PI.12	MPF2	O	I2S1 left right channel clock.
I2S1	I2S1_MCLK	PB.14	MPF1	O	I2S1 master clock output pin.
I2S1	I2S1_MCLK	PC.3	MPF1	O	I2S1 master clock output pin.
I2S1	I2S1_MCLK	PG.7	MPF2	O	I2S1 master clock output pin.
ICE_SW	ICE_CLK	PG.10	MPF1	I	Serial wired debugger clock pin
ICE_SW	ICE_DAT	PG.11	MPF1	I/O	Serial wired debugger data pin
INT	INT0	PA.0	MPF8	I	External interrupt0 input pin.
INT	INT1	PB.0	MPF8	I	External interrupt1 input pin.
INT	INT2	PC.0	MPF8	I	External interrupt2 input pin.
INT	INT3	PD.0	MPF8	I	External interrupt3 input pin.
INT	INT4	PE.0	MPF8	I	External interrupt4 input pin.
INT	INT5	PF.0	MPF8	I	External interrupt5 input pin.
INT	INT6	PG.0	MPF8	I	External interrupt6 input pin.
INT	INT7	PH.0	MPF8	I	External interrupt7 input pin.
GPIO	nRESET	nRESET	MFP0	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
GPIO	PA.0	PA.0	MFP0	I/O	General purpose digital I/O pin.
GPIO	PA.1	PA.1	MFP0	I/O	General purpose digital I/O pin.
GPIO	PA.10	PA.10	MFP0	I/O	General purpose digital I/O pin.
GPIO	PA.11	PA.11	MFP0	I/O	General purpose digital I/O pin.
GPIO	PA.12	PA.12	MFP0	I/O	General purpose digital I/O pin.
GPIO	PA.13	PA.13	MFP0	I/O	General purpose digital I/O pin.
GPIO	PA.14	PA.14	MFP0	I/O	General purpose digital I/O pin.

GPIO	PA.15	PA.15	MFP0	I/O	General purpose digital I/O pin.
GPIO	PA.2	PA.2	MFP0	I/O	General purpose digital I/O pin.
GPIO	PA.3	PA.3	MFP0	I/O	General purpose digital I/O pin.
GPIO	PA.4	PA.4	MFP0	I/O	General purpose digital I/O pin.
GPIO	PA.5	PA.5	MFP0	I/O	General purpose digital I/O pin.
GPIO	PA.6	PA.6	MFP0	I/O	General purpose digital I/O pin.
GPIO	PA.7	PA.7	MFP0	I/O	General purpose digital I/O pin.
GPIO	PA.8	PA.8	MFP0	I/O	General purpose digital I/O pin.
GPIO	PA.9	PA.9	MFP0	I/O	General purpose digital I/O pin.
GPIO	PB.0	PB.0	MFP0	I/O	General purpose digital I/O pin.
GPIO	PB.1	PB.1	MFP0	I/O	General purpose digital I/O pin.
GPIO	PB.10	PB.10	MFP0	I/O	General purpose digital I/O pin.
GPIO	PB.11	PB.11	MFP0	I/O	General purpose digital I/O pin.
GPIO	PB.12	PB.12	MFP0	I/O	General purpose digital I/O pin.
GPIO	PB.13	PB.13	MFP0	I/O	General purpose digital I/O pin.
GPIO	PB.14	PB.14	MFP0	I/O	General purpose digital I/O pin.
GPIO	PB.15	PB.15	MFP0	I/O	General purpose digital I/O pin.
GPIO	PB.3	PB.3	MFP0	I/O	General purpose digital I/O pin.
GPIO	PB.4	PB.4	MFP0	I/O	General purpose digital I/O pin.
GPIO	PB.5	PB.5	MFP0	I/O	General purpose digital I/O pin.
GPIO	PB.6	PB.6	MFP0	I/O	General purpose digital I/O pin.
GPIO	PB.7	PB.7	MFP0	I/O	General purpose digital I/O pin.
GPIO	PB.8	PB.8	MFP0	I/O	General purpose digital I/O pin.
GPIO	PB.9	PB.9	MFP0	I/O	General purpose digital I/O pin.
GPIO	PC.0	PC.0	MFP0	I/O	General purpose digital I/O pin.
GPIO	PC.1	PC.1	MFP0	I/O	General purpose digital I/O pin.
GPIO	PC.10	PC.10	MFP0	I/O	General purpose digital I/O pin.
GPIO	PC.11	PC.11	MFP0	I/O	General purpose digital I/O pin.
GPIO	PC.12	PC.12	MFP0	I/O	General purpose digital I/O pin.
GPIO	PC.13	PC.13	MFP0	I/O	General purpose digital I/O pin.
GPIO	PC.14	PC.14	MFP0	I/O	General purpose digital I/O pin.
GPIO	PC.15	PC.15	MFP0	I/O	General purpose digital I/O pin.
GPIO	PC.2	PC.2	MFP0	I/O	General purpose digital I/O pin.
GPIO	PC.3	PC.3	MFP0	I/O	General purpose digital I/O pin.
GPIO	PC.4	PC.4	MFP0	I/O	General purpose digital I/O pin.

GPIO	PC.5	PC.5	MFP0	I/O	General purpose digital I/O pin.
GPIO	PC.6	PC.6	MFP0	I/O	General purpose digital I/O pin.
GPIO	PC.7	PC.7	MFP0	I/O	General purpose digital I/O pin.
GPIO	PC.8	PC.8	MFP0	I/O	General purpose digital I/O pin.
GPIO	PC.9	PC.9	MFP0	I/O	General purpose digital I/O pin.
GPIO	PD.0	PD.0	MFP0	I/O	General purpose digital I/O pin.
GPIO	PD.1	PD.1	MFP0	I/O	General purpose digital I/O pin.
GPIO	PD.10	PD.10	MFP0	I/O	General purpose digital I/O pin.
GPIO	PD.11	PD.11	MFP0	I/O	General purpose digital I/O pin.
GPIO	PD.12	PD.12	MFP0	I/O	General purpose digital I/O pin.
GPIO	PD.13	PD.13	MFP0	I/O	General purpose digital I/O pin.
GPIO	PD.14	PD.14	MFP0	I/O	General purpose digital I/O pin.
GPIO	PD.15	PD.15	MFP0	I/O	General purpose digital I/O pin.
GPIO	PD.2	PD.2	MFP0	I/O	General purpose digital I/O pin.
GPIO	PD.3	PD.3	MFP0	I/O	General purpose digital I/O pin.
GPIO	PD.4	PD.4	MFP0	I/O	General purpose digital I/O pin.
GPIO	PD.5	PD.5	MFP0	I/O	General purpose digital I/O pin.
GPIO	PD.6	PD.6	MFP0	I/O	General purpose digital I/O pin.
GPIO	PD.7	PD.7	MFP0	I/O	General purpose digital I/O pin.
GPIO	PD.8	PD.8	MFP0	I/O	General purpose digital I/O pin.
GPIO	PD.9	PD.9	MFP0	I/O	General purpose digital I/O pin.
GPIO	PE.0	PE.0	MFP0	I/O	General purpose digital I/O pin.
GPIO	PE.1	PE.1	MFP0	I/O	General purpose digital I/O pin.
GPIO	PE.10	PE.10	MFP0	I/O	General purpose digital I/O pin.
GPIO	PE.11	PE.11	MFP0	I/O	General purpose digital I/O pin.
GPIO	PE.12	PE.12	MFP0	I/O	General purpose digital I/O pin.
GPIO	PE.13	PE.13	MFP0	I/O	General purpose digital I/O pin.
GPIO	PE.14	PE.14	MFP0	I/O	General purpose digital I/O pin.
GPIO	PE.15	PE.15	MFP0	I/O	General purpose digital I/O pin.
GPIO	PE.2	PE.2	MFP0	I/O	General purpose digital I/O pin.
GPIO	PE.3	PE.3	MFP0	I/O	General purpose digital I/O pin.
GPIO	PE.4	PE.4	MFP0	I/O	General purpose digital I/O pin.
GPIO	PE.5	PE.5	MFP0	I/O	General purpose digital I/O pin.
GPIO	PE.6	PE.6	MFP0	I/O	General purpose digital I/O pin.
GPIO	PE.7	PE.7	MFP0	I/O	General purpose digital I/O pin.

GPIO	PE.8	PE.8	MFP0	I/O	General purpose digital I/O pin.
GPIO	PE.9	PE.9	MFP0	I/O	General purpose digital I/O pin.
GPIO	PF.0	PF.0	MFP0	I/O	General purpose digital I/O pin.
GPIO	PF.1	PF.1	MFP0	I/O	General purpose digital I/O pin.
GPIO	PF.10	PF.10	MFP0	I/O	General purpose digital I/O pin.
GPIO	PF.11	PF.11	MFP0	I/O	General purpose digital I/O pin.
GPIO	PF.12	PF.12	MFP0	I/O	General purpose digital I/O pin.
GPIO	PF.13	PF.13	MFP0	I/O	General purpose digital I/O pin.
GPIO	PF.14	PF.14	MFP0	I/O	General purpose digital I/O pin.
GPIO	PF.15	PF.15	MFP0	I/O	General purpose digital I/O pin.
GPIO	PF.2	PF.2	MFP0	I/O	General purpose digital I/O pin.
GPIO	PF.3	PF.3	MFP0	I/O	General purpose digital I/O pin.
GPIO	PF.4	PF.4	MFP0	I/O	General purpose digital I/O pin.
GPIO	PF.5	PF.5	MFP0	I/O	General purpose digital I/O pin.
GPIO	PF.6	PF.6	MFP0	I/O	General purpose digital I/O pin.
GPIO	PF.7	PF.7	MFP0	I/O	General purpose digital I/O pin.
GPIO	PF.8	PF.8	MFP0	I/O	General purpose digital I/O pin.
GPIO	PF.9	PF.9	MFP0	I/O	General purpose digital I/O pin.
GPIO	PG.0	PG.0	MFP0	I/O	General purpose digital I/O pin.
GPIO	PG.1	PG.1	MFP0	I/O	General purpose digital I/O pin.
GPIO	PG.10	PG.10	MFP0	I/O	General purpose digital I/O pin.
GPIO	PG.11	PG.11	MFP0	I/O	General purpose digital I/O pin.
GPIO	PG.12	PG.12	MFP0	I/O	General purpose digital I/O pin.
GPIO	PG.13	PG.13	MFP0	I/O	General purpose digital I/O pin.
GPIO	PG.14	PG.14	MFP0	I/O	General purpose digital I/O pin.
GPIO	PG.15	PG.15	MFP0	I/O	General purpose digital I/O pin.
GPIO	PG.2	PG.2	MFP0	I/O	General purpose digital I/O pin.
GPIO	PG.3	PG.3	MFP0	I/O	General purpose digital I/O pin.
GPIO	PG.4	PG.4	MFP0	I/O	General purpose digital I/O pin.
GPIO	PG.5	PG.5	MFP0	I/O	General purpose digital I/O pin.
GPIO	PG.6	PG.6	MFP0	I/O	General purpose digital I/O pin.
GPIO	PG.7	PG.7	MFP0	I/O	General purpose digital I/O pin.
GPIO	PG.8	PG.8	MFP0	I/O	General purpose digital I/O pin.
GPIO	PG.9	PG.9	MFP0	I/O	General purpose digital I/O pin.
GPIO	PH.0	PH.0	MFP0	I/O	General purpose digital I/O pin.

GPIO	PH.1	PH.1	MFP0	I/O	General purpose digital I/O pin.
GPIO	PH.10	PH.10	MFP0	I/O	General purpose digital I/O pin.
GPIO	PH.11	PH.11	MFP0	I/O	General purpose digital I/O pin.
GPIO	PH.12	PH.12	MFP0	I/O	General purpose digital I/O pin.
GPIO	PH.13	PH.13	MFP0	I/O	General purpose digital I/O pin.
GPIO	PH.14	PH.14	MFP0	I/O	General purpose digital I/O pin.
GPIO	PH.15	PH.15	MFP0	I/O	General purpose digital I/O pin.
GPIO	PH.2	PH.2	MFP0	I/O	General purpose digital I/O pin.
GPIO	PH.3	PH.3	MFP0	I/O	General purpose digital I/O pin.
GPIO	PH.4	PH.4	MFP0	I/O	General purpose digital I/O pin.
GPIO	PH.5	PH.5	MFP0	I/O	General purpose digital I/O pin.
GPIO	PH.6	PH.6	MFP0	I/O	General purpose digital I/O pin.
GPIO	PH.7	PH.7	MFP0	I/O	General purpose digital I/O pin.
GPIO	PH.8	PH.8	MFP0	I/O	General purpose digital I/O pin.
GPIO	PH.9	PH.9	MFP0	I/O	General purpose digital I/O pin.
GPIO	PI.0	PI.0	MFP0	I/O	General purpose digital I/O pin.
GPIO	PI.1	PI.1	MFP0	I/O	General purpose digital I/O pin.
GPIO	PI.10	PI.10	MFP0	I/O	General purpose digital I/O pin.
GPIO	PI.11	PI.11	MFP0	I/O	General purpose digital I/O pin.
GPIO	PI.12	PI.12	MFP0	I/O	General purpose digital I/O pin.
GPIO	PI.13	PI.13	MFP0	I/O	General purpose digital I/O pin.
GPIO	PI.14	PI.14	MFP0	I/O	General purpose digital I/O pin.
GPIO	PI.15	PI.15	MFP0	I/O	General purpose digital I/O pin.
GPIO	PI.2	PI.2	MFP0	I/O	General purpose digital I/O pin.
GPIO	PI.3	PI.3	MFP0	I/O	General purpose digital I/O pin.
GPIO	PI.4	PI.4	MFP0	I/O	General purpose digital I/O pin.
GPIO	PI.5	PI.5	MFP0	I/O	General purpose digital I/O pin.
GPIO	PI.6	PI.6	MFP0	I/O	General purpose digital I/O pin.
GPIO	PI.7	PI.7	MFP0	I/O	General purpose digital I/O pin.
GPIO	PI.8	PI.8	MFP0	I/O	General purpose digital I/O pin.
GPIO	PI.9	PI.9	MFP0	I/O	General purpose digital I/O pin.
OTG_PHY	USB0_D-	USB0_D-		A	USB0 differential signal D-.
OTG_PHY	USB0_D+	USB0_D+		A	USB0 differential signal D+.
OTG_PHY	USB0_OTG_ID	USB0_OTG_ID		I	USB0 OTG ID pin.
OTG_PHY	VBUS	VBUS		A	USB PHY VBUS power input pin.

ADC	V_{REF}	V_{REF}		A	Voltage reference input for ADC. Note: This pin needs to be connected with 0.1uF/10uF capacitors.
OTG_PHY	VRES	VRES		A	USB PHY VRES ground input pin. Add an 8.2K ohm resistor to VSSA.
OTG_PHY	VSSA	VSSA		P	Ground pin for digital circuit. Add a Feritte Bead to digital ground V_{SS}.
LDO_CAP	LDO_CAP	LDO_CAP		P	LDO output pin. Note: This pin needs to be connected with a 1uF capacitor.
LDO_CAP	USB_VDD33_CAP	USB_VDD33_CAP		P	Internal power regulator output 3.3V decoupling pin.
OPA0	OPA0_N	PF.10	MPF1	I/O	General purpose digital I/O pin.
OPA0	OPA0_P	PF.9	MPF1	I/O	General purpose digital I/O pin.
OPA0	OPA0_O	PF.11	MPF1	O	Operational amplifier output pin
OPA1	OPA1_N	PF.13	MPF1	I/O	General purpose digital I/O pin.
OPA1	OPA1_P	PF.12	MPF1	I/O	General purpose digital I/O pin.
OPA1	OPA1_O	PF.14	MPF1	O	Operational amplifier output pin
OTG	USB0_OTG5V_EN	PB.1	MPF1	O	USB0 external VBUS regulator enabled
OTG	USB0_OTG5V_ST	PB.0	MPF1	I	USB0 external VBUS regulator status
OTHER	CLKO	PC.5	MPF1	O	Clock Output Pin.
POWER	AV_{DD}	AV_{DD}		P	Power supply for internal analog circuit.
POWER	AV_{SS}	AV_{SS}		P	Ground pin for digital circuit.
POWER	V_{BAT}	V_{BAT}		P	Battery power input pin.
POWER	VBUS	VBUS		A	USB PHY VBUS power input pin.
POWER	V_{DD}	V_{DD}		P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
POWER	V_{SS}	V_{SS}		P	Ground pin for digital circuit.
POWER	VSSA	VSSA		P	Ground pin for digital circuit. Add a Feritte Bead to digital ground V_{SS}.
PS2D	PS2_CLK	PG.3	MPF1	O	PS2 clock pin.
PS2D	PS2_DAT	PG.4	MPF1	I/O	PS2 data pin.
QEI0	QEI0_A	PC.5	MPF5	I	Quadrature encoder phase A input of QEI Unit 0.
QEI0	QEI0_B	PC.4	MPF5	I	Quadrature encoder phase B input of QEI Unit 0.
QEI0	QEI0_Z	PC.3	MPF5	I	Quadrature encoder phase Z input of QEI Unit 0.
QEI1	QEI1_A	PA.6	MPF5	I	Quadrature encoder phase A input of QEI Unit 1.
QEI1	QEI1_B	PA.5	MPF5	I	Quadrature encoder phase B input of QEI Unit 1.
QEI1	QEI1_Z	PA.4	MPF5	I	Quadrature encoder phase Z input of QEI Unit 1.
SC0	SC0_CD	PA.0	MPF2	I	SmartCard0 card detect pin.

SC0	SC0_CLK	PA.7	MPF2	O	SmartCard0 clock pin.
SC0	SC0_DAT	PA.10	MPF2	I/O	SmartCard0 data pin.
SC0	SC0_PWR	PA.9	MPF2	O	SmartCard0 power pin.
SC0	SC0_RST	PA.8	MPF2	O	SmartCard0 reset pin.
SC1	SC1_CD	PC.3	MPF2	I	SmartCard1 card detect pin.
SC1	SC1_CD	PG.7	MPF3	I	SmartCard1 card detect pin.
SC1	SC1_CLK	PC.1	MPF2	O	SmartCard1 clock pin.
SC1	SC1_CLK	PG.6	MPF3	O	SmartCard1 clock pin.
SC1	SC1_DAT	PB.15	MPF2	I/O	SmartCard1 data pin.
SC1	SC1_DAT	PC.0	MPF2	I/O	SmartCard1 data pin.
SC1	SC1_DAT	PG.5	MPF3	I/O	SmartCard1 data pin.
SC1	SC1_PWR	PC.2	MPF2	O	SmartCard1 power pin.
SC1	SC1_PWR	PG.4	MPF3	O	SmartCard1 power pin.
SC1	SC1_RST	PB.14	MPF2	O	SmartCard1 reset pin.
SC1	SC1_RST	PC.4	MPF2	O	SmartCard1 reset pin.
SC1	SC1_RST	PG.3	MPF3	O	SmartCard1 reset pin.
SC2	SC2_CD	PA.6	MPF1	I	SmartCard2 card detect pin.
SC2	SC2_CLK	PA.3	MPF1	O	SmartCard2 clock pin.
SC2	SC2_DAT	PA.2	MPF1	I/O	SmartCard2 data pin.
SC2	SC2_PWR	PA.4	MPF1	O	SmartCard2 power pin.
SC2	SC2_RST	PA.5	MPF1	O	SmartCard2 reset pin.
SC3	SC3_CD	PC.10	MPF1	I	SmartCard3 card detect pin.
SC3	SC3_CD	PI.12	MPF4	I	SmartCard3 card detect pin.
SC3	SC3_CLK	PA.14	MPF3	O	SmartCard3 clock pin.
SC3	SC3_CLK	PD.12	MPF1	O	SmartCard3 clock pin.
SC3	SC3_CLK	PG.9	MPF4	O	SmartCard3 clock pin.
SC3	SC3_DAT	PA.13	MPF3	I/O	SmartCard3 data pin.
SC3	SC3_DAT	PD.10	MPF1	I/O	SmartCard3 data pin.
SC3	SC3_DAT	PG.8	MPF4	I/O	SmartCard3 data pin.
SC3	SC3_PWR	PA.15	MPF1	O	SmartCard3 power pin.
SC3	SC3_PWR	PI.11	MPF4	O	SmartCard3 power pin.
SC3	SC3_RST	PC.9	MPF3	O	SmartCard3 reset pin.
SC3	SC3_RST	PD.11	MPF1	O	SmartCard3 reset pin.
SC3	SC3_RST	PG.7	MPF4	O	SmartCard3 reset pin.
SC4	SC4_CD	PC.12	MPF2	I	SmartCard4 card detect pin.

SC4	SC4_CLK	PD.0	MPF2	O	SmartCard4 clock pin.
SC4	SC4_DAT	PC.15	MPF2	I/O	SmartCard4 data pin.
SC4	SC4_PWR	PC.14	MPF2	O	SmartCard4 power pin.
SC4	SC4_RST	PC.13	MPF2	O	SmartCard4 reset pin.
SC5	SC5_CD	PA.1	MPF2	I	SmartCard5 card detect pin.
SC5	SC5_CD	PD.4	MPF1	I	SmartCard5 card detect pin.
SC5	SC5_CLK	PD.3	MPF1	O	SmartCard5 clock pin.
SC5	SC5_CLK	PH.15	MPF2	O	SmartCard5 clock pin.
SC5	SC5_DAT	PD.7	MPF1	I/O	SmartCard5 data pin.
SC5	SC5_DAT	PI.2	MPF1	I/O	SmartCard5 data pin.
SC5	SC5_PWR	PD.6	MPF1	O	SmartCard5 power pin.
SC5	SC5_PWR	PI.1	MPF2	O	SmartCard5 power pin.
SC5	SC5_RST	PD.5	MPF1	O	SmartCard5 reset pin.
SC5	SC5_RST	PI.0	MPF2	O	SmartCard5 reset pin.
SDHOST0	SD0_CDn	PD.3	MPF4	I	SD mode #0 – card detect
SDHOST0	SD0_CDn	PE.5	MPF4	I	SD mode #0 – card detect
SDHOST0	SD0_CDn	PF.6	MPF4	I	SD mode #0 – card detect
SDHOST0	SD0_CLK	PD.7	MPF4	O	SD mode #0– clock;
SDHOST0	SD0_CLK	PE.7	MPF4	O	SD mode #0– clock;
SDHOST0	SD0_CLK	PF.8	MPF4	O	SD mode #0– clock;
SDHOST0	SD0_CMD	PD.6	MPF4	I/O	SD mode #0 – command/response
SDHOST0	SD0_CMD	PE.6	MPF4	I/O	SD mode #0 – command/response
SDHOST0	SD0_CMD	PF.7	MPF4	I/O	SD mode #0 – command/response
SDHOST0	SD0_DAT0	PE.11	MPF4	I/O	SD mode #0 data line bit 0;
SDHOST0	SD0_DAT0	PF.5	MPF4	I/O	SD mode #0 data line bit 0;
SDHOST0	SD0_DAT1	PE.10	MPF4	I/O	SD mode #0 data line bit 1;
SDHOST0	SD0_DAT1	PF.4	MPF4	I/O	SD mode #0 data line bit 1;
SDHOST0	SD0_DAT2	PE.9	MPF4	I/O	SD mode #0 data line bit 2;
SDHOST0	SD0_DAT2	PF.3	MPF4	I/O	SD mode #0 data line bit 2;
SDHOST0	SD0_DAT3	PE.8	MPF4	I/O	SD mode #0 data line bit 3;
SDHOST0	SD0_DAT3	PF.2	MPF4	I/O	SD mode #0 data line bit 3;
SDHOST1	SD1_CDn	PC.12	MPF4	I	SD mode #1 – card detect
SDHOST1	SD1_CLK	PC.14	MPF4	O	SD mode #1– clock;
SDHOST1	SD1_CMD	PC.13	MPF4	I/O	SD mode #1 – command/response
SDHOST1	SD1_DAT0	PD.2	MPF4	I/O	SD mode #1 data line bit 0;

SDHOST1	SD1_DAT1	PD.1	MPF4	I/O	SD mode #1 data line bit 1;
SDHOST1	SD1_DAT2	PD.0	MPF4	I/O	SD mode #1 data line bit 2;
SDHOST1	SD1_DAT3	PC.15	MPF4	I/O	SD mode #1 data line bit 3;
Slew	HS	PA.2	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PA.3	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PA.4	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PA.5	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PA.6	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PA.7	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PA.8	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PA.9	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PA.10	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PA.11	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PA.12	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PA.13	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PA.14	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PA.15	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PB.3	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PB.4	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PB.5	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PB.6	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PB.7	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PB.8	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PB.9	Slew		This pad is embedded with “Slew Rate Control” capability.

Slew	HS	PB.10	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PB.11	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PB.12	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PB.13	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PB.14	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PB.15	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PC.0	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PC.1	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PC.2	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PC.3	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PC.4	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PC.5	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PC.6	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PC.7	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PC.8	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PC.9	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PC.10	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PC.11	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PC.12	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PC.13	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PC.14	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PC.15	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PD.0	Slew		This pad is embedded with “Slew Rate Control” capability.

Slew	HS	PD.1	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PD.2	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PD.3	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PD.4	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PD.5	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PD.6	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PD.7	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PD.8	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PD.9	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PD.13	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PD.14	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PD.15	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PE.2	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PE.3	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PE.4	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PE.5	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PE.6	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PE.7	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PE.8	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PE.9	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PE.10	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PE.11	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PE.12	Slew		This pad is embedded with “Slew Rate Control” capability.

Slew	HS	PE.13	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PE.14	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PF.0	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PF.1	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PF.2	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PF.3	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PF.4	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PF.5	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PF.6	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PF.7	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PF.8	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PF.9	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PF.10	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PG.7	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PG.8	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PG.9	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PH.5	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PH.6	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PH.7	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PH.8	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PH.9	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PH.10	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PI.3	Slew		This pad is embedded with “Slew Rate Control” capability.

Slew	HS	PI.4	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PI.5	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PI.6	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PI.7	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PI.8	Slew		This pad is embedded with “Slew Rate Control” capability.
Slew	HS	PI.11	Slew		This pad is embedded with “Slew Rate Control” capability.
SPI0	SPI0_CLK	PC.8	MPF4	O	SPI0 serial clock pin.
SPI0	SPI0_CLK	PE.5	MPF3	O	SPI0 serial clock pin.
SPI0	SPI0_MISO0	PC.6	MPF4	I/O	1st SPI0 MISO (Master In, Slave Out) pin.
SPI0	SPI0_MISO0	PE.2	MPF3	I/O	1st SPI0 MISO (Master In, Slave Out) pin.
SPI0	SPI0_MISO0	PE.6	MPF3	I/O	1st SPI0 MISO (Master In, Slave Out) pin.
SPI0	SPI0_MISO1	PC.3	MPF4	I/O	2nd SPI0 MISO (Master In, Slave Out) pin.
SPI0	SPI0_MISO1	PE.10	MPF3	I/O	2nd SPI0 MISO (Master In, Slave Out) pin.
SPI0	SPI0_MOSI0	PC.7	MPF4	I/O	1st SPI0 MOSI (Master Out, Slave In) pin.
SPI0	SPI0_MOSI0	PE.3	MPF3	I/O	1st SPI0 MOSI (Master Out, Slave In) pin.
SPI0	SPI0_MOSI0	PE.7	MPF3	I/O	1st SPI0 MOSI (Master Out, Slave In) pin.
SPI0	SPI0_MOSI1	PC.4	MPF4	I/O	2nd SPI0 MOSI (Master Out, Slave In) pin.
SPI0	SPI0_MOSI1	PE.11	MPF3	I/O	2nd SPI0 MOSI (Master Out, Slave In) pin.
SPI0	SPI0_SS0	PC.2	MPF4	I/O	1st SPI0 slave select pin.
SPI0	SPI0_SS0	PE.4	MPF3	I/O	1st SPI0 slave select pin.
SPI1	SPI1_CLK	PD.1	MPF1	O	SPI1 serial clock pin.
SPI1	SPI1_CLK	PD.14	MPF1	O	SPI1 serial clock pin.
SPI1	SPI1_MISO0	PD.0	MPF1	I/O	1st SPI1 MISO (Master In, Slave Out) pin.
SPI1	SPI1_MISO0	PD.15	MPF1	I/O	1st SPI1 MISO (Master In, Slave Out) pin.
SPI1	SPI1_MISO1	PC.14	MPF1	I/O	2nd SPI1 MISO (Master In, Slave Out) pin.
SPI1	SPI1_MOSI0	PC.15	MPF1	I/O	1st SPI1 MOSI (Master Out, Slave In) pin.
SPI1	SPI1_MOSI0	PF.0	MPF1	I/O	1st SPI1 MOSI (Master Out, Slave In) pin.
SPI1	SPI1_MOSI1	PC.13	MPF1	I/O	2nd SPI1 MOSI (Master Out, Slave In) pin.
SPI1	SPI1_SS0	PC.12	MPF1	I/O	1st SPI1 slave select pin.
SPI1	SPI1_SS0	PD.13	MPF1	I/O	1st SPI1 slave select pin.
SPI2	SPI2_CLK	PB.3	MPF2	O	SPI2 serial clock pin.
SPI2	SPI2_CLK	PG.9	MPF1	O	SPI2 serial clock pin.

SPI2	SPI2_CLK	PH.6	MPF1	O	SPI2 serial clock pin.
SPI2	SPI2_MISO0	PB.4	MPF2	I/O	1st SPI2 MISO (Master In, Slave Out) pin.
SPI2	SPI2_MISO0	PG.7	MPF1	I/O	1st SPI2 MISO (Master In, Slave Out) pin.
SPI2	SPI2_MISO0	PH.7	MPF1	I/O	1st SPI2 MISO (Master In, Slave Out) pin.
SPI2	SPI2_MISO1	PB.12	MPF2	I/O	2nd SPI2 MISO (Master In, Slave Out) pin.
SPI2	SPI2_MISO1	PH.9	MPF1	I/O	2nd SPI2 MISO (Master In, Slave Out) pin.
SPI2	SPI2_MISO1	PI.12	MPF1	I/O	2nd SPI2 MISO (Master In, Slave Out) pin.
SPI2	SPI2_MOSI0	PB.5	MPF2	I/O	1st SPI2 MOSI (Master Out, Slave In) pin.
SPI2	SPI2_MOSI0	PG.8	MPF1	I/O	1st SPI2 MOSI (Master Out, Slave In) pin.
SPI2	SPI2_MOSI0	PH.8	MPF1	I/O	1st SPI2 MOSI (Master Out, Slave In) pin.
SPI2	SPI2_MOSI1	PB.13	MPF2	I/O	2nd SPI2 MOSI (Master Out, Slave In) pin.
SPI2	SPI2_MOSI1	PF.1	MPF1	I/O	2nd SPI2 MOSI (Master Out, Slave In) pin.
SPI2	SPI2_MOSI1	PH.10	MPF1	I/O	2nd SPI2 MOSI (Master Out, Slave In) pin.
SPI2	SPI2_SS0	PB.2	MPF2	I/O	1st SPI2 slave select pin.
SPI2	SPI2_SS0	PH.5	MPF1	I/O	1st SPI2 slave select pin.
SPI2	SPI2_SS0	PI.11	MPF1	I/O	1st SPI2 slave select pin.
SPI3	SPI3_CLK	PA.4	MPF2	O	SPI3 serial clock pin.
SPI3	SPI3_CLK	PA.8	MPF3	O	SPI3 serial clock pin.
SPI3	SPI3_CLK	PF.3	MPF1	O	SPI3 serial clock pin.
SPI3	SPI3_CLK	PI.4	MPF1	O	SPI3 serial clock pin.
SPI3	SPI3_MISO0	PA.2	MPF2	I/O	1st SPI3 MISO (Master In, Slave Out) pin.
SPI3	SPI3_MISO0	PA.9	MPF3	I/O	1st SPI3 MISO (Master In, Slave Out) pin.
SPI3	SPI3_MISO0	PF.4	MPF1	I/O	1st SPI3 MISO (Master In, Slave Out) pin.
SPI3	SPI3_MISO0	PI.5	MPF1	I/O	1st SPI3 MISO (Master In, Slave Out) pin.
SPI3	SPI3_MISO1	PA.11	MPF3	I/O	2nd SPI3 MISO (Master In, Slave Out) pin.
SPI3	SPI3_MISO1	PD.8	MPF1	I/O	2nd SPI3 MISO (Master In, Slave Out) pin.
SPI3	SPI3_MISO1	PI.7	MPF2	I/O	2nd SPI3 MISO (Master In, Slave Out) pin.
SPI3	SPI3_MOSI0	PA.3	MPF2	I/O	1st SPI3 MOSI (Master Out, Slave In) pin.
SPI3	SPI3_MOSI0	PA.10	MPF3	I/O	1st SPI3 MOSI (Master Out, Slave In) pin.
SPI3	SPI3_MOSI0	PF.5	MPF1	I/O	1st SPI3 MOSI (Master Out, Slave In) pin.
SPI3	SPI3_MOSI0	PI.6	MPF1	I/O	1st SPI3 MOSI (Master Out, Slave In) pin.
SPI3	SPI3_MOSI1	PA.12	MPF3	I/O	2nd SPI3 MOSI (Master Out, Slave In) pin.
SPI3	SPI3_MOSI1	PD.9	MPF1	I/O	2nd SPI3 MOSI (Master Out, Slave In) pin.
SPI3	SPI3_MOSI1	PI.8	MPF2	I/O	2nd SPI3 MOSI (Master Out, Slave In) pin.
SPI3	SPI3_SS0	PA.5	MPF2	I/O	1st SPI3 slave select pin.

SPI3	SPI3_SS0	PA.7	MPF3	I/O	1st SPI3 slave select pin.
SPI3	SPI3_SS0	PF.2	MPF1	I/O	1st SPI3 slave select pin.
SPI3	SPI3_SS0	PI.3	MPF1	I/O	1st SPI3 slave select pin.
T0EX	TM0_EXT	PC.8	MPF1	I	Timer0 external capture input
T1EX	TM1_EXT	PC.7	MPF1	I	Timer1 external capture input
T2EX	TM2_EXT	PC.6	MPF1	I	Timer2 external capture input
T3EX	TM3_EXT	PC.14	MPF3	I	Timer3 external capture input
TAMPER	TAMPER0	PA.0	MPF1	I/O	Tamper detect pin 0.
TAMPER	TAMPER1	PA.1	MPF1	I/O	Tamper detect pin 1.
Timer0	TM0_CNT_OUT	PB.4	MPF4	I/O	Timer0 event counter input/toggle output.
Timer0	TM0_CNT_OUT	PD.1	MPF3	I/O	Timer0 event counter input/toggle output.
Timer1	TM1_CNT_OUT	PB.1	MPF3	I/O	Timer1 event counter input/toggle output.
Timer1	TM1_CNT_OUT	PE.8	MPF3	I/O	Timer1 event counter input/toggle output.
Timer2	TM2_CNT_OUT	PC.6	MPF5	I/O	Timer2 event counter input/toggle output.
Timer2	TM2_CNT_OUT	PE.1	MPF3	I/O	Timer2 event counter input/toggle output.
Timer3	TM3_CNT_OUT	PC.1	MPF5	I/O	Timer3 event counter input/toggle output.
Timer3	TM3_CNT_OUT	PD.11	MPF3	I/O	Timer3 event counter input/toggle output.
UART0	UART0_CTS	PA.12	MPF1	I	Clear to Send input pin for UART0.
UART0	UART0_CTS	PG.0	MPF1	I	Clear to Send input pin for UART0.
UART0	UART0_RTS	PA.11	MPF1	O	Request to Send output pin for UART0.
UART0	UART0_RTS	PF.15	MPF1	O	Request to Send output pin for UART0.
UART0	UART0_RXD	PA.13	MPF1	I	Data receiver input pin for UART0.
UART0	UART0_RXD	PG.1	MPF1	I	Data receiver input pin for UART0.
UART0	UART0_TXD	PA.14	MPF1	O	Data transmitter output pin for UART0.
UART0	UART0_TXD	PG.2	MPF1	O	Data transmitter output pin for UART0.
UART1	UART1_CTS	PB.5	MPF1	I	Clear to Send input pin for UART1.
UART1	UART1_CTS	PF.12	MPF2	I	Clear to Send input pin for UART1.
UART1	UART1_RTS	PB.4	MPF1	O	Request to Send output pin for UART1.
UART1	UART1_RTS	PF.11	MPF2	O	Request to Send output pin for UART1.
UART1	UART1_RXD	PB.2	MPF1	I	Data receiver input pin for UART1.
UART1	UART1_RXD	PF.14	MPF2	I	Data receiver input pin for UART1.
UART1	UART1_TXD	PB.3	MPF1	O	Data transmitter output pin for UART1.
UART1	UART1_TXD	PF.13	MPF2	O	Data transmitter output pin for UART1.
UART2	UART2_CTS	PC.9	MPF2	I	Clear to Send input pin for UART2.
UART2	UART2_CTS	PH.2	MPF1	I	Clear to Send input pin for UART2.

UART2	UART2_RTS	PA.15	MPF2	O	Request to Send output pin for UART2.
UART2	UART2_RTS	PF.8	MPF1	O	Request to Send output pin for UART2.
UART2	UART2_RXD	PC.10	MPF2	I	Data receiver input pin for UART2.
UART2	UART2_RXD	PF.6	MPF1	I	Data receiver input pin for UART2.
UART2	UART2_TXD	PC.11	MPF1	O	Data transmitter output pin for UART2.
UART2	UART2_TXD	PF.7	MPF1	O	Data transmitter output pin for UART2.
UART3	UART3_CTS	PD.7	MPF2	I	Clear to Send input pin for UART3.
UART3	UART3_CTS	PH.14	MPF1	I	Clear to Send input pin for UART3.
UART3	UART3_RTS	PD.6	MPF2	O	Request to Send output pin for UART3.
UART3	UART3_RTS	PH.13	MPF1	O	Request to Send output pin for UART3.
UART3	UART3_RXD	PD.4	MPF2	I	Data receiver input pin for UART3.
UART3	UART3_RXD	PH.11	MPF1	I	Data receiver input pin for UART3.
UART3	UART3_TXD	PD.5	MPF2	O	Data transmitter output pin for UART3.
UART3	UART3_TXD	PH.12	MPF1	O	Data transmitter output pin for UART3.
UART4	UART4_CTS	PB.7	MPF3	I	Clear to Send input pin for UART4.
UART4	UART4_CTS	PB.13	MPF1	I	Clear to Send input pin for UART4.
UART4	UART4_CTS	PC.3	MPF3	I	Clear to Send input pin for UART4.
UART4	UART4_CTS	PG.9	MPF3	I	Clear to Send input pin for UART4.
UART4	UART4_RTS	PB.6	MPF3	O	Request to Send output pin for UART4.
UART4	UART4_RTS	PB.12	MPF1	O	Request to Send output pin for UART4.
UART4	UART4_RTS	PC.2	MPF3	O	Request to Send output pin for UART4.
UART4	UART4_RTS	PG.8	MPF3	O	Request to Send output pin for UART4.
UART4	UART4_RXD	PB.4	MPF3	I	Data receiver input pin for UART4.
UART4	UART4_RXD	PC.0	MPF3	I	Data receiver input pin for UART4.
UART4	UART4_RXD	PH.0	MPF2	I	Data receiver input pin for UART4.
UART4	UART4_TXD	PB.5	MPF3	O	Data transmitter output pin for UART4.
UART4	UART4_TXD	PC.1	MPF3	O	Data transmitter output pin for UART4.
UART4	UART4_TXD	PH.1	MPF1	O	Data transmitter output pin for UART4.
UART5	UART5_CTS	PB.8	MPF1	I	Clear to Send input pin for UART5.
UART5	UART5_CTS	PD.13	MPF2	I	Clear to Send input pin for UART5.
UART5	UART5_RTS	PB.9	MPF1	O	Request to Send output pin for UART5.
UART5	UART5_RTS	PD.14	MPF2	O	Request to Send output pin for UART5.
UART5	UART5_RXD	PB.11	MPF1	I	Data receiver input pin for UART5.
UART5	UART5_RXD	PF.0	MPF2	I	Data receiver input pin for UART5.
UART5	UART5_TXD	PB.10	MPF1	O	Data transmitter output pin for UART5.

UART5	UART5_TXD	PD.15	MPF2	O	Data transmitter output pin for UART5.
USBIOPHY	USB1_D-	PB.2	MPF3	A	USB1 differential signal D-.
USBIOPHY	USB1_D+	PB.3	MPF3	A	USB1 differential signal D+.
USBPHY	USB_VDD33_CAP	USB_VDD33_CAP		P	Internal power regulator output 3.3V decoupling pin.
USBPHY	USB0_D-	USB0_D-		A	USB0 differential signal D-.
USBPHY	USB0_D+	USB0_D+		A	USB0 differential signal D+.
USBPHY	USB0_OTG_ID	USB0_OTG_ID		I	USB0 OTG ID pin.
USBPHY	VBUS	VBUS		A	USB PHY VBUS power input pin.
USBPHY	VRES	VRES		A	USB PHY VRES ground input pin. Add an 8.2K ohm resistor to VSSA.
USBPHY	VSSA	VSSA		A	Ground pin for digital circuit. Add a Feritte Bead to digital ground V_{SS}.
CAP	CAP_DATA0	PD.3	MPF5	I	Image data input bus bit 0.
CAP	CAP_DATA1	PD.2	MPF5	I	Image data input bus bit 1.
CAP	CAP_DATA2	PD.1	MPF5	I	Image data input bus bit 2.
CAP	CAP_DATA3	PD.0	MPF5	I	Image data input bus bit 3.
CAP	CAP_DATA4	PC.15	MPF5	I	Image data input bus bit 4.
CAP	CAP_DATA5	PC.14	MPF5	I	Image data input bus bit 5.
CAP	CAP_DATA6	PC.13	MPF5	I	Image data input bus bit 6.
CAP	CAP_DATA7	PC.12	MPF5	I	Image data input bus bit 7.
CAP	CAP_HSYNC	PD.6	MPF5	I	Image capture interface HSYNC input pin.
CAP	CAP_PIXCLK	PD.7	MPF5	I	Image capture interface pix clock input pin.
CAP	CAP_SCLK	PD.4	MPF5	O	Image capture interface sensor clock pin.
CAP	CAP_SFIELD	PA.2	MPF5	I	Video input interface SFIELD input pin.
CAP	CAP_VSYNC	PD.5	MPF5	I	Image capture interface VSYNC input pin.
X32K	X32K_IN	PG.15	MPF1	I	External 32.768 kHz (low-speed) crystal input pin.
X32K	X32K_OUT	PG.14	MPF1	O	External 32.768 kHz (low-speed) crystal output pin.
XIN1	XT1_IN	PG.13	MPF1	I	External 4~24 MHz (high-speed) crystal input pin.
XIN1	XT1_OUT	PG.12	MPF1	O	External 4~24 MHz (high-speed) crystal output pin.

5 BLOCK DIAGRAM

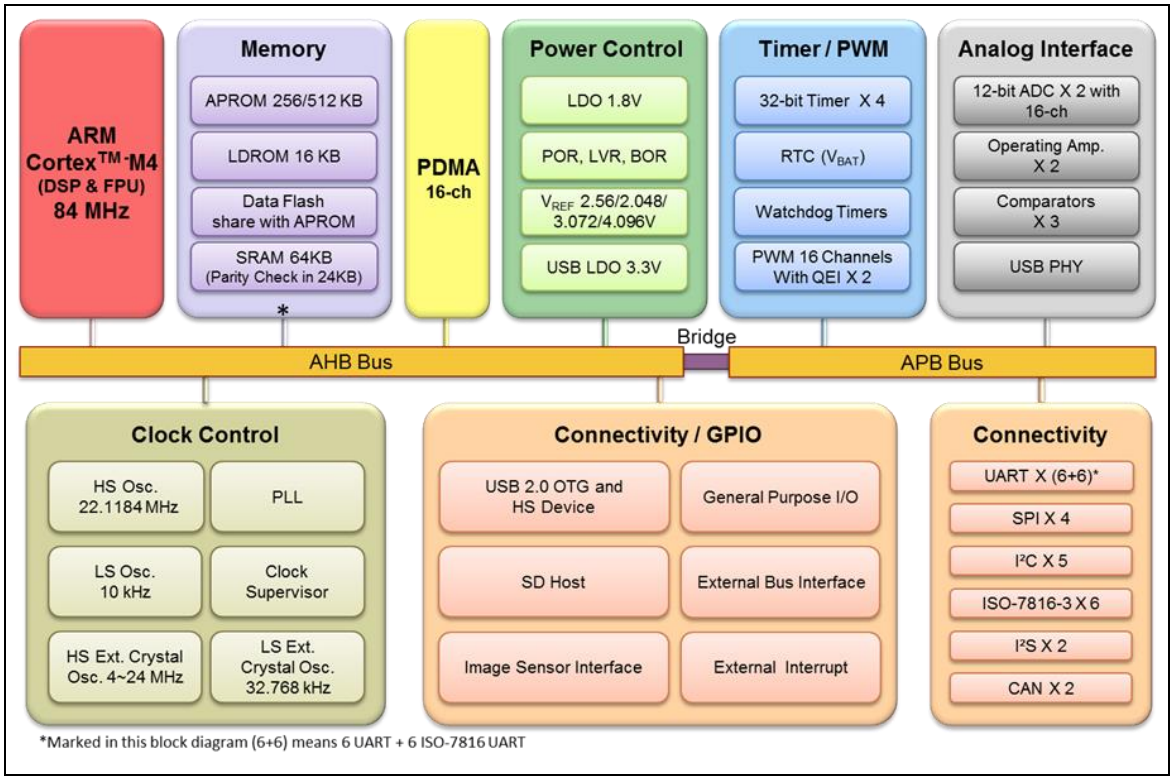


Figure 4.3-1 NuMicro™ NUC442 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M4 Core

The Cortex®-M4 processor, a configurable, multistage, 32-bit RISC processor, has three AMBA AHB-Lite interfaces for best parallel performance and includes an NVIC component. The processor with optional hardware debug functionality can execute Thumb code and is compatible with other Cortex®-M profile processors. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The Cortex®-M4F is a processor with the same capability as the Cortex®-M4 processor and includes floating point arithmetic functionality. The NUC442 series is embedded with Cortex™-M4F processor. Throughout this document, the name Cortex®-M4 refers to both Cortex®-M4 and Cortex®-M4F processors. The following figure shows the functional controller of the processor.

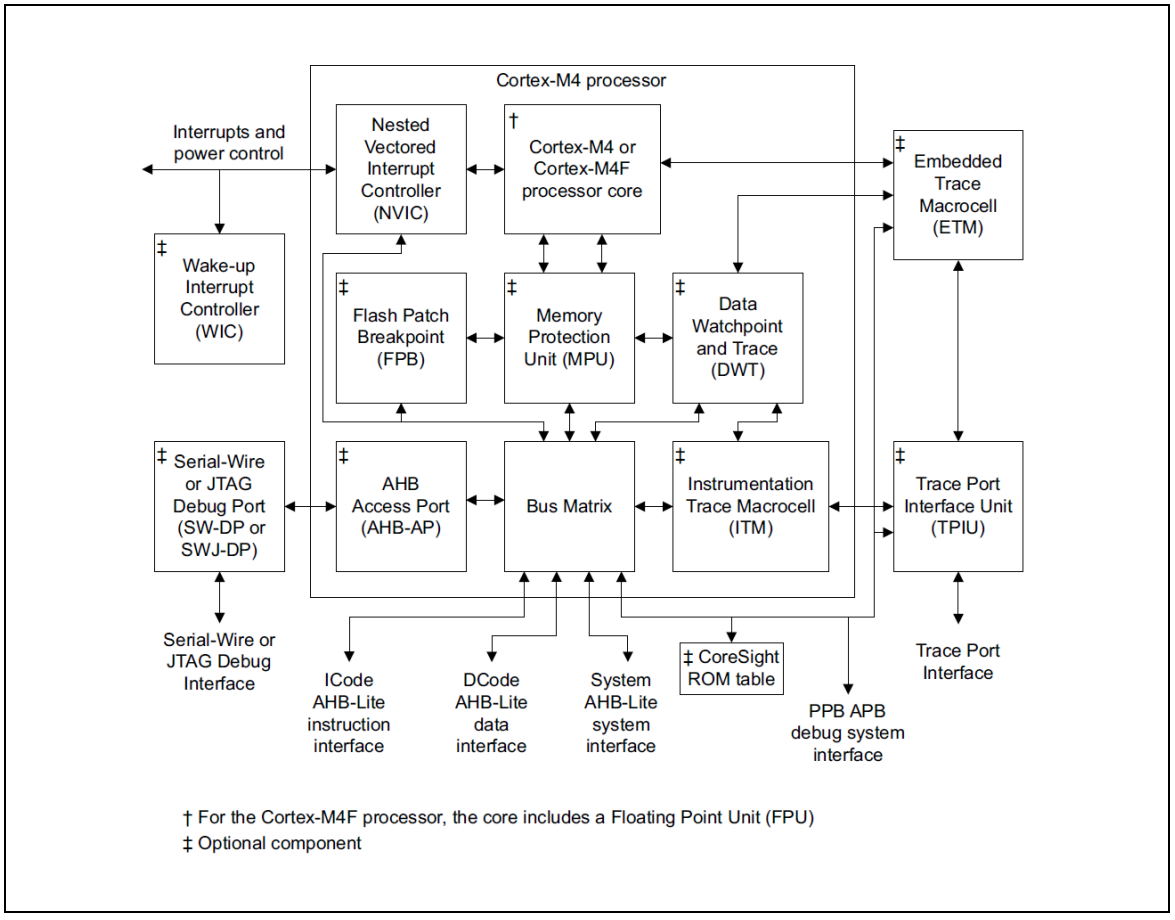


Figure 6.1-1 Cortex®-M4 Block Diagram

Cortex®-M4 processor features:

- A low gate count processor core, with low latency interrupt processing that has:
  - A subset of the Thumb instruction set, defined in the *ARMv7-M Architecture Reference Manual*
  - Banked Stack Pointer (SP)

- Hardware integer divide instructions, SDIV and UDIV
- Handler and Thread modes
- Thumb and Debug states
- Support for interruptible-continued instructions LDM, STM, PUSH, and POP for low interrupt latency
- Automatic processor state saving and restoration for low latency *Interrupt Service Routine (ISR)* entry and exit
- Support for ARMv6 big-endian byte-invariant or little-endian accesses
- Support for ARMv6 unaligned accesses

- Floating Point Unit (FPU) in the Cortex®-M4F processor providing:
  - 32-bit instructions for single-precision (C float) data-processing operations
  - Combined Multiply and Accumulate instructions for increased precision (Fused MAC)
  - Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
  - Hardware support for denormals and all IEEE rounding modes
  - 32 dedicated 32-bit single precision registers, also addressable as 16 double-word registers
  - Decoupled three stage pipeline
- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Features include:
  - External interrupts. Configurable from 1 to 240 (the NUC442 series configured with 97 interrupts)
  - Bits of priority, configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping which enables selection of preempting interrupt levels and non-preempting interrupt levels
  - Support for tril-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
  - Processor state automatically saved on interrupt entry, and restored on interrupt exit with on instruction overhead
  - Support for Wake-up Interrupt Controller (WIC) with Ultra-low Power Sleep mode
- Memory Protection Unit (MPU). An optional MPU for memory protection, including:
  - Eight memory regions
  - Sub Region Disable (SRD), enabling efficient use of memory regions
  - The ability to enable a background region that implements the default memory map attributes
- Low-cost debug solution that features:
  - Debug access to all memory and registers in the system, including access to memory mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is

asserted.

- Serial Wire Debug Port(SW-DP) debug access
- Optional Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
- Optional Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
- Optional Instrumentation Trace Macrocell (ITM) for support of printf() style debugging
- Optional Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer (TPA), including Single Wire Output (SWO) mode

- Bus interfaces:
  - Three Advanced High-performance Bus-Lite (AHB-Lite) interfaces: ICode, Dcode, and System bus interfaces
  - Private Peripheral Bus (PPB) based on Advanced Peripheral Bus (APB) interface
  - Bit-band support that includes atomic bit-band write and read operations.
  - Memory access alignment
  - Write buffer for buffering of write data
  - Exclusive access transfers for multiprocessor systems

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the below listed events. For these reset event flags can be read by SYS_RSTSTS register.

- Hardware Reset
  - Power-on Reset (POR)
  - Low level on the nRESEST Pin (nRST)
  - Watchdag Time-out Reset (WDT)
  - Low Voltage Reset (LVR)
  - Brown out Detector Reset BOD_RST)
- Software Reset
  - MCU Reset- SYSRESETREQ(AIRCR[2])
  - Cortes-M4 Core One-shot Reset – CPURST(IPRSTC[1])
  - Chip One-shot Reset – CHIPRST(IPRSTC[0])

Note: ISPCON.BS keeps the original value after MCU Reset and CPU Reset.

6.2.3 System Power Distribution

In this chip, power distribution is divided into three segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from VBUS offers the power for operating the USB transceiver.
- RTC power from V_{BAT} supplies the power to internal regulator which provides a fixed 1.8V power for RTC operation and I/O pins .

The outputs of internal voltage regulators, LDO and VDD33, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). The following figure shows the power distribution of the NuMicro™ NUC442.

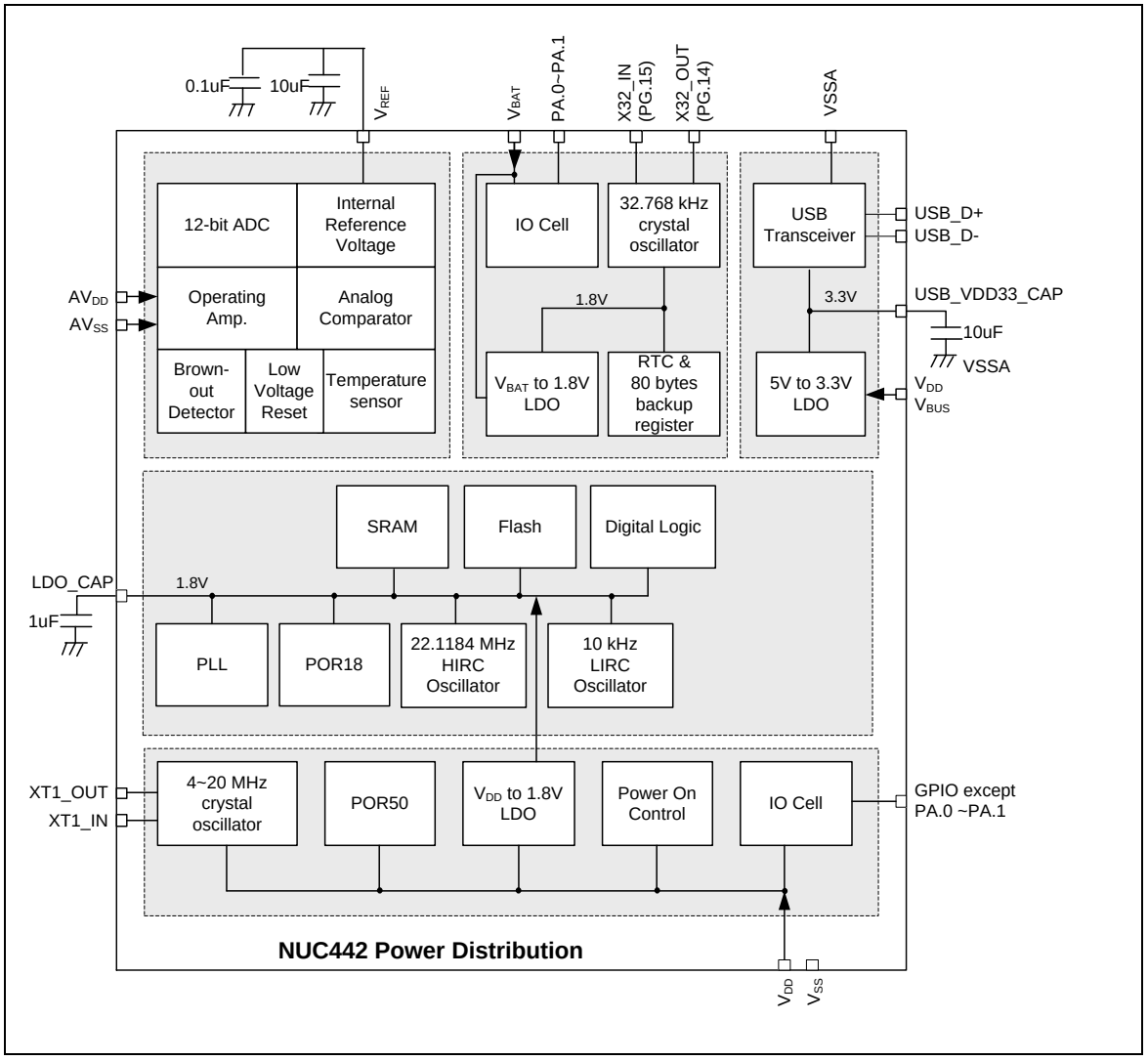


Figure 6.2-1 NuMicro™ NUC442 Power Distribution Diagram

6.2.4 System Memory Map

The NUC442 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in the following table. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripherals. The NUC442 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0007_FFFF	FLASH_BA	FLASH Memory Space (128KB)
0x2000_0000 – 0x2000_FFFF	SRAM_BA	SRAM Memory Space (16KB)
0x6000_0000 – 0x6FFF_FFFF	EXTMEM_BA	External Memory Space (256MB)
Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers
0x4000_0300 – 0x4000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_8000 – 0x4000_8FFF	PDMA_BA	Peripheral DMA Control Registers
0x4000_9000 – 0x4000_9FFF	USBH_BA	USB Host Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers
0x4000_D000 – 0x4000_DFFF	SDH_BA	SD HOST Control Registers
0x4001_0000 – 0x4001_0FFF	EBI_BA	External Bus Interface Control Registers
0x4001_9000 – 0x4001_9FFF	USBD_BA	USB device Control Registers
0x4003_0000 – 0x4003_0FFF	CAP_BA	Image Capture interface Registers
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers
0x5000_8000 – 0x5000_FFFF	CRYP_BA	Cryptographic Accelerator Registers
APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_0FFF	WDT_BA	Watchdog Timer Control Registers
0x4004_1000 – 0x4004_1FFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4004_3000 – 0x4004_3FFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
0x4004_4000 – 0x4004_4FFF	EADC_BA	Enhance Analog-Digital-Converter (ADC) Control Registers
0x4004_5000 – 0x4004_5FFF	ACMP_BA	Analog Comparator Control Registers
0x4004_6000 – 0x4004_6FFF	OPA_BA	OP Amplifier Control Registers
0x4004_8000 – 0x4004_8FFF	I2S0_BA	I^2S0 Interface Control Registers
0x4004_9000 – 0x4004_9FFF	I2S1_BA	I^2S1 Interface Control Registers
0x4004_D000 – 0x4004_DFFF	OTG_BA	USB OTG
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers

0x4005_8000 – 0x4005_8FFF	PWM0_BA	PWM0_0/1/2/3/4/5 Control Registers
0x4005_9000 – 0x4005_9FFF	PWM1_BA	PWM1_0/1/2/3/4/5 Control Registers
0x4005_C000 – 0x4005_CFFF	EPWM0_BA	Enhanced PWM0_0/1/2/3/4/5 Control Registers
0x4005_D000 – 0x4005_DFFF	EPWM1_BA	Enhanced PWM1_0/1/2/3/4/5 Control Registers
0x4006_0000 – 0x4006_0FFF	SPI0_BA	SPI0 with Master/Slave function Control Registers
0x4006_1000 – 0x4006_1FFF	SPI1_BA	SPI1 with Master/Slave function Control Registers
0x4006_2000 – 0x4006_2FFF	SPI2_BA	SPI2 with Master/Slave function Control Registers
0x4006_3000 – 0x4006_3FFF	SPI3_BA	SPI3 with Master/Slave function Control Registers
0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4007_1000 – 0x4007_1FFF	UART1_BA	UART1 Control Registers
0x4007_2000 – 0x4007_2FFF	UART2_BA	UART2 Control Registers
0x4007_3000 – 0x4007_3FFF	UART3_BA	UART3 Control Registers
0x4007_4000 – 0x4007_4FFF	UART4_BA	UART4 Control Registers
0x4007_5000 – 0x4007_5FFF	UART5_BA	UART5 Control Registers
0x4008_0000 – 0x4008_0FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4008_1000 – 0x4008_1FFF	I2C1_BA	I^2C1 Interface Control Registers
0x4008_2000 – 0x4008_2FFF	I2C2_BA	I^2C2 Interface Control Registers
0x4008_3000 – 0x4008_3FFF	I2C3_BA	I^2C3 Interface Control Registers
0x4008_4000 – 0x4008_4FFF	I2C4_BA	I^2C4 Interface Control Registers
0x4009_0000 – 0x4009_0FFF	SC0_BA	Smartcard0 Control Registers
0x4009_1000 – 0x4009_1FFF	SC1_BA	Smartcard1 Control Registers
0x4009_2000 – 0x4009_2FFF	SC2_BA	Smartcard2 Control Registers
0x4009_3000 – 0x4009_3FFF	SC3_BA	Smartcard3 Control Registers
0x4009_4000 – 0x4009_4FFF	SC4_BA	Smartcard4 Control Registers
0x4009_5000 – 0x4009_5FFF	SC5_BA	Smartcard5 Control Registers
0x400A_0000 – 0x400A_0FFF	CAN0_BA	CAN0 Bus Control Registers
0x400A_1000 – 0x400A_1FFF	CAN1_BA	CAN1 Bus Control Registers
0x400B_0000 – 0x400B_0FFF	QEI0_BA	Quadrature Encoder Interface 0 Control Registers
0x400B_1000 – 0x400B_1FFF	QEI1_BA	Quadrature Encoder Interface 1 Control Registers
0x400B_0000 – 0x400B_0FFF	ECAP0_BA	Capture Engine 0 Control Registers
0x400B_1000 – 0x400B_1FFF	ECAP1_BA	Capture Engine 1 Control Registers
0x400E_0000 – 0x400E_0FFF	PS2_BA	PS/2 interface Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers

0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-1 Address Space Assignments for On-Chip Controllers

6.2.5 SRAM Memory Organization

The NUC442 series supports embedded SRAM with total 64 Kbytes size and the SRAM organization is separated to two banks: SRAM bank0 (16 Kbytes) and SRAM bank1 (48 Kbytes). Each of these two banks address space and can be accessed simultaneously.

- Supports total 64 Kbytes SRAM
- Supports byte / half word / word write
- Supports SRAM bank0 / SRAM bank1 for independent access
- Supports parity error check function on SRAM bank0 full range, and SRAM bank1 first 8 Kbytes range
- Supports oversize response error
- Supports remap address to 0x1000_0000

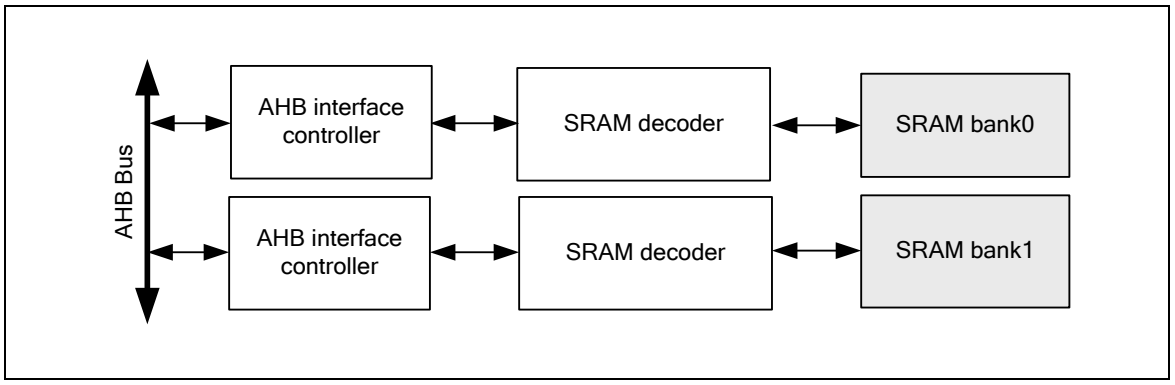


Figure 6.2-2 SRAM Block Diagram

Figure 6.2-3 shows the SRAM organization of NUC442 series. The bank0 address space is from 0x2000_0000 to 0x2000_3FFF. The bank1 address space is from 0x2000_4000 to 0x2000_FFFF. The address between 0x2001_0000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

The address of each bank is remapping from 0x2000_0000 to 0x1000_0000. CPU can access SRAM bank0 through 0x2000_0000 to 0x2000_3FFF or 0x1000_0000 to 0x1000_3FFF, and access SRAM bank1 through 0x2000_4000 to 0x2000_FFFF or 0x1000_4000 to 0x1000_FFFF

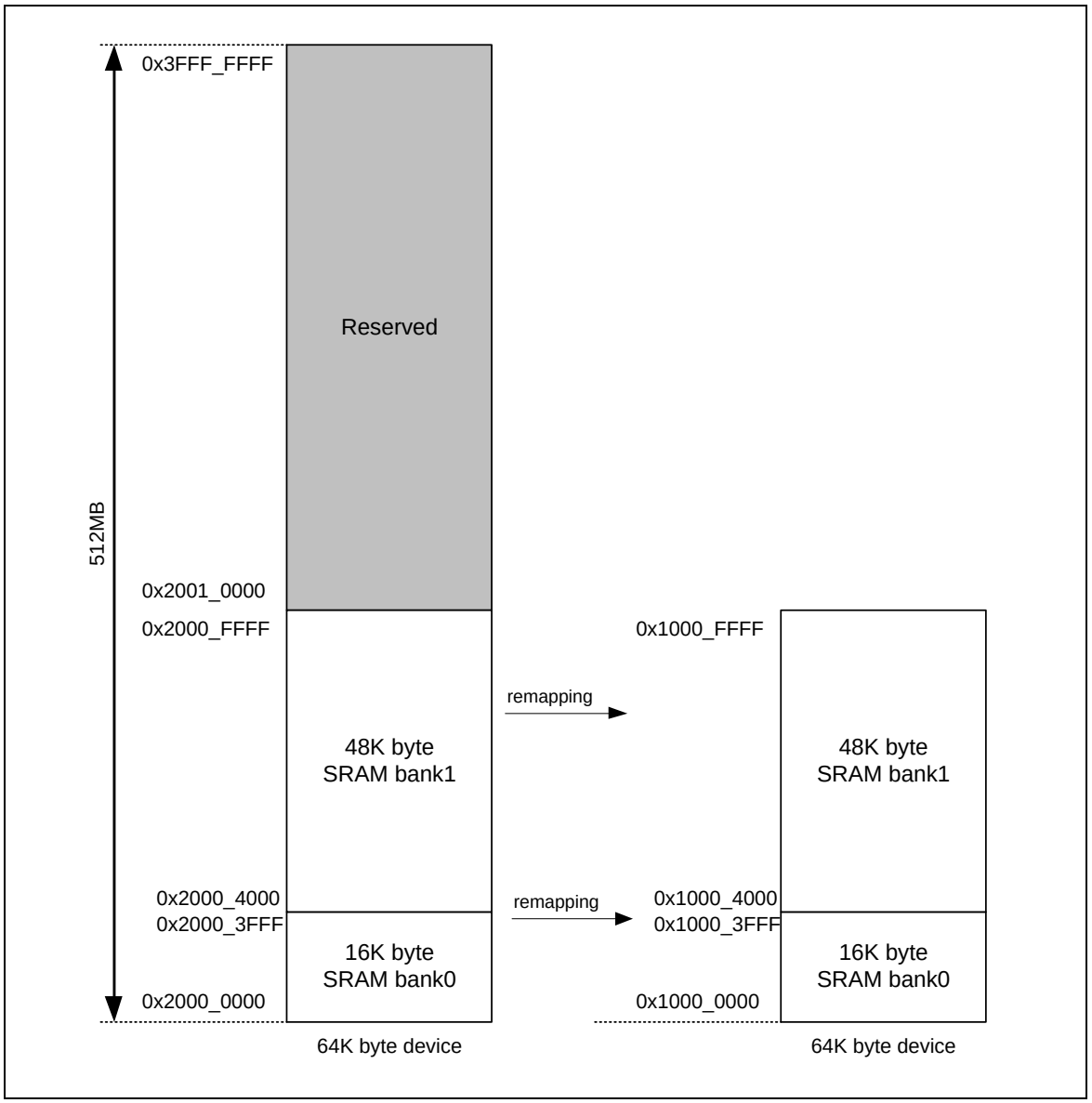


Figure 6.2-3 SRAM Memory Organization

First 24 Kbytes of SRAM has byte parity error check function. When CPU is accessing SRAM address (0x2000_0000 – 0x2000_5FFF), the parity error checking mechanism is dynamic operating. As bank0 parity error occured, the PERRIF (SYS_SRAM_STATUS[0]) will be asserted to 1, bank1 parity error occured, the PERRIF (SYS_SRAM_STATUS[1]) will be asserted to 1 and the SYS_SRAM0_ERRADDR register will record the address with parity error of bank0,

SYS_SRAM1_ERRADDR register will record the address with parity error of bank1 .Chip will enter interrupt when SRAM parity error occurred if PERRIEN (SYS_SRAM_INTCTL[0]) is set to 1. When SRAM parity error occured, chip will stop detecting SRAM parity error until user writes 1 to clear the PERRIF (SYS_SRAM_STATUS[0]) bit.

6.2.6 System Timer (SysTick)

The Cortex®-M4 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "*ARM® Cortex®-M4 Technical Reference Manual*" and "*ARM® v6-M Architecture Reference Manual*".

6.2.7 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

- An implementation-defined number of interrupts, in the range 1-240 interrupts.
- A programmable priority level of 0-16 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

6.2.7.1 Exception Model and System Interrupt Map

The following table lists the exception model supported by NUC4xx series. Software can set 16 levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0x00” and the lowest priority is denoted as “0xF0” (The 4-LSB always 0). The default priority of all the user-configurable interrupts is “0x00”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. On system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the VTOR to relocate the vector table start address to a different memory location, in the range 0x00000080 to 0x3FFFFF80,

The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Exception Type	Vector Number	Vector Address	Priority
Reset	1	0x00000004	-3
NMI	2	0x00000008	-2
Hard Fault	3	0x0000000C	-1
Memory Manager Fault	4	0x00000010	Configurable
Bus Fault	5	0x00000014	Configurable
Usage Fault	6	0x00000018	Configurable
Reserved	7 ~ 10		Reserved
SVCall	11	0x0000002C	Configurable
Debug Monitor	12	0x00000030	Configurable
Reserved	13		Reserved
PendSV	14	0x00000038	Configurable
SysTick	15	0x0000003C	Configurable
Interrupt (IRQ0 ~ IRQ)	16 ~ 144	0x00000000 + (Vector Number)*4	Configurable

Table 6.2-2 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BOD_OUT	Brown-Out low voltage detected interrupt
17	1	IRC_INT	IRC TRIM interrupt
18	2	PWRWU_INT	Clock controller interrupt for chip wake-up from power down state
19	3	SRAMF	SRAM parity check fail
20	4	CLKF	Clock detection fail

21	5	-	Reserved
22	6	RTC_INT	Real time clock interrupt
23	7	TAMPER	TAMPER interrupt
24	8	EINT0	External signal interrupt from PA.0 pin
25	9	EINT1	External signal interrupt from PB.0 pin
26	10	EINT2	External signal interrupt from PC.0 pin
27	11	EINT3	External signal interrupt from PD.0 pin
28	12	EINT4	External signal interrupt from PE.0 pin
29	13	EINT5	External signal interrupt from PF.0 pin
30	14	EINT6	External signal interrupt from PG.0 pin
31	15	EINT7	External signal interrupt from PH.0 pin
32	16	GPA_INT	External signal interrupt from PI.0 pin
33	17	GPB_INT	External signal interrupt from PA[15:1]
34	18	GPC_INT	External signal interrupt from PB[15:1]
35	19	GPD_INT	External signal interrupt from PC[15:1]
36	20	GPE_INT	External signal interrupt from PD[15:1]
37	21	GPF_INT	External signal interrupt from PE[15:1]
38	22	GPG_INT	External signal interrupt from PF[15:1]
39	23	GPH_INT	External signal interrupt from PG[15:1]
40	24	GPI_INT	External signal interrupt from PH[15:1]
41	25	GPJ_INT	External signal interrupt from PI[15:1]
42 ~ 47	26 ~ 31	-	Reserved
48	32	TMR0_INT	Timer 0 interrupt
49	33	TMR1_INT	Timer 1 interrupt
50	34	TMR2_INT	Timer 2 interrupt
51	35	TMR3_INT	Timer 3 interrupt
52 ~ 55	36 ~ 39	-	Reserved
56	40	PDMA_INT	PDMA interrupt
57	41	-	Reserved
58	42	ADC_INT	ADC interrupt
59 ~ 61	43 ~ 45	-	Reserved
62	46	WDT_INT	Watchdog Timer interrupt
63	47	WWDG_INT	Window Watchdog Timer interrupt
64	48	EADC0	Enhanced ADC 0 interrupt
65	49	EADC1	Enhanced ADC 1 interrupt

66	50	EADC2	Enhanced ADC 2 interrupt
67	51	EADC3	Enhanced ADC 3 interrupt
68 ~ 71	52 ~ 55	-	Reserved
72	56	ACMP_INT	Analog Comparator-0 or Comaprator-1 interrupt
73 ~ 75	57 ~ 59	-	Reserved
76	60	OPA0_INT	Analog OP0 interrupt
77	61	OPA1_INT	Analog OP1 interrupt
78	62	ICAP0	Internal Capture 0 interrupt
79	63	ICAP1	Internal Capture 1 interrupt
80	64	PWM0_0_INT	Internal Capture 1 interruptPWM0_0 interrupt
81	65	PWM0_1_INT	PWM0_1 interrupt
82	66	PWM0_2_INT	PWM0_2 interrupt
83	67	PWM0_3_INT	PWM0_3 interrupt
84	68	PWM0_4_INT	PWM0_4 interrupt
85	69	PWM0_5_INT	PWM0_5 interrupt
86	70	PWMABRK	PWMA BRK interrupt
87	71	QEI0	QEI0 interrupt
88	72	PWM1_0_INT	PWM1_0 interrupt
89	73	PWM1_1_INT	PWM1_1 interrupt
90	74	PWM1_2_INT	PWM1_2 interrupt
91	75	PWM1_3_INT	PWM1_3 interrupt
92	76	PWM1_4_INT	PWM1_4 interrupt
93	77	PWM1_5_INT	PWM1_5 interrupt
94	78	PWMBBRK	PWMB BRK interrupt
95	79	QEI1	QEI1 interrupt
96	80	EPWMA_INT	EPWMA interrupt
97	81	EPWMABRK	EPWMA brake interrupt
98	82	EPWMB_INT	EPWMB interrupt
99	83	EPWMBBRK	EPWMB brake interrupt
100 ~ 103	84 ~ 87	-	Reserved
104	88	UDC_INT	USB device interrupt
105	89	UHC_INT	USB host interrupt
106	90	OTG_INT	USB OTG interrupt
107 ~ 111	91 ~ 95	-	Reserved
112	96	SPI0_INT	SPI0 interrupt

113	97	SPI1_INT	SPI1 interrupt
114	98	SPI2_INT	SPI2 interrupt
115	99	SPI3_INT	SPI3 interrupt
116 ~ 119	100 ~ 103	-	Reserved
120	104	UART0_INT	UART0 interrupt
121	105	UART1_INT	UART1 interrupt
122	106	UART2_INT	UART2 interrupt
123	107	UART3_INT	UART3 interrupt
124	108	UART4_INT	UART4 interrupt
125	109	UART5_INT	UART5 interrupt
126 ~ 127	110 ~ 111	-	Reserved
128	112	I2C0_INT	I2C0 interrupt
129	113	I2C1_INT	I2C1 interrupt
130	114	I2C2_INT	I2C2 interrupt
131	115	I2C3_INT	I2C3 interrupt
132	116	I2C4_INT	I2C4 interrupt
133 ~ 135	117 ~ 119	-	Reserved
136	120	SC0	Smartcard 0 interrupt
137	121	SC1	Smartcard 1 interrupt
138	122	SC2	Smartcard 2 interrupt
139	123	SC3	Smartcard 3 interrupt
140	124	SC4	Smartcard 4 interrupt
141	125	SC5	Smartcard 5 interrupt
142 ~ 143	126 ~ 127	-	Reserved
144	128	CAN0_INT	CAN0 interrupt
145	129	CAN1_INT	CAN1 interrupt
146 ~ 147	130 ~ 131	-	Reserved
148	132	I2S_INT	I2S interrupt
149	133	I2S1_INT	I2S1 interrupt
150 ~ 151	134 ~ 135	-	Reserved
152	136	SDHOST	SD host interrupt
153	137	-	Reserved
154	138	PS2_INT	PS/2 interrupt
155	139	CAP	Image capture interface interrupt
156	140	CRYPTO	Crypto interrupt

Table 6.2-3 Interrupt Number Table

6.2.7.2 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in the section 6.2.7.3 of TRM.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the power-down enable bit (PWR_DOWN_EN) and Cortex®-M4 core executes the WFI/WFE instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high-speed crystal (HXT) and 22.1184 MHz internal high-speed oscillator (HIRC) to reduce the overall system power consumption. The following figures show the clock generator and the overview of the clock source control.

The clock generator consists of 6 clock sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLL source can be selected from 4~24 MHz external high speed crystal (HXT) or 22.1184 MHz internal high speed oscillator (HIRC)) (PLLFOUT)
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)
- 32.768 kHz external low speed crystal oscillator (LXT)
- USB PHY's PLL output clock frequency (PLL2FOUT)

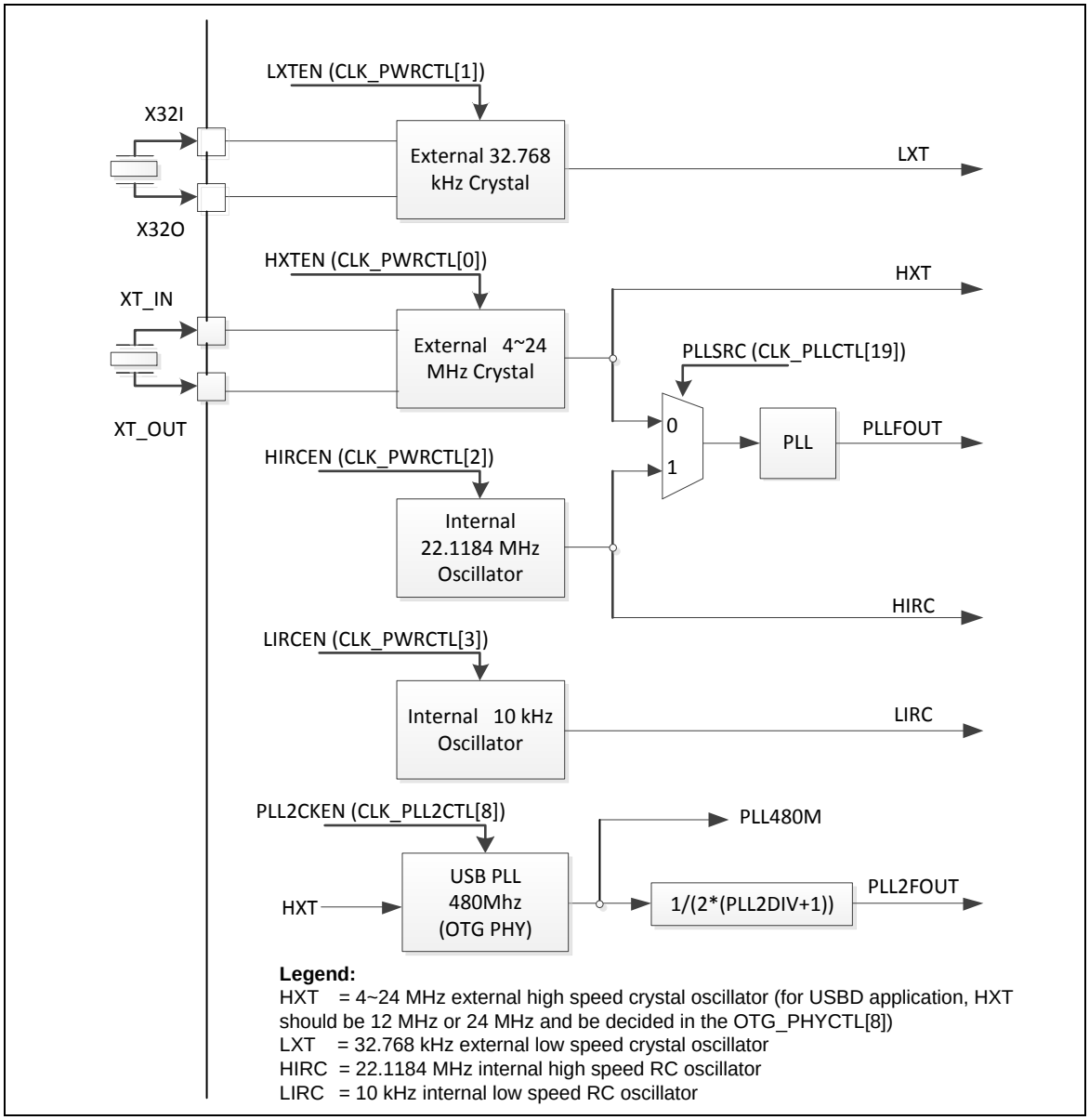


Figure 6.3-1 Clock Generator Block Diagram

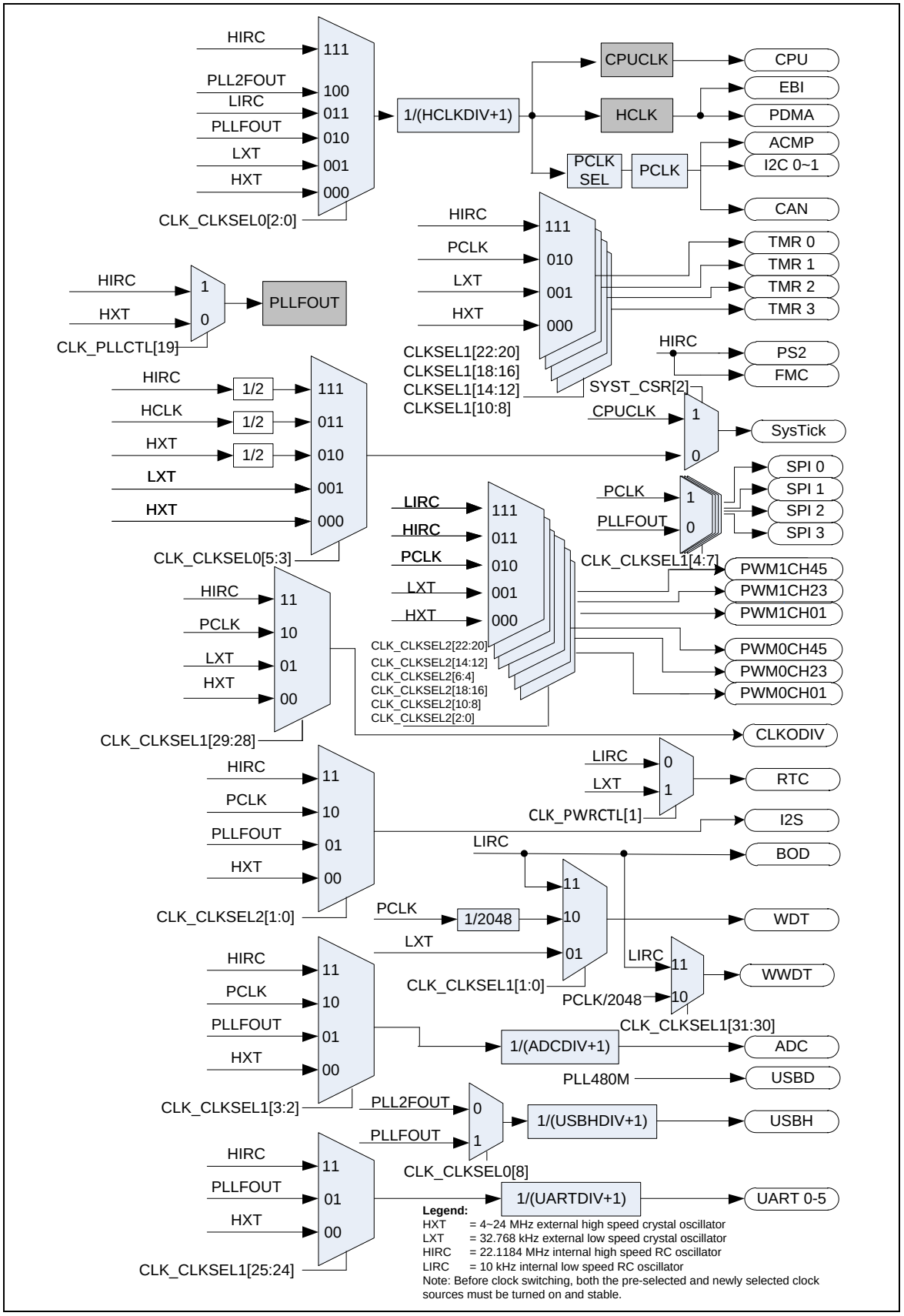


Figure 6.3-2 Clock Generator Global View Diagram

6.3.2 System Clock and SysTick Clock

The system clock has 6 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0 [2:0]). The block diagram is shown in the following figure.

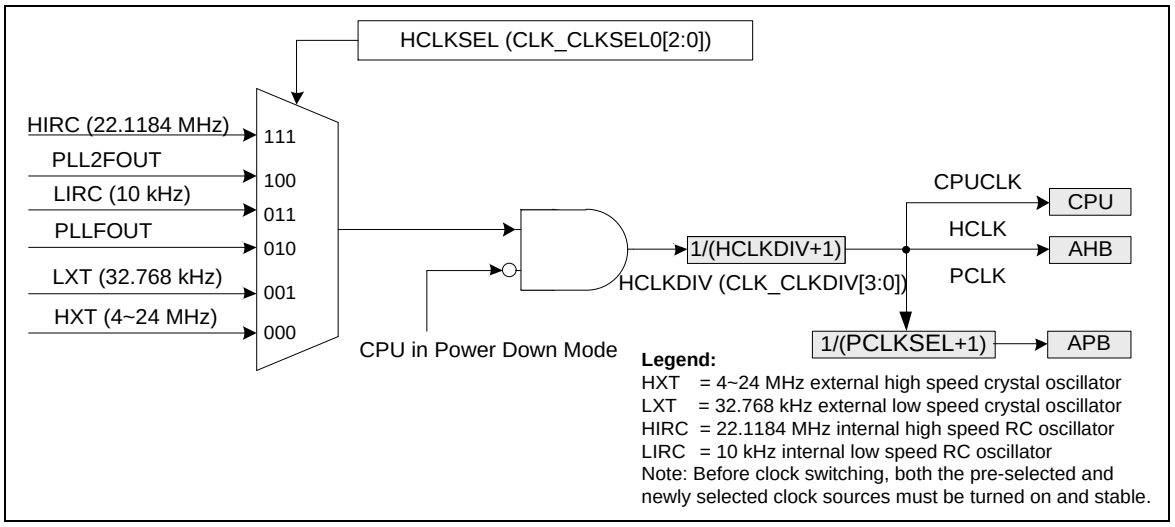


Figure 6.3-2 System Clock Block Diagram

6.3.3 Clock Monitor

The system clock has auto clock switch function to prevent system clock from being stopped. There are two clock detectors to monitor CPUCLK and HIRC and they have individual enable and interrupt control. The clock switch procedure is shown in the following figure. When any one detector is enabled, the LXT clock is enabled automatically. When the HIRC clock detector is enabled, the HIRC clock is enabled automatically.

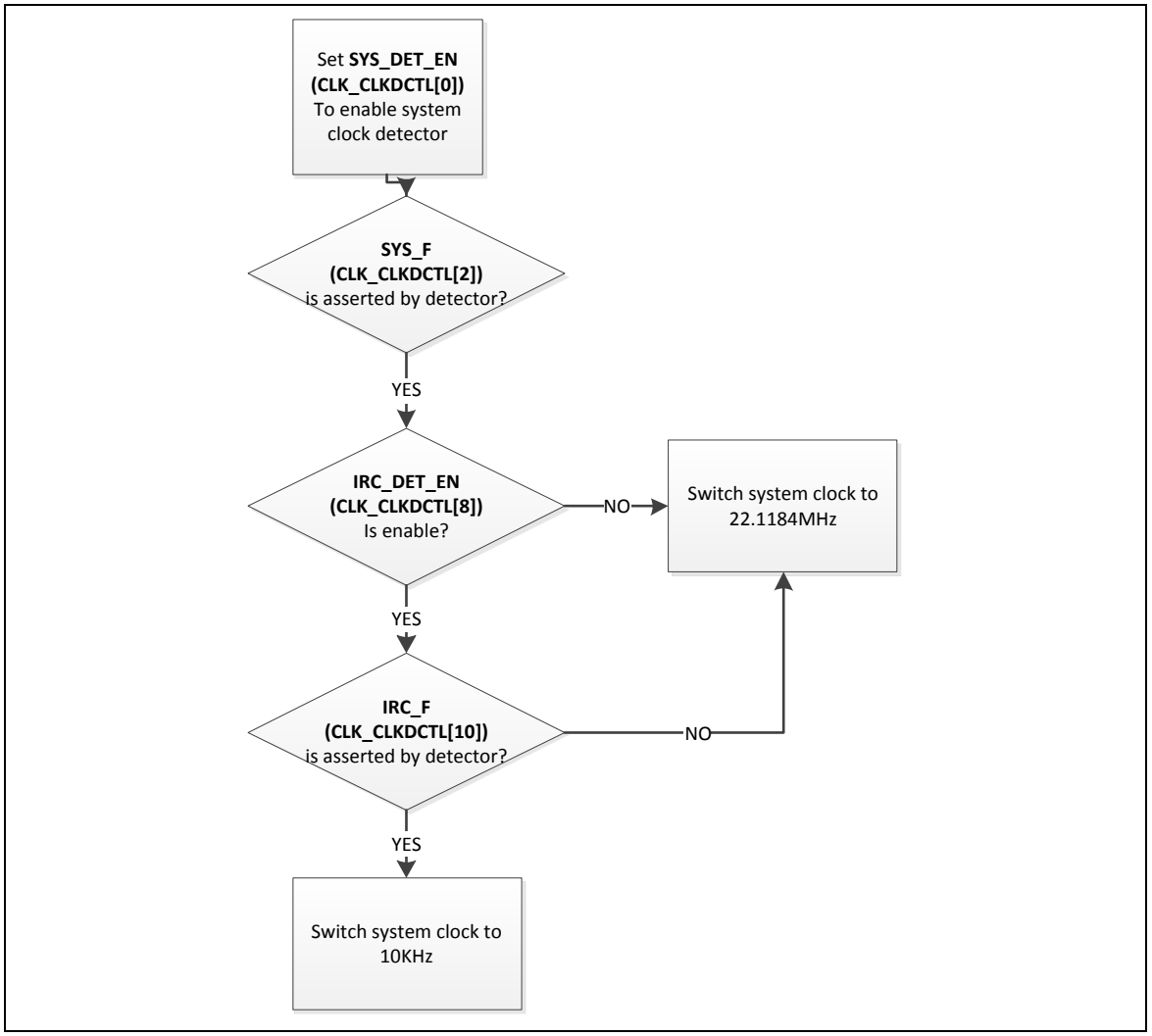


Figure 6.3-3 System Clock Switch Procedure

The clock source of SysTick in Cortex®-M4 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in the following figure.

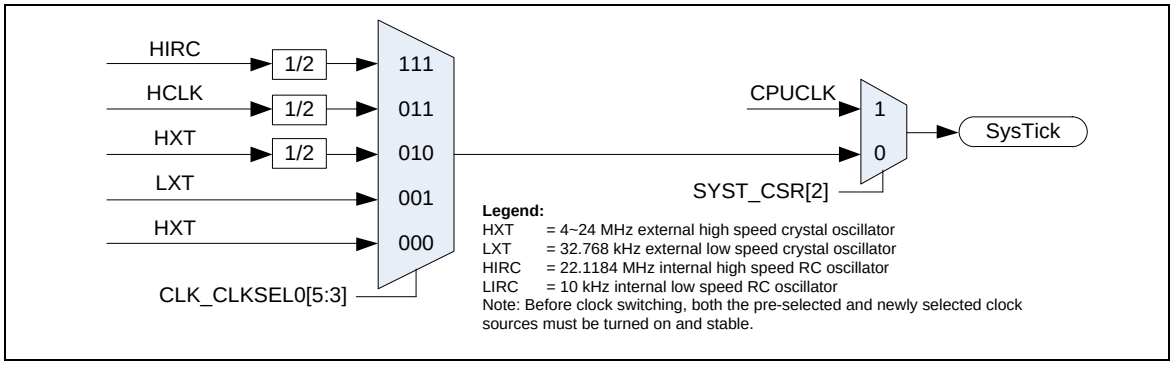


Figure 6.3-4 SysTick Clock Control Block Diagram

6.3.4 Peripherals Clock

The peripherals clock had different clock source switch setting, which depends on the different peripheral. Please refer the CLK_CLKSEL1 and CLK_CLKSEL2 register description in 5.3.7.

6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources, and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For theses clocks, which still keep active, are listed below:

- Clock Generator
  - 10 kHz internal low-speed oscillator(LIRC) clock
  - 32.768 kHz external low-speed crystal (LXT)clock
- Peripherals Clock (When these IP adopt 32.768 kHz external or 10 kHz low-speed oscillator as clock source)

6.3.6 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (CLK_CLKOCTL[3:0]).

When writing 1 to FDIVEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to FDIVEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

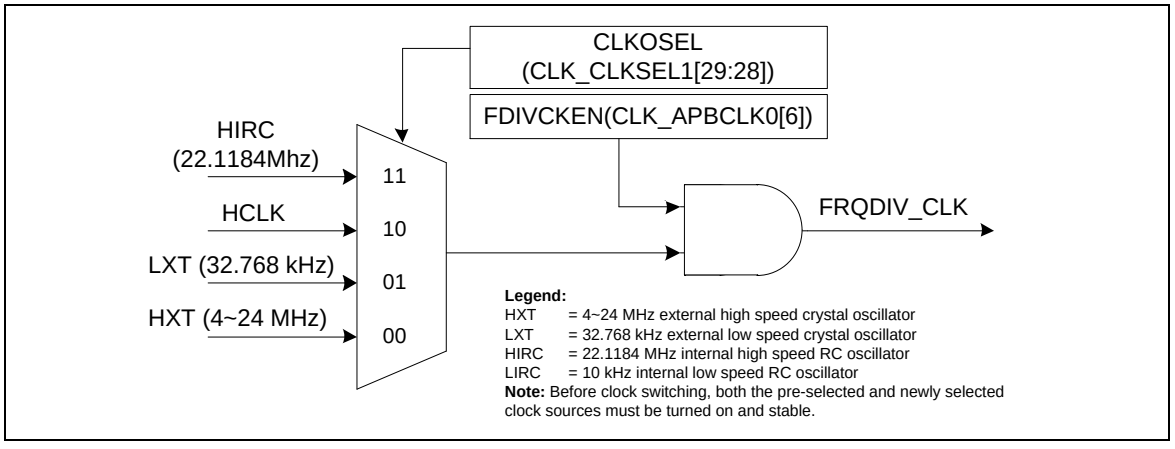


Figure 6.3-5 Clock Source of Frequency Divider

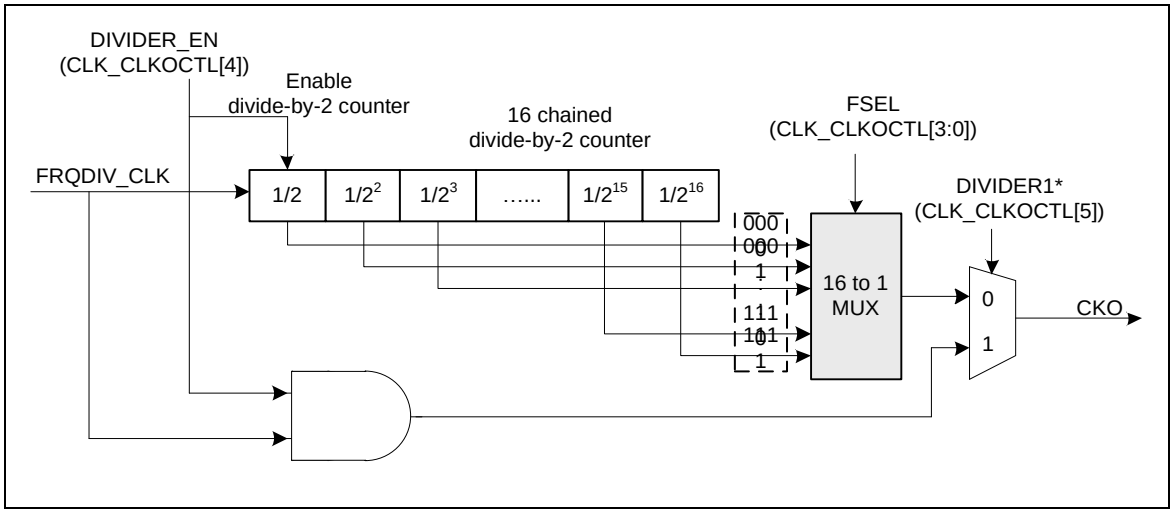


Figure 6.3-6 Block Diagram of Frequency Divider

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NUC442 is equipped with 256/512 Kbytes on-chip embedded flash for application program memory (APROM) and data flash that can be updated through ISP procedure. In-System-Programming (ISP) and In-Application-Programming (IAP) enables user to update chip embedded flash when chip is soldered on PCB. After chip is powered on, Cortex®-M4 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, the NUC442 also provides Data Flash for user to store some application dependent data before chip is powered off.

The NUC442 supports another flexible feature: configurable data flash size. The data flash size is decided by data flash enable (DFEN) in Config0 and data flash base address (DFBADR) in Config1. When DFEN is set to 1, the data flash size is zero. When DFEN is set to 0, the APROM and data flash share 256/512 Kbytes continuous address and the start address of data flash is defined by (DFBADR) in Config1.

6.4.2 Features

- Runs up to 84 MHz with zero wait state for continuous address read access
- 256/512 Kbytes application program memory (APROM) and data flash
- 16 Kbytes in system programming (ISP) loader program memory (LDROM)
- Configurable Data flash size with 2 Kbytes page erase unit
- Flash write protect size with 16 Kbytes per block unit
- User Configuration memory with CRC checking
- In System Program (ISP) /In Application Program (IAP) to update on chip Flash

6.5 External Bus Interface (EBI)

6.5.1 Overview

The NUC442 series is equipped with an external bus interface (EBI) for external device use. To minimize the connections between external device and this chip, EBI supports address bus and data bus multiplex mode. Also, the address latch enable (ALE) signal supported differentiate the address and data cycle.

In consideration of pin resource, address and Data separate mode can improve the EBI performance and save the address latch.

6.5.2 Features

External Bus Interface has the following functions:

- Four chip selects (nCS[0]~nCS[3])
- External devices with max. 32M-byte (8-bit data width)/64M-byte (16-bit data width) addressable space supported for each chip select (nCS[x])
- Variable external bus base clock (MCLK)
- 8-bit or 16-bit data width are supported for each chip select (nCS[x])
- Variable data access time (tACC), address latch enable time (tALE) and address hold time (tAHD) supported for each chip select (nCS[x])
- Address bus and data bus multiplex mode supported to save the address pins
- Address bus and data bus separate mode supported to have better performance
- Configurable idle cycle supported for different access condition: Write command finish (W2X), Read-to-Read (R2R) and Read-to-Write(R2W)

6.6 General Purpose I/O (GPIO)

6.6.1 Overview

The NUC442 series has up to 114 General Purpose I/O pins shared with other function pins depending on the chip configuration. These 114 pins are arranged in 8 ports named GPIOA, GPIOB, GPIOC, GPIOD, GPIOE, GPIOF, GPIOG and GPIOH. GPIO has 16 pins on echo port. Each one of the 114 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or quasi-bidirectional mode. After reset, the I/O type of all pins stay in quasi-bidirectional mode and port data register Px_DOUT[15:0] resets to 0x0000_FFFF. Each I/O pin has a very weak individual pull-up resistor which is about 110 KΩ~300 KΩ for V_{DD} is from 5.0 V to 2.5 V.

6.6.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Driver and High Sink IO mode

6.7 PDMA Controller (PDMA)

6.7.1 Overview

The direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can module transfers data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controllers have a total of 16 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.7.2 Features

- Supports 16 independently configurable channels.
- Selectable 2 level of priority (fixed priority or round-robin priority).
- Data size of 8, 16, and 32 bits.
- Source and destination address increment size by byte, half-word, word or no increment.
- Supports software or peripheral request, and the request type can be single or burst.
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table.

6.8 Timer Controller (TIMER)

6.8.1 Overview

The Timer Controller includes four 32-bit timers, TIMER0 ~ TIMER3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.8.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Time-out period = (Period of timer clock input) * (8-bit prescale counter + 1) * CMPDAT (TIMERx_CMP[23:0])
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- 24-bit up counter value is readable through TIMERx_CNT (Timer Data Register)
- Supports event counting function to count the event from external pin (TM0~TM3)
- Supports external capture pin (TM0_EXT~TM3_EXT) for interval measurement
- Supports external capture pin (TM0_EXT~TM3_EXT) to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated

6.9 PWM Generator and Capture Timer (PWM)

6.9.1 Overview

The NUC442 has two PWM generators — PWM0 and PWM1. PWM0 supports 6 channels PWM output or 6 channels input capture, and these two functions share the same pins (PWM0_CH0/ PWM0_CH1/PWM0_CH2/PWM0_CH3/PWM0_CH4/PWM0_CH5). PWM1 also supports 6 channels PWM output or 6 channels input capture, and these two functions share the same pins (PWM1_CH0/PWM1_CH1/PWM1_CH2/ PWM1_CH3/PWM1_CH4/PWM1_CH5).

The PWM generator has 16-bit PWM counter and comparator, and the PWM counter supports edge-aligned or center-aligned operating types. The PWM generator supports two standard PWM output modes: Independent output mode and Complementary output mode with 8-bit Dead-zone generator. In addition, PWM generator supports two special output mode: Synchronize mode and Group mode. It also has 8-bit prescaler and clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16) to support wide range clock frequency of PWM counter. For PWM output control unit, it supports polarity output function, independent pin mask function and brake function. PWM generator can send ADC start trigger signal if one of the following conditions happened: PWM counter period point, PWM counter center point, PWM output rising edge and PWM output falling edge.

The PWM generator also supports input capture function. It supports latch PWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.9.2 Features

6.9.2.1 PWM function features

- Supports 12 PWM output channels with 16-bit resolution
- Supports 8-bit prescaler and clock divider
- Supports period point, center point and edge point PWM Interrupt
- Supports One-shot or Auto-reload PWM counter operation mode
- Supports Edge-aligned or Center-aligned PWM counter type
- Supports 8-bit dead zone with maximum divided 16 prescaler
- Supports brake function source from pin or comparator output
- Supports mask function for each PWM pin
- Supports independent, complementary, synchronized and group PWM output mode
- Supports trigger ADC start conversion at PWM counter period point, PWM counter center point, PWM output rising edge and PWM output falling edge

6.9.2.2 Capture Function Features

- Supports 12 Capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports capture interrupt

6.10 Enhanced PWM Generator (EPWM)

6.10.1 Overview

This device is built in two PWM units with the same architecture which function is specially designed for driving motor control applications. Using the PWM, input capture module and QEI controller with proper control flow by software can easily drive the 3-phase Brushless DC motor, 3-phase AC induction motor and DC motor.

6.10.2 Features

Each unit supports the features below:

- Three independent 16-bit PWM duty control units with maximum 6 port pins:
  - 3 independent PWM output:
    EPWM0_CH0, EPWM0_CH2 and EPWM0_CH4 for Unit 0
    EPWM1_CH0, EPWM1_CH2 and EPWM1_CH4 for Unit 1
  - 3 complementary PWM pairs, with each pin in a pair mutually complement to each other and capable of programmable dead-time insertion:
    (EPWMx_CH0, EPWMx_CH1), (EPWM_CMPDAT2, EPWMx_CH3) and (EPWMx_CH4, EPWMx_CH5) where x=0~1.
  - 3 synchronous PWM pairs, with each pin in a pair in-phase:
    (EPWMx_CH0, EPWMx_CH1), (EPWMx_CH2, EPWMx_CH3) and (EPWMx_CH4, EPWMx_CH5) where x=0~1
- Group control bits:
  EPWMx_CH2 and EPWMx_CH4 are synchronized with EPWMx_CH0
- Supports Edge aligned mode and Center aligned mode
- Programmable dead-time insertion between complementary paired PWMs
- Each pin of EPWMx_CH0 to EPWMx_CH5 has independent polarity setting control
- Mask output control for Electrically Commutated Motor operation
- Tri-state output at reset and brake state
- Hardware brake protection
- Two Interrupt Sources:
  - Interrupt is synchronously requested at PWM frequency when up/down counter comparison matched (edge and center aligned modes) or underflow (center aligned mode).
  - Interrupt is requested when external brake pins asserted
- PWM signals before polarity control stage are defined in the view of positive logic. The PWM ports is active high or active low are controlled by polarity control register.
- High Source/Sink current.

After CPU reset the internal output of the each PWM channels depends on the polarity setting. The interval between successive outputs is controlled by a 16–bit up/down counter which uses a software selectable clock source with configurable internal clock pre-scalar as its input. The PWM counter clock has the frequency as the clock source F_{PWM} = EPWMx_CLK/Pre-scalar; Here the EPWMx_CLK synchronized with CPU clock HCLK.

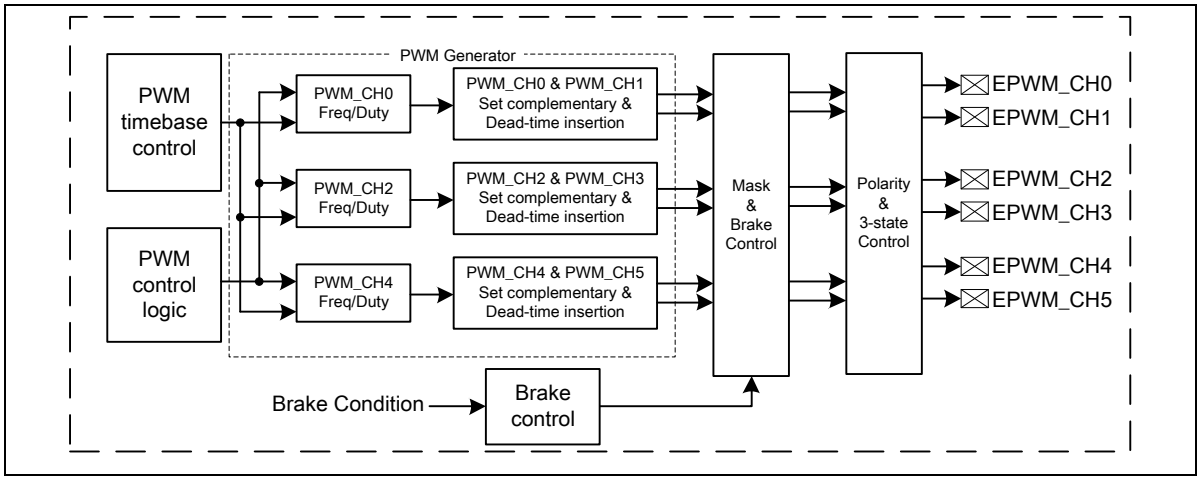


Figure 6.10-1 PWM Block Diagram

6.11 Enhanced Input Capture Timer

6.11.1 Overview

This device provides up to two units of Input Capture Timer/Counter which capture function can detect the digital edge changed signal at channel inputs. Each unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

6.11.2 Features

- Up to two Input Capture Timer/Counter Units, Input Capture 0 and Input Capture 1.
- Each unit has own interrupt vector.
- 24-bit Input Capture up-counting timer/counter
- With noise filter in front end of input ports.
- Edge detector with three options:
  - Rising edge detection
  - Falling edge detection
  - Both edge detection
- Each input channel is supported one capture counter hold register.
- Captured event reset/reload capture counter option.
- Supports compare-match function.

6.12 Quadrature Encoder Interface (QEI)

6.12.1 Overview

There are two QEI controllers in this device. The Quadrature Encoder Interface (QEI) decodes speed of rotation and motion sensor information. It can be used in any application that uses a quadrature encoder for feedback.

6.12.2 Features

- Up to two QEI controllers, QEI0 and QEI1.
- Two QEI phase inputs, QEA and QEB; One Index input.
- One QEI control register (QEI_CTL) and one QEI Status Register (QEI_STATUS)
- Four Quadrature encoder pulse counter operation modes:
  - Mode0: x4 free-counting mode
  - Mode1: x2 free-counting mode
  - Mode2: x4 compare-counting mode
  - Mode3: x2 compare-counting mode
- Encoder Pulse Width measurement mode

6.13 Watchdog Timer (WDT)

6.13.1 Overview

The Watchdog Timer is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.13.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval.
- Selectable time-out interval (2^4 ~ 2^{18}) and the time-out interval is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable Watchdog Timer reset delay period, including (1024+2)、(128+2) 、(16+2) or (1+2) WDT_CLK reset delay period.
- Supports force Watchdog Timer enabled after chip powered on or reset while CWDTEN (Config0[31] watchdog enable) bit is set to 0.
- Supports Watchdog Timer time-out wake-up function when WDT clock source is selected as 10 kHz low-speed oscillator.

6.14 Window Watchdog Timer (WWDT)

6.14.1 Overview

The Window Watchdog Timer is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.14.2 Features

- 6-bit down counter (WWDT_CNT[5:0]) and 6-bit compare value (WWDT_CTL[21:16]) to make the window period flexible
- Selectable maximum 11-bit WWDT clock prescale (WWDT_CTL[11:8]) to make WWDT time-out interval variable

6.15 Real Time Clock (RTC)

6.15.1 Overview

The Real Time Clock (RTC) controller provides the real time clock and calendar information. The clock source of RTC controller is from an external 32.768 kHz low-speed crystal which connected at pins X32I and X32O (refer to pin Description) or from an external 32.768 kHz low-speed oscillator output fed at pin X32I. The RTC controller provides the real time clock (hour, minute, second) in RTC_TIME (RTC Time Loading Register) as well as calendar information (year, month, day) in RTC_CAL (RTC Calendar Loading Register). It also offers RTC alarm function that user can preset the alarm time in RTC_TALM (RTC Time Alarm Register) and alarm calendar in RTC_CALM (RTC Calendar Alarm Register). The data format of RTC time and calendar message are all expressed in BCD (Binary Coded Decimal) format.

The RTC controller supports periodic RTC Time Tick and Alarm Match interrupts. The periodic RTC Time Tick interrupt has 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second which are selected by RTC_TICK (RTC_TICK[2:0] Time Tick Register). When real time and calendar message in RTC_TIME and RTC_CAL are equal to alarm time and calendar settings in RTC_TALM and RTC_CALM, the ALMIF (RTC_INTSTS [0] RTC Alarm Interrupt Flag) is set to 1 and the RTC alarm interrupt signal is generated if the ALMIEN (RTC_INTEN [0] Alarm Interrupt Enable) is enabled.

Both RTC Time Tick and Alarm Match interrupt signal can cause chip to wake-up from Idle or Power-down mode if the corresponding interrupt enable bit (ALMIEN or TICKIEN) is set to 1 before chip enters Idle or Power-down mode.

6.15.2 Features

- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register
- Supports Leap Year indication in RTC_LEAPYEAR register
- Supports Day of the Week counter in RTC_WEEKDAY register
- Frequency of RTC clock source compensated by the RTC_FREQADJ register
- All time and calendar message expressed in BCD format
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Supports RTC Time Tick and Alarm Match interrupt
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated
- Supports 96 bytes spare registers to store user's important information
- Supports a tamper detect function to detect the transition of tamper detect pin

6.16 UART Interface Controller (UART)

The NUC442 provides up to six channels of Universal Asynchronous Receiver/Transmitters (UART). UART0 supports High-speed UART and UART1~5 perform Normal Speed UART, besides, all the UART channels support flow control function.

6.16.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function, LIN master/slave mode function and RS-485 mode functions. Each UART channel supports seven types of interrupts including transmitter FIFO empty interrupt (INT_THRE), receiver threshold level reaching interrupt (INT_RDA), line status interrupt (parity error or framing error or break interrupt) (INT_RLS), receiver buffer time-out interrupt (INT_TOUT), MODEM/Wake-up status interrupt (INT_MODEM), Buffer error interrupt (INT_BUF_ERR) and LIN interrupt (INT_LIN).

The UART0 is built-in with a 64-byte transmitter FIFO (TX_FIFO) and a 64-byte receiver FIFO (RX_FIFO) that reduces the number of interrupts presented to the CPU and the UART1~2 are equipped 16-byte transmitter FIFO (TX_FIFO) and 16-byte receiver FIFO (RX_FIFO). The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 4 error conditions (parity error, framing error, break interrupt and buffer error) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need.

All of the controllers support auto-flow control function that uses two low-level signals, /CTS (clear-to-send) and /RTS (request-to-send), to control the flow of data transfer between the UART and external devices (ex: Modem). When auto-flow is enabled, the UART is not allowed to receive data until the UART asserts /RTS to external device. When the number of bytes in the RX FIFO equals the value of RTSTRGLV (UART_FIFO [19:16]), the /RTS is de-asserted. The UART sends data out when UART controller detects /CTS is asserted from external device. If a valid asserted /CTS is not detected the UART controller will not send data out.

The UART controllers also provides Serial IrDA (SIR, Serial Infrared) function (User must set IrDA_EN (UART_FUNCSEL[1]) to enable IrDA function). The SIR specification defines a short-range infrared asynchronous serial transmission mode with one start bit, 8 data bits, and 1 stop bit. The maximum data rate is 115.2 Kbps (half duplex). The IrDA SIR block contains an IrDA SIR Protocol encoder/decoder. The IrDA SIR protocol is half-duplex only. So it cannot transmit and receive data at the same time. The IrDA SIR physical layer specifies a minimum 10ms transfer delay between transmission and reception. This delay feature must be implemented by software.

The alternate function of UART controllers is LIN (Local Interconnect Network) function. The LIN mode is selected by setting the LIN_EN bit (UART_FUNCSEL[0]). In LIN mode, one start bit and 8-bit data format with 1-bit stop bit are required in accordance with the LIN standard.

For the NUC442 series, another alternate function of UART controllers is RS-485 9-bit mode function, and direction control provided by RTS pin to implement the function by software. The RS-485 mode is selected by setting the UART_FUNCSEL register to select RS-485 function. The RS-485 driver control is implemented using the RTS control signal from an asynchronous serial port to enable the RS-485 driver. In RS-485 mode, many characteristics of the RX and TX are the same as UART.

6.16.2 Features

- Full duplex, asynchronous communications
- Separate receive / transmit 64/16 bytes (UART0/UART1~5) entry FIFO for data payloads

- Supports hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function
- Supports 8-bit receiver buffer time-out detection function
- UART0~5 can be served by the DMA controller
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8]) register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8-bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Support for 3-/16-bit duration
- Supports LIN function mode
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detect function for receiver
  - Supports master identifier field parity generation and slave identifier field parity check function
  - Supports LIN slave header reception function
  - Supports LIN slave automatic resynchronization function
  - Supports LIN slave header error detect function
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software direct enable control provided by RTS pin

6.17 Smart Card Host Interface (SC)

6.17.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

6.17.2 Features

- ISO-7816-3 T = 0, T = 1 compliant.
- EMV2000 compliant
- Up to six ISO-7816-3 ports
- Separates receive/transmit 4 byte entry FIFO for data payloads.
- Programmable transmission clock frequency.
- Programmable receiver buffer trigger level.
- Programmable guard time selection (11 ETU ~ 267 ETU).
- A 24-bit and two 8 bit counters for Answer to Request (ATR) and waiting times processing.
- Supports auto inverse convention function.
- Supports transmitter and receiver error retry and error number limitation function.
- Supports hardware activation sequence process.
- Supports hardware warm reset sequence process.
- Supports hardware deactivation sequence process.
- Supports hardware auto deactivation sequence when detected the card removal.
- Supports UART mode
  - Full duplex, asynchronous communications.
  - Separates receiving / transmitting 4 bytes entry FIFO for data payloads.
  - Supports programmable baud rate generator for each channel.
  - Supports programmable receiver buffer trigger level.
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting SC_EGT register.
  - Programmable even, odd or no parity bit generation and detection.
  - Programmable stop bit, 1 or 2 stop bit generation

6.18 PS/2 Device Controller (PS2D)

6.18.1 Overview

The PS/2 device controller provides basic timing control for PS/2 communication. All communication between the device and the host is managed through the CLK and DATA pins. Unlike PS/2 keyboard or mouse device controller, the received/transmit code needs to be translated as meaningful code by firmware. The device controller generates the CLK signal after receiving a request to send, but host has ultimate control over communication. DATA sent from the host to the device is read on the rising edge and DATA sent from device to the host is change after rising edge. A 16 bytes FIFO is used to reduce CPU intervention. Software can select 1 to 16 bytes for a continuous transmission.

6.18.2 Features

- Host communication inhibit and request to send detection
- Reception frame error detection
- Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
- Double buffer for data reception
- Software override bus

6.19 I²C Serial Interface Controller (Master/Slave)

6.19.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more details about I²C Bus Timing.

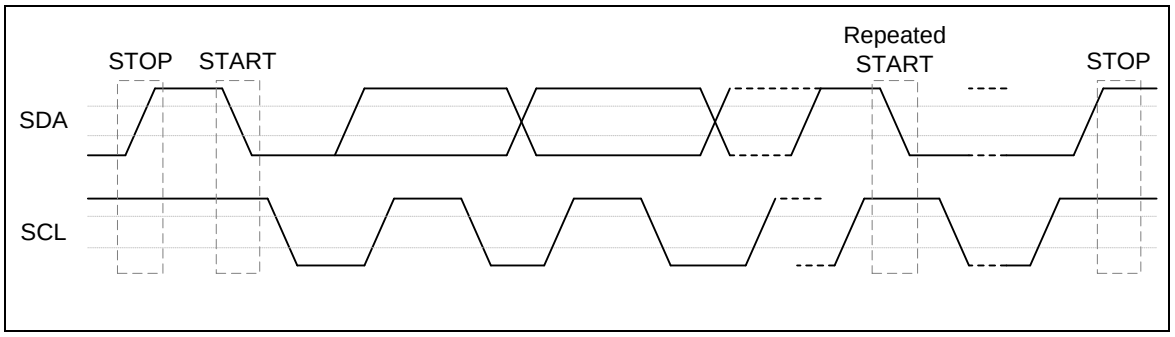


Figure 6.19-1 I²C Bus Timing

The device on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. To enable this port, the bit I2CEN (I2C_CTL[6]) should be set to '1'. The I²C H/W interfaces to the I²C bus via two pins: SDA and SCL. Pull up resistor is needed for I²C operation as these are open drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

6.19.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to stretch and un-stretch serial transfer
- Built-in a 14-bit time-out counter will request the I²C interrupt if the I²C bus hangs up and time-out counter overflows.
- Programmable divider allowing for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave addresses with mask option)
- Supports address match wakeup function

6.20 Serial Peripheral Interface (SPI)

6.20.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol that operates in full duplex mode. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The NUC442 series contains up to four sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each controller can be configured as a master or a slave device.

The SPI controller supports 2-bit Transfer mode to connect 2 off-chip slave devices at the same time. This controller also supports the PDMA function to access the data buffer and also supports Dual and Quad I/O Transfer mode.

6.20.2 Features

- Up to four sets of SPI controllers
- Supports Master or Slave mode operation
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode
- Configurable bit length of a transfer word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports byte reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface

6.21 I²S Controller (I²S)

6.21.1 Overview

The I²S controller consists of IIS protocol to interface with external audio CODEC. Two 8 word deep FIFO for read path and write path respectively and is capable of handling 8/16/24/32 bits word sizes. DMA controller handles the data movement between FIFO and memory.

6.21.2 Features

- Operates as either Master or Slave
- Capable of handling 8, 16, 24 and 32 bits word sizes
- Supports Mono and stereo audio data
- Supports I²S and MSB justified data format
- Provides two 8 word FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Two DMA requests, one for transmitting and the other for receiving

6.22 USB 2.0 Device Controller (USBD)

6.22.1 Overview

The USB device controller interfaces the AHB bus and the UTMI bus. The USB controller contains both the AHB master interface and AHB slave interface. CPU programs the USB controller registers through the AHB slave interface. For IN or OUT transfer, the USB device controller needs to write data to memory or read data from memory through the AHB master interface. The USB device controller is complaint with USB 2.0 specification and it contains 12 configurable endpoints in addition to control endpoint. These endpoints could be configured to BULK, INTERRUPT or ISO. The USB device controller has a built-in DMA to relieve the load of CPU.

6.22.2 Features

- USB Specification reversion 2.0 compliant
- Supports 12 configurable endpoints in addition to Control Endpoint
- Each of the endpoints can be Isochronous, Bulk or Interrupt and either IN or OUT direction
- Three different operation modes of an in-endpoint – Auto Validation mode, Manual Validation mode, Fly mode
- Supports DMA operation
- 4092 Bytes Configurable RAM used as endpoint buffer
- Supports Endpoint Maximum Packet Size up to 1024 bytes

6.23 USB 1.1 Host Controller (USBH)

6.23.1 Overview

The Universal Serial Bus (USB) is a low-cost, low-to-middle-speed peripheral interface standard intended for modem, scanners, PDAs, keyboards, mice, and other devices that do not require a high-bandwidth parallel interface. The USB is a 4-wire serial cable bus that supports serial data exchange between a Host Controller and one or several peripheral devices. The attached peripherals share USB bandwidth through a host-scheduled, token-based protocol. Peripherals may be attached, configured, used, and detached, while the host and other peripherals continue operation (i.e. hot plug and unplug is supported).

A major design goal of the USB standard is to allow flexible, plug-and-play networks of USB devices. In any USB network, there will be only one host, but there can be many devices and hubs.

6.23.2 Features

- Fully compliant with USB Revision 1.1 specification.
- Open Host Controller Interface (OHCI) Revision 1.0 compatible.
- Supports both full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt and Isochronous transfers.
- Supports two USB host ports:
  - USB Host port 1 is shared with USB device (OTG function).
  - USB Host port 2 is an independent host port. The port 2 host function can work even port1 functioned used as an USB device.
- Built-in DMA for real-time data transfer.
- Multiple low power modes for efficient power management.

6.24 USB OTG Controller

6.24.1 Overview

The USB OTG controller is used to interface USB OTG PHY and USB controller, either USB host controller or USB device controller. The USB OTG controller supports the HNP and SRP protocols defined in the On-The-Go and Embedded Host Supplement to the USB 2.0 Revision 1.3 Specification. Combining USB host controller, USB device controller and USB OTG controller can act as Host-only, Device-only, ID-dependent or OTG Device through setting. Host-only mode can support both full-speed and low-speed. Device-only mode only supports high-speed. ID-dependent mode and OTG Device mode supporting speed is dependent on current role.

6.24.2 Features

- Built-in OTG PHY to support protocols defined in On-The-GO Supplement Rev 1.3 Specification, Including:
  - HNP: Host Negotiation Protocol
  - SRP: Session Request Protocol
- Configurable to operate as:
  - Host-only
  - Device-only
  - ID dependent device
  - OTG device: A-device or B-device, depending on the ID pin status.

6.25 Controller Area Network (CAN)

6.25.1 Overview

The C_CAN consists of the CAN Core, Message RAM, Message Handler, Control Registers and Module Interface. The CAN Core performs communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks for acceptance filtering of received messages are stored in the Message RAM. All functions concerning the handling of messages are implemented in the Message Handler. These functions include acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the C_CAN can be accessed directly by the software through the module interface. These registers are used to control/configure the CAN Core and the Message Handler and to access the Message RAM.

6.25.2 Features

- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1 MBit/s
- 32 Message Objects
- Each Message Object has its own identifier mask
- Programmable FIFO mode (concatenation of Message Objects)
- Maskable interrupt
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation
- 16-bit module interfaces to the AMBA APB bus
- Supports wake-up function

6.26 Secure Digital Host Controller

6.26.1 Overview

The Secure Digital Host Controller (SD Host) has DMAC unit and SD unit. The DMAC unit provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer (128 bytes), and the SD unit controls the interface of SD/SDHC. The SDHOST controller can support SD/SDHC and cooperated with DMAC to provide a fast data transfer between system memory and cards.

6.26.2 Features

- AMBA AHB master/slave interface compatible, for data transfer and register read/write.
- Supports single DMA channel.
- Supports hardware Scatter-Gather function.
- Using single 128 Bytes shared buffer for data exchange between system memory and cards.
- Synchronous design for DMA with single clock domain, AHB bus clock (HCLK).
- Interface with DMAC for register read/write and data transfer.
- Supports SD/SDHC card.
- Completely asynchronous design for Secure Digital with two clock domains, HCLK and Engine clock, note that frequency of HCLK should be higher than the frequency of peripheral clock.

6.27 Cryptographic Accelerator

6.27.1 Overview

The Crypto (Cryptographic Accelerator) includes a secure pseudo random number generator (PRNG) core and supports AES, DES/TDES, and SHA algorithms.

The PRNG core supports 64 bits, 128 bits, 192 bits, and 256 bits random number generation.

The AES accelerator is an implementation fully compliant with the AES (Advance Encryption Standard) encryption and decryption algorithm. The AES accelerator supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, and CBC-CS3 mode.

The DES/TDES accelerator is an implementation fully compliant with the DES and Triple DES encryption/decryption algorithm. The DES/TDES accelerator supports ECB, CBC, CFB, OFB, and CTR mode.

The SHA accelerator is an implementation fully compliant with the SHA-160, SHA-224 and SHA-256.

6.27.2 Features

- PRNG
  - Supports 64 bits, 128 bits , 192 bits, and 256 bits random number generation
- AES
  - Supports FIPS NIST 197
  - Supports SP800-38A and addendum
  - Supports 128, 192, and 256 bits key
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB , CTR, CBC-CS1, CBC-CS2, and CBC-CS3 mode
  - Supports key expander
- DES
  - Supports FIPS 46-3
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, and CTR mode
- TDES
  - Supports FIPS NIST 800-67
  - Implemented according to the X9.52 standard
  - Supports two keys or three keys mode
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, and CTR mode
- SHA
  - Supports FIPS NIST 180, 180-2
  - Supports SHA-160, SHA-224, and SHA-256

6.28 Image Capture Interface (ICAP)

6.28.1 Overview

The Image Capture Interface is designed to capture image data from a sensor. After capturing or fetching image data, it will process the image data, and then FIFO outputs them into a frame buffer.

6.28.2 Features

- 8-bit RGB565 sensor
- 8-bit YUV422 sensor
- Supports CCIR601 YCbCr color range scale to full YUV color range
- Supports 4 packaging format for packet data output: YUYV, Y only, RGB565, RGB555
- Supports YUV422 planar data output
- Supports the CROP function to crop input image to the required size for digital application.
- Supports the down scaling function to scale input image to the required size for digital application.
- Supports frame rate control
- Supports field detection and even/odd field skip mechanism
- Supports packet output dual buffer control through hardware buffer controller
- Supports negative/sepia/posterization color effect
- Supports two independent capture interfaces

6.29 CRC Controller

6.29.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with programmable polynomial settings.

6.29.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

6.30 Analog-to-Digital Converter (ADC)

6.30.1 Overview

The NUC442 contains one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 12 external input channels. The A/D converter supports three operation modes — Single Mode, Single-cycle Scan Mode and Continuous Scan Mode. The A/D converters can be started by software, external pin (STADC) or PWM trigger.

6.30.2 Features

- Analog input voltage range: 0~Analog Supply Voltage from AV_{DD}
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 12 single-end analog input channels or 6 differential analog input channels.
- Supports conversion rate 400 kSPS while V_{REF} is between 2.5V~5.5V and up to 800 kSPS while V_{REF} is between 4.5V~5.5V in single-end mode.
- Supports conversion rate 800 kSPS while V_{REF} is between 2.5V~5.5V and up to 1 MSPS while V_{REF} is between 3.0V~5.5V in differential mode.
- Three operation modes
  - Single Mode: A/D conversion is performed one time on a specified channel
  - Single-cycle Scan Mode: A/D conversion is performed one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel
  - Continuous Scan Mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion
- An A/D conversion can be started by
  - Software write 1 to A/D conversion start bit (ADST)
  - External pin (STADC)
  - PWM trigger with optional start delay period
- Conversion results are held in data registers for each channel with valid and overrun indicators
- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result is larger than, smaller than or equal to the compare register setting
- Supports internal source: internal band-gap voltage, and internal temperature sensor output voltage
- Supports PDMA transfer

6.31 12-bit Analog-to-Digital Converter (Enhanced ADC)

6.31.1 Overview

The NUC442 series contains two 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 16 external input channels and 5 internal channels. The two A/D converters ADC0 and ADC1 can be sampled with simultaneous or single sampling mode. The A/D converters can be started by software, PWM triggers, timer0~3 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC pulse trigger and external pin (STADC) input signal.

6.31.2 Features

- Enhanced ADC mode with dual ADC
- Analog input voltage range: 0~Analog Supply Voltage from AV_{DD}.
- 12-bit resolution and 10-bit accuracy is guaranteed.
- Two SAR ADC converters, including ADC0 and ADC1
- Up to 16 single-end analog external input channels
- Up to 5 internal channels; ADC0 supports four internal channels, including temperature sensor, band-gap voltage, analog ground and OP amplifier 0; ADC1 supports only OP amplifier 1
- Four ADC interrupts with individual interrupt vectors
- Supports conversion rate 400 kSPS while V_{REF} is between 2.5V~5.5V and up to 800 kSPS while V_{REF} is between 4.5V~5.5V in single-end mode.
- Double buffer for channel 0~3 of each ADC0 and ADC1
- Two operating modes:
  - Single sampling mode: two ADC converters run at normal operation.
  - Simultaneous sampling mode: Allow two ADC converters can be sampled simultaneously.
- An A/D conversion can be started by:
  - Software write 1 to A/D start conversion bit (SWTRGx, x = 0~15)
  - External pin (STADC)
  - Timer0~3 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC pulse triggers
  - PWM triggers
- Conversion results are held in 16 data registers with valid and overrun indicators.
- Each of SAMPLE00~SAMPLE07 ADC control logic modules configurable for ADC0 converter channel ADC0_CH0~ADC0_CH7 and trigger source.
- Each of SAMPLE10~SAMPLE17 ADC control logic modules configurable for ADC1 converter channel ADC1_CH0~ADC1_CH7 and trigger source.
- ADC0 channel 8, 9, 10, 11 input sources as band-gap voltage, temperature sensor, analog ground and OP amplify 0.
- ADC1 channel 8 as OP amplify 1.

Note: if user configures bit 8 of VREFCR register to 1, the NUC442 ADC becomes Enhanced ADC mode with dual ADC, if user configure bit 8 of VREFCR register to 0, the NUC442 ADC become basic ADC mode with single ADC

6.32 Analog Comparator Controller (ACMP)

6.32.1 Overview

The NUC442 contains three comparators which can be used in a number of different configurations. The comparator output is a logical one when positive input is greater than negative input; otherwise, the output is zero. Each comparator can be configured to cause an interrupt when the comparator output value changes. The block diagram is shown below.

6.32.2 Features

- Analog input voltage range: 0 ~ AV_{DD}
- Supports hysteresis function
- Selectable input sources of positive input and negative input
- One ACMP interrupt vector for all comparators

6.33 OP Amplifier

6.33.1 Overview

This device integrated two operational amplifiers. It can be enabled through OPENx (OPA_CTL[1:0]) bits. User can measure the outputs of the OP amplifier as the OP amplifier output to the integrated EADC channel EADC0_11 and EADC1_8, where digital results can be taken.

6.33.2 Features

- Analog input voltage range: 0~AV_{DD}.
- Two analog OP amplifiers
- Software enabled to connect OP amplifier 0,1 outputs to A/D converter channel AINA[B], AINB[8] respectively
- Schmitt trigger buffer outputs of OP amplifier0, 1 can be as one of the comparator interrupt sources.
- OP amplifier 0 output can be an optional input source of integrated comparator 0 positive input
- OP amplifier 1 output can be an optional input source of integrated comparator 1 positive input

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{DD} - V_{SS}$	DC Power Supply	-0.3	+7.0	V
V_{BAT}	Battery Power Supply	+2.4	+5.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+105	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	400	mA
I_{SS}	Maximum Current out of V_{SS}	-	400	mA
I_{IO}	Maximum Current sunk by an I/O pin	-	35	mA
	Maximum Current sourced by an I/O pin	-	35	mA
	Maximum Current sunk by total I/O pins	-	240	mA
	Maximum Current sourced by total I/O pins	-	240	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

7.2 DC Electrical Characteristics

(V_{DD} - V_{SS} = 2.5 ~ 5.5 V, T_A = 25℃)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operation voltage	2.5	-	5.5	V	V_{DD} = 2.5 V ~ 5.5 V up to 84 MHz
V_{SS} / AV_{SS}	Power Ground	-0.3	-	-	V	
V_{LDO}	LDO Output Voltage	1.62	1.8	1.98	V	V_{DD} ≥ 2.5 V
V_{BG}	Band-gap Voltage	1.22	1.25	1.28	V	V_{DD} = 2.5 V ~ 5.5 V, T_A = 25℃
		1.18	1.25	1.32	V	V_{DD} = 2.5 V ~ 5.5 V, T_A = -40℃~105℃
V_{DD}-AV_{DD}	Allowed Voltage Difference for V_{DD} and AV_{DD}	-0.3	0	0.3	V	-
I_{DD1}	Operating Current Normal Run Mode HCLK = 84 MHz while(1){} Executed from Flash	-	116	-	mA	V_{DD} 5.5V; HXT 12 MHz; HIRC Disable; PLL Enabled; All digital modules Enabled
I_{DD2}		-	52	-	mA	V_{DD} 5.5V; HXT 12 MHz; HIRC Disabled; PLL Enabled; All digital modules Disabled
I_{DD3}		-	112	-	mA	V_{DD} 3.3V; HXT 12 MHz; HIRC Disable; PLL Enabled; All digital modules Enabled

I_{DD4}		-	50	-	mA	V_{DD} 3.3 V HXT 12 MHz HIRC Disabled PLL Enabled All digital modules Disabled
I_{DD5}	Operating Current Normal Run Mode HCLK =22.1184 MHz while(1){} Executed from Flash	-	32	-	mA	V_{DD} 5.5V HXT Disabled HIRC Enabled PLL Disabled All digital modules Enabled
I_{DD6}		-	13	-	mA	. V_{DD} 5.5V HXT Disabled HIRC Enabled PLL Disabled All digital modules Disabled
I_{DD7}		-	32	-	mA	V_{DD} 3.3V HXT Disabled HIRC Enabled PLL Disabled All digital modules Enabled
I_{DD8}		-	13	-	mA	V_{DD} 3.3V HXT Disabled HIRC Enabled PLL Disabled All digital modules Disabled

I_{DD9}	Operating Current Normal Run Mode HCLK = 12 MHz while(1){} Executed from Flash	-	21	-	mA	V_{DD} 5.5 V HXT 12 MHz HIRC Disabled PLL Disabled All digital modules Enabled
I_{DD10}		-	10	-	mA	V_{DD} 5.5 V HXT 12 MHz HIRC Disabled PLL Disabled All digital modules Disabled
I_{DD11}		-	19	-	mA	V_{DD} 3.3 V HXT 12 MHz HIRC Disabled PLL Disabled All digital modules Enabled
I_{DD12}		-	8.5	-	mA	V_{DD} 3.3 V HXT 12 MHz HIRC Disabled PLL Disabled All digital modules Disabled
I_{DD13}	Operating Current Normal Run Mode HCLK =4 MHz while(1){} Executed from Flash	-	9	-	mA	V_{DD} 5.5 V HXT 4 MHz HIRC Disabled PLL Disabled All digital modules Enabled
I_{DD14}		-	5	-	mA	V_{DD} 5.5 V HXT 4 MHz HIRC Disabled PLL Disabled All digital modules Disabled

I_{DD15}	Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Executed from Flash	-	7.5	-	mA	V_{DD} 3.3 V HXT 4 MHz HIRC Disabled PLL Disabled All digital modules Enabled
I_{DD16}		-	3.5	-	mA	V_{DD} 3.3 V HXT 4 MHz HIRC Disabled PLL Disabled All digital modules Disabled
I_{DD17}		-	364	-	µA	V_{DD} 5.5 V HXT Disabled HIRC Disabled LIRC Enabled PLL Disabled All digital modules Enabled Only enable modules which support 10 kHz LIRC clock source
I_{DD18}		-	354	-	µA	V_{DD} 5.5 V HXT Disabled HIRC Disabled LIRC Enabled PLL Disabled All digital modules Disabled

I_{DD19}	Operating Current Idle Mode HCLK = 84 MHz	-	206	-	µA	V_{DD} 3.3 V HXT Disabled HIRC Disabled LIRC Enabled PLL Disabled All digital modules Enabled Only enable modules which support 10 kHz LIRC clock source
I_{DD20}		-	196	-	µA	V_{DD} 3.3 V HXT Disabled HIRC Disabled LIRC Enabled PLL Disabled All digital modules Disabled
I_{IDLE1}		-	89	-	mA	V_{DD} 5.5V HXT 12 MHz HIRC Disable PLL Enabled All digital modules Enabled
I_{IDLE2}		-	22	-	mA	V_{DD} 5.5V HXT 12 MHz HIRC Disabled PLL Enabled All digital modules Disabled
I_{IDLE3}		-	87	-	mA	V_{DD} 3.3V HXT 12 MHz HIRC Disable PLL Enabled All digital modules Enabled

I_{IDLE4}	Operating Current Idle Mode HCLK =22.1184 MHz	-	21	-	mA	V_{DD} 3.3V HXT 12 MHz HIRC Disabled PLL Enabled All digital modules Disabled
I_{IDLE5}		-	24	-	mA	V_{DD} 5.5V HXT Disabled HIRC Enabled PLL Disabled All digital modules Enabled
I_{IDLE6}		-	5.5	-	mA	. V_{DD} 5.5V HXT Disabled HIRC Enabled PLL Disabled All digital modules Disabled
I_{IDLE7}		-	23.7	-	mA	V_{DD} 3.3V HXT Disabled HIRC Enabled PLL Disabled All digital modules Enabled
I_{IDLE8}		-	5.3	-	mA	V_{DD} 3.3V HXT Disabled HIRC Enabled PLL Disabled All digital modules Disabled

I_{IDLE9}	Operating Current Idle Mode HCLK =12 MHz	-	16.7	-	mA	V_{DD} 5.5 V HXT 12 MHz HIRC Disabled PLL Disabled All digital modules Enabled
I_{IDLE10}		-	5.4	-	mA	V_{DD} 5.5 V HXT 12 MHz HIRC Disabled PLL Disabled All digital modules Disabled
I_{IDLE11}		-	15	-	mA	V_{DD} 3.3 V HXT 12 MHz HIRC Disabled PLL Disabled All digital modules Enabled
I_{IDLE12}		-	3.8	-	mA	V_{DD} 3.3 V HXT 12 MHz HIRC Disabled PLL Disabled All digital modules Disabled
I_{IDLE13}	Operating Current Idle Mode HCLK =4 MHz	-	7.5	-	mA	V_{DD} 5.5 V HXT 4 MHz HIRC Disabled PLL Disabled All digital modules Enabled
I_{IDLE14}		-	3.5	-	mA	V_{DD} 5.5 V HXT 4 MHz HIRC Disabled PLL Disabled All digital modules Disabled

I_{IDLE15}	Operating Current Idle Mode at 10 kHz	-	6	-	mA	V_{DD} 3.3 V HXT 4 MHz HIRC Disabled PLL Disabled All digital modules Enabled
I_{IDLE16}		-	2	-	mA	V_{DD} 3.3 V HXT 4 MHz HIRC Disabled PLL Disabled All digital modules Disabled
I_{IDLE17}		-	360	-	µA	V_{DD} 5.5 V HXT Disabled HIRC Disabled LIRC Enabled PLL Disabled All digital modules Enabled Only enable modules which support 10 kHz LIRC clock source
I_{IDLE18}		-	350	-	µA	V_{DD} 5.5 V HXT Disabled HIRC Disabled LIRC Enabled PLL Disabled All digital modules Disabled

I_{IDLE19}		-	202	-	µA	V_{DD} 3.3 V HXT Disabled HIRC Disabled LIRC Enabled PLL Disabled All digital modules Enabled Only enable modules which support 10 kHz LIRC clock source
I_{IDLE20}		-	192	-	µA	V_{DD} 3.3 V HXT Disabled HIRC Disabled LIRC Enabled PLL Disabled All digital modules Disabled
I_{PWD1}	Standby Current Power-down Mode (Deep Sleep Mode)	-	60	100	µA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.
I_{PWD2}		-	55	95	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off.
I_{IL}	Logic 0 Input Current (Quasi-bidirectional Mode)	-	-65	-	µA	V_{DD} = 5.5 V, V_{IN} = 0V
I_{TL}	Logic 1 to 0 Transition Current (Quasi-bidirectional Mode) [*3]	-	-690	-750	µA	V_{DD} = 5.5 V, V_{IN} = 2.0V
I_{LK}	Input Leakage Current	-2	-	+2	µA	V_{DD} = 5.5 V, 0 < V_{IN} < V_{DD} Open-drain or input only mode
V_{IL1}	Input Low Voltage (TTL Input)	-0.3	-	0.8	V	V_{DD} = 4.5 V
		-0.3	-	0.6		V_{DD} = 2.5 V
V_{IH1}	Input High Voltage /4 (TTL Input)	2.0	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{IL3}	Input Low Voltage XTAL1[*2]	0	-	0.8	V	V_{DD} = 4.5 V
		0	-	0.4		V_{DD} = 2.5 V
V_{IH3}	Input High Voltage XTAL1[*2]	3.5	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		2.4	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{ILS}	Negative-going Threshold (Schmitt Input), nRST	-0.3	-	0.2 V_{DD}	V	-
V_{IHS}	Positive-going Threshold (Schmitt Input), nRST	0.7 V_{DD}	-	V_{DD} + 0.3	V	-
R_{RST}	Internal nRST Pin Pull-up Resistor	40		150	kΩ	-

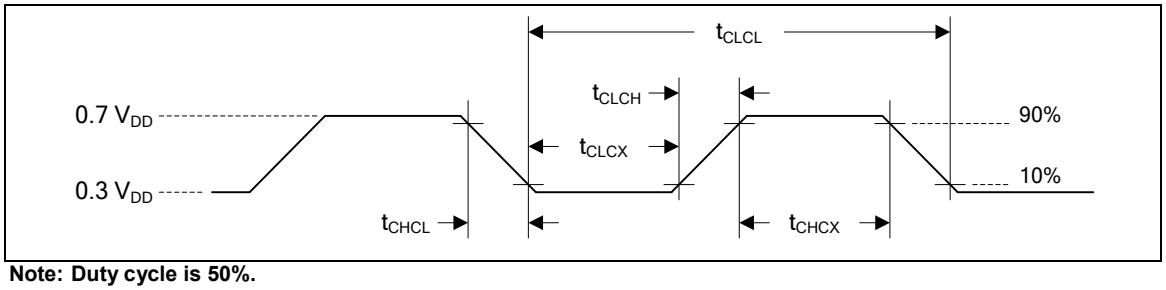
V_{ILS}	Negative-going Threshold (Schmitt input)	-0.3	-	0.3 V_{DD}	V	-
V_{IHS}	Positive-going Threshold (Schmitt input)	0.7 V_{DD}	-	V_{DD} + 0.3	V	-
I_{SR11}	Source Current (Quasi-bidirectional Mode)	-300	-370	-	μA	V_{DD} = 4.5 V, V_S = 2.4 V
I_{SR12}		-50	-70	-	μA	V_{DD} = 2.7 V, V_S = 2.2 V
I_{SR13}		-40	-60	-	μA	V_{DD} = 2.5 V, V_S = 2.0 V
I_{SR21}	Source Current (Push-pull Mode)	-20	-25	-	mA	V_{DD} = 4.5 V, V_S = 2.4 V
I_{SR22}		-3	-5	-	mA	V_{DD} = 2.7 V, V_S = 2.2 V
I_{SR23}		-2.5	-4.5	-	mA	V_{DD} = 2.5 V, V_S = 2.0 V
I_{SK11}	Sink Current (Quasi-bidirectional, Open-Drain and Push-pull Mode)	10	15	-	mA	V_{DD} = 4.5 V, V_S = 0.45 V
I_{SK12}		6	9	-	mA	V_{DD} = 2.7 V, V_S = 0.45 V
I_{SK13}		5	8	-	mA	V_{DD} = 2.5 V, V_S = 0.45 V

Notes:

1. nRST pin is a Schmitt trigger input.
2. XTAL1 is a CMOS input.
3. Pins can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, the transition current reaches its maximum value when V_{IN} approximates to 2V.

7.3 AC Electrical Characteristics

7.3.1 External Input Clock



Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

7.3.2 External 4~24 MHz High Speed Crystal (HXT)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Condition
V_{HXT}	Operation Voltage	2.5	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
I_{HXT}	Operating Current	-	2.6	-	mA	12 MHz, V_{DD} = 5.5V
		-	1.3	-	mA	12 MHz, V_{DD} = 3.3V
f_{HXT}	Clock Frequency	4	-	24	MHz	-

7.3.3 Typical Crystal Application Circuits

Crystal	C1	C2
4 MHz ~ 24 MHz	10~20 pF	10~20 pF

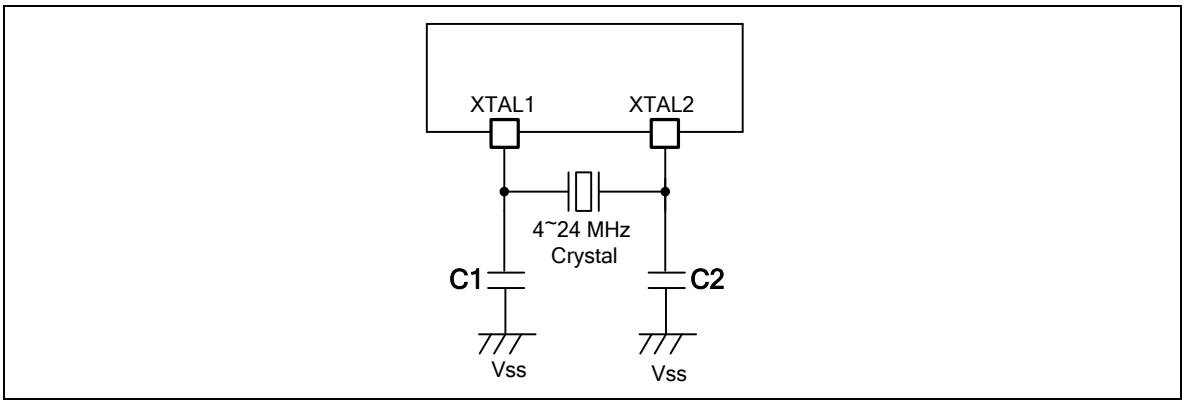


Figure 7.3-1 NUC442 Typical Crystal Application Circuit

7.3.4 External 32 kHz Low Speed Crystal (LXT)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Condition
V_{LXT}	Operation Voltage	2.5	-	5.5	V	-
T_A	Temperature	-40	-	85	℃	-
I_{LXT}	Operating Current	-	1.6	-	uA	V_{BAT} = 3.3V
F_{LXT}	Clock Frequency	-	32768	-	Hz	-

7.3.5 22.1184 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{HRC}	Supply Voltage	1.62	1.8	1.98	V	-
f_{HRC}	Center Frequency	-	22.1184	-	MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	T_A = 25℃ V_{DD} = 5 V
		-2	-	+2	%	T_A = -40℃ ~ 105℃ V_{DD} = 2.5 V ~ 5.5 V
I_{HRC}	Operating Current	-	655	-	μA	T_A = 25℃,V_{DD} = 3.3 V

7.3.6 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{LRC}	Supply Voltage	2.5	-	5.5	V	-
f_{LRC}	Center Frequency	-	10	-	kHz	-
	Oscillator Frequency	-25	-	+25	%	V_{DD} = 2.5 V ~ 5.5 V T_A = 25℃
		-40	-	+40	%	V_{DD} = 2.5 V ~ 5.5 V T_A = -40℃ ~ +105℃

7.3.7 Input/Output AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
Tf_{IO}	Output High to Low Level Fall Time	-	7[2]	-	ns	V_{DD} = 5 V, T_A = 25℃ CL=30p GPIOx_HS = 0[1]
		-	5[2]	-	ns	V_{DD} = 5 V, T_A = 25℃ CL=30p GPIOx_HS = 1[1]
Tr_{IO}	Output Low to High Level Rise Time	-	7[2]	-	ns	V_{DD} = 5 V, T_A = 25℃ CL=30p GPIOx_HS = 0[1]
		-	6[2]	-	ns	V_{DD} = 5 V, T_A = 25℃ CL=30p GPIOx_HS = 1[1]

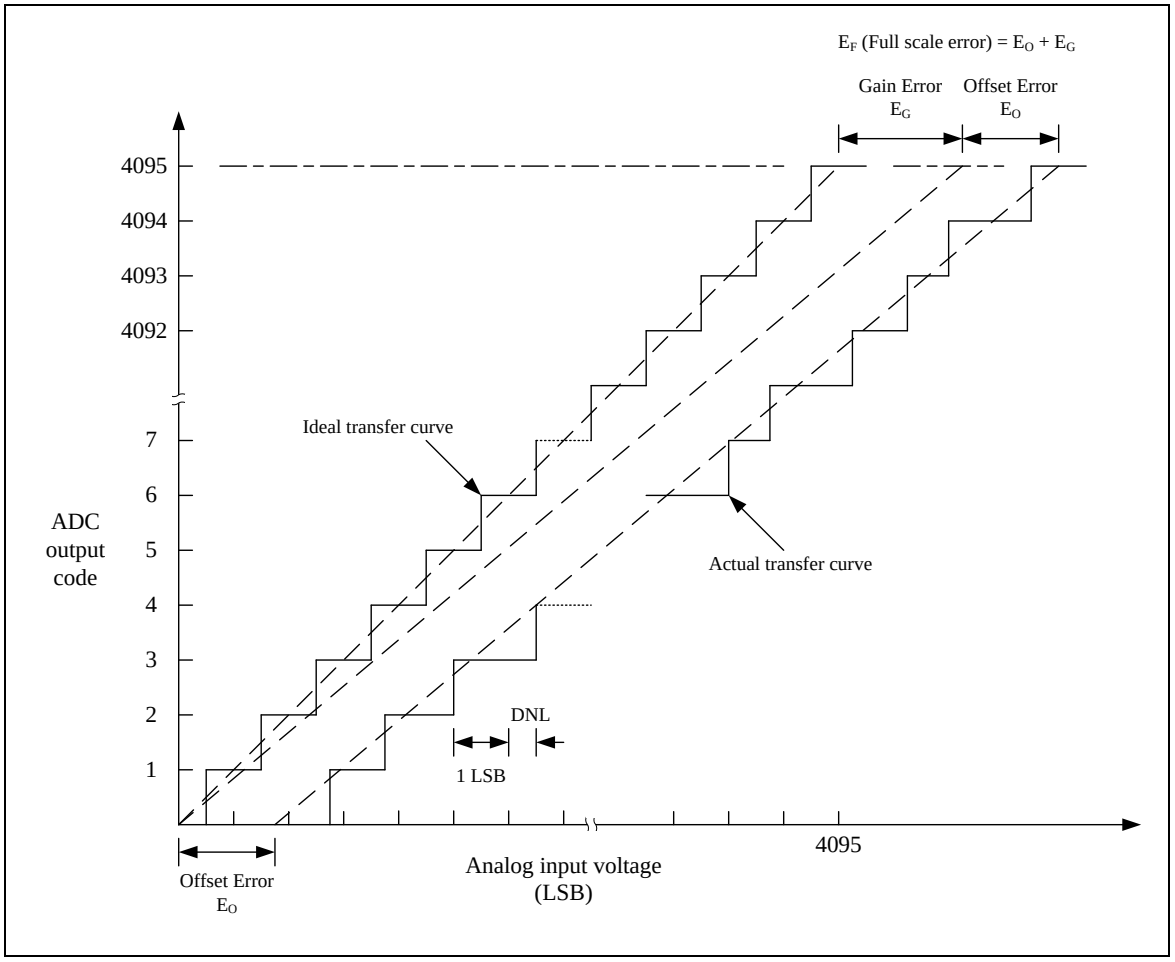
Notes:

1. The I/O speed is configured using the GPIOx_HS bits. Refer to the TRM for a description of GPIO Port configuration register.
2. Guaranteed by design, and not tested in production.

7.4 Analog Characteristics

7.4.1 12-bit SAR ADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	12	Bit	-
DNL	Differential Nonlinearity Error	-	±1	-1~+4	LSB	-
INL	Integral Nonlinearity Error	-	±2	±4	LSB	-
E_O	Offset Error	-	2	4	LSB	-
E_G	Gain Error (Transfer Gain)	-	-2	-4	LSB	-
E_A	Absolute Error	-	3	4	LSB	-
-	Monotonic	Guaranteed			-	-
F_{ADC}	ADC Clock Frequency	-	-	16	MHz	AV_{DD} = 4.5~5.5 V
		-	-	8		AV_{DD} = 2.5~5.5 V
F_S	Sample Rate (F_{ADC}/T_{CONV})	-	-	800	kSPS	AV_{DD} = 4.5~5.5 V
		-	-	400	kSPS	AV_{DD} = 2.5~5.5 V
T_{ACQ}	Acquisition Time (Sample Stage)	7			$1/F_{ADC}$	-
T_{CONV}	Total Conversion Time	20			$1/F_{ADC}$	-
AV_{DD}	Supply Voltage	2.5	-	5.5	V	-
I_{DDA}	Supply Current (Avg.)	-	2.9	-	mA	AV_{DD} = 5 V
V_{IN}	Analog Input Voltage	0	-	AV_{DD}	V	-
C_{IN}	Input Capacitance	-	7	-	pF	-
R_{IN}	Input Load	-	6	-	kΩ	-



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

7.4.2 LDO and Power Management

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	DC Power Supply	2.5	-	5.5	V	-
V_{LDO}	Output Voltage	1.62	1.8	1.98	V	-
T_A	Temperature	-40	25	105	℃	-
C_{LDO}	Capacitor	-	1	-	μF	R_{ESR} = 1Ω

Notes:

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 1μF or higher capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

7.4.3 Low Voltage Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-
T_A	Temperature	-40	25	105	℃	-
I_{LVR}	Quiescent Current	-	1	5	μA	AV_{DD} = 5.5 V
V_{LVR}	Threshold Voltage	1.9	2.00	2.10	V	T_A = 25℃
		1.7	1.90	2.10	V	T_A = -40℃
		2.00	2.20	2.45	V	T_A = 105℃

7.4.4 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-
T_A	Temperature	-40	25	105	℃	-
I_{BOD}	Quiescent Current	-	120	-	μA	AV_{DD} = 5.5 V
V_{BOD}	Brown-out Voltage (Falling edge)	4.2	4.4	4.6	V	BOV_VL [1:0] = 11
		3.5	3.7	3.9	V	BOV_VL [1:0] = 10
		2.5	2.7	2.9	V	BOV_VL [1:0] = 01
		2.0	2.2	2.4	V	BOV_VL [1:0] = 00
V_{BOD}	Brown-out Voltage (Rising edge)	4.3	4.5	4.8	V	BOV_VL [1:0] = 11
		3.6	3.8	3.9	V	BOV_VL [1:0] = 10
		2.5	2.7	2.9	V	BOV_VL [1:0] = 01
		2.0	2.2	2.4	V	BOV_VL [1:0] = 00

7.4.5 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	105	℃	-
V_{POR}	Reset Voltage	-	2.0	-	V	V+
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	-	-	100	mV	-
RR_{VDD}	V_{DD} Raising Rate to Ensure Power-on Reset	0.025	-	-	V/ms	-
t_{POR}	Minimum Time for V_{DD} Stays at VPOR to Ensure Power-on Reset	0.5	-	-	ms	-

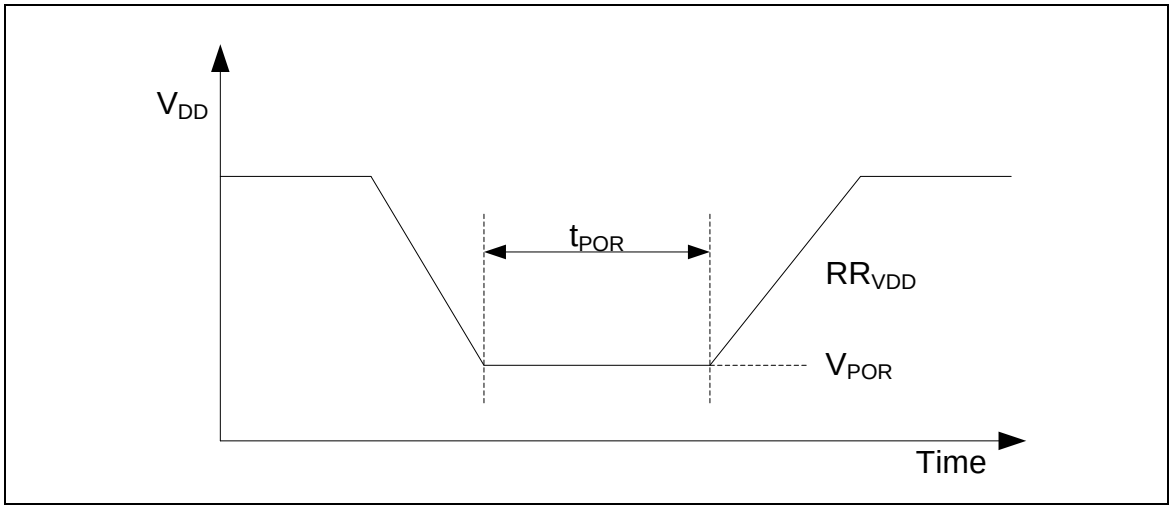


Figure 7.4-1 Power-up Ramp Condition

7.4.6 Temperature Sensor

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{TEMP}	Supply Voltage	1.62	1.8	1.98	V	
T_A	Temperature	-40	-	105	℃	
I_{TEMP}	Current Consumption	-	3	-	μA	
-	Gain	-1.65	-1.66	-1.68	mV/℃	
-	Offset	760	762	766	mV	T_A = 0℃

Note:

The temperature sensor formula for the output voltage (Vtemp) is as below equation.

Vtemp (mV) = Gain (mV/℃) x Temperature (℃) + Offset (mV)

7.4.7 Comparator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{CMP}	Supply Voltage	2.5		5.5	V	
T_A	Temperature	-40	25	105	℃	-
I_{CMP}	Operation Current	-	35	70	μA	AV_{DD} = 5 V
V_{OFF}	Input Offset Voltage		10	20	mV	-
V_{SW}	Output Swing	0.1	-	AV_{DD} - 0.1	V	-
V_{COM}	Input Common Mode Range	0.35	-	AV_{DD} - 0.3	V	-
-	DC Gain	40	70	-	dB	-
T_{PGD}	Propagation Delay	-	200	-	ns	V_{CM} = 1.2 V, V_{DIFF} = 0.1 V
V_{HYS}	Hysteresis	-	±40	±60	mV	
T_{STB}	Stable time	-	-	1	μs	

7.4.8 OP Amplifier

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AV_{DD}	-	3.0	3.3	5.5	V
Input offset voltage	-	-	2	5	mV
Input offset average drift		-	-	1	uV/℃
Output swing	-	0.1	-	V_{DD}-0.1	V
Input common mode range	-	0.1	-	V_{DD}-1.2	V

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
DC gain	-	-	80	-	dB
Unity gain freq.	AV_{DD}=5V	-	-	5	MHz
Phase margin		-	50°	-	°
PSRR+	AV_{DD}=5V	-	90	-	dB
CMRR	AV_{DD}=5V	-	90	-	dB
Slew rate	AV_{DD}=5V, RLOAD=33K, CLOAD=50p	6.0	-	-	V/us
Wake up time		-	-	1	us
Quiescent current		-	600	-	uA

7.4.9 Internal Voltage Reference

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{VREF}	AV_{DD}	-	2.4		5.5	V
V_{ref1}	V_{REF}(2.56V)	AV_{DD} >= 2.9V	2.483	2.56	2.637	V
V_{ref2}	V_{REF}(2.048V)	AV_{DD} >= 2.4V	1.986	2.048	2.109	V
V_{ref3}	V_{REF}(3.072V)	AV_{DD} >= 3.4V	2.98	3.072	3.164	V
V_{ref4}	V_{REF}(4.096V)	AV_{DD} >= 4.5V	3.973	4.096	4.219	V

7.4.10 USB PHY Specification

7.4.10.1 Low-/full-Speed DC Electrical Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High (driven)		2.0			V
V_{IL}	Input Low				0.8	V
V_{DI}	Differential Input Sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential Common-mode Range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended Receiver Threshold		0.8		2.0	V
	Receiver Hysteresis			200		mV
V_{OL}	Output Low (driven)		0		0.3	V
V_{OH}	Output High (driven)		2.8		3.6	V
V_{CRS}	Output Signal Cross Voltage		1.3		2.0	V
R_{PU}	Pull-up Resistor		1.425		1.575	kΩ
Z_{DRV}	Driver Output Resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver Capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

7.4.10.2 High-Speed DC Electrical Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{HSDI}	High-speed differential Input level	|PADP-PADM|	150			mV
V_{HSSQ}	High-speed SQ detection threshold	|PADP-PADM|	100		150	mV
V_{HSCM}	High-speed Common-mode Range		-50		500	mV
V_{HSOL}	High-speed Output Low		-10		10	mV
V_{HSOH}	High-speed Output High		360		440	mV
V_{CHIRPJ}	Chirp J level		700		1100	mV
V_{CHIRPK}	Chirp K level		-900		-500	mV
Z_{HSDRV}	High-speed Driver Output Resistance	45Ω±10%	40.5		49.5	Ω

7.4.10.3 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	C_L=50p	4		20	ns
T_{FF}	Fall Time	C_L=50p	4		20	ns
T_{FRFF}	Rise and Fall Time Matching	$T_{FRFF}=T_{FR}/T_{FF}$	90		111.11	%

7.4.10.4 USB High-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{HSR}	Rise Time	Z_{HSDRV}=45Ω	500		900	ps
T_{HSF}	Fall Time	Z_{HSDRV}=45Ω	500		900	ps

7.4.10.5 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{VBUS}	VBUS Current (Steady State)	Standby		TBD		μA

7.4.10.6 USB LDO Specification

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BUS}	VBUS Pin Input Voltage		4.0	5.0	5.5	V
V_{DD33}	LDO Output Voltage		2.97	3.3	3.63	V
C_{bp}	External Bypass Capacitor			1.0	-	uF

7.5 Flash DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply Voltage	1.62	1.8	1.98	V	
T_{RET}	Data Retention	100	-	-	year	T_A = 25℃
T_{ERASE}	Page Erase Time	20	-	-	ms	
T_{PROG}	Program Time	40	-	-	us	
	Endurance		20000		times	

Notes:

1. V_{FLA} is source from chip LDO output voltage.
2. Guaranteed by design, and not tested in production.

7.6 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min.	Max.	Min.	Max.	
t_{LOW}	SCL low period	4.7		1.2		uS
t_{HIGH}	SCL high period	4		0.6		uS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7		1.2		uS
$t_{HD;\ STA}$	START condition hold time	4		0.6		uS
$t_{SU;\ STO}$	STOP condition setup time	4		0.6		uS
t_{BUF}	Bus free time	4.7[3]		1.2[3]		uS
$t_{SU;DAT}$	Data setup time	250		100		nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r	SCL/SDA rise time		1000	20+0.1Cb	300	nS
t_f	SCL/SDA fall time		300		300	nS
C_b	Capacitive load for each bus line		400		400	pF

Notes:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

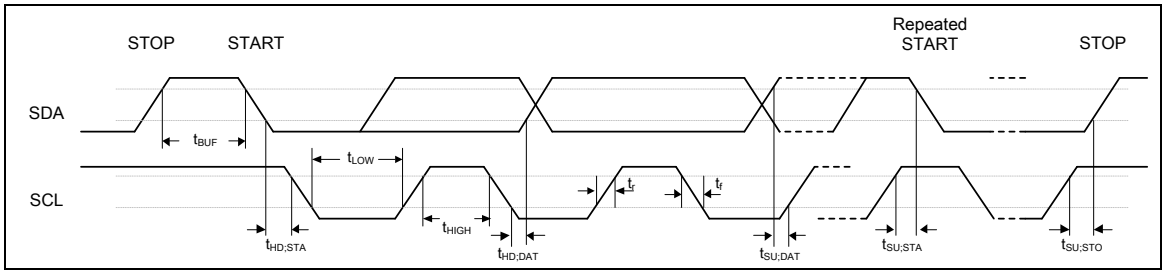


Figure 7.6-1 I²C Timing Diagram

7.7 SPI Dynamic Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
SPI Master Mode (V_{DD} = 4.5 V ~ 5.5 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	4	-	-	ns
t_V	Data output valid time	-	1	2	ns
SPI Master Mode (V_{DD} = 3.0 V ~ 3.6 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0			ns
t_{DH}	Data hold time	4.5			ns
t_V	Data output valid time		2	4	ns
SPI Slave Mode (V_{DD} = 4.5 V ~ 5.5 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	3.5	-	-	ns
t_V	Data output valid time	-	16	22	ns
SPI Slave Mode (V_{DD} = 3.0 V ~ 3.6 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0			ns
t_{DH}	Data hold time	4.5			ns
t_V	Data output valid time		18	24	ns

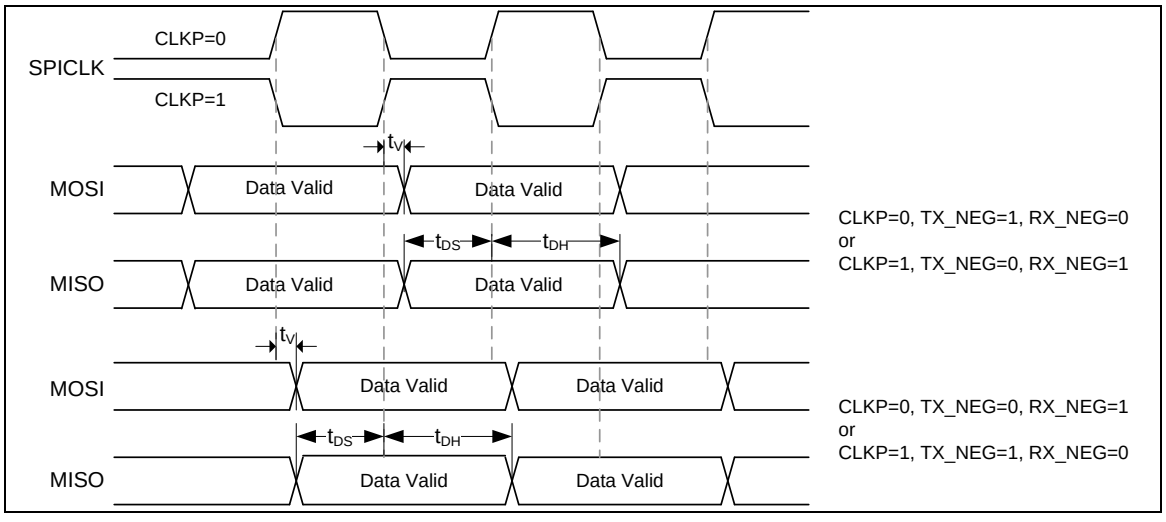


Figure 7.7-1 SPI Master Mode Timing Diagram

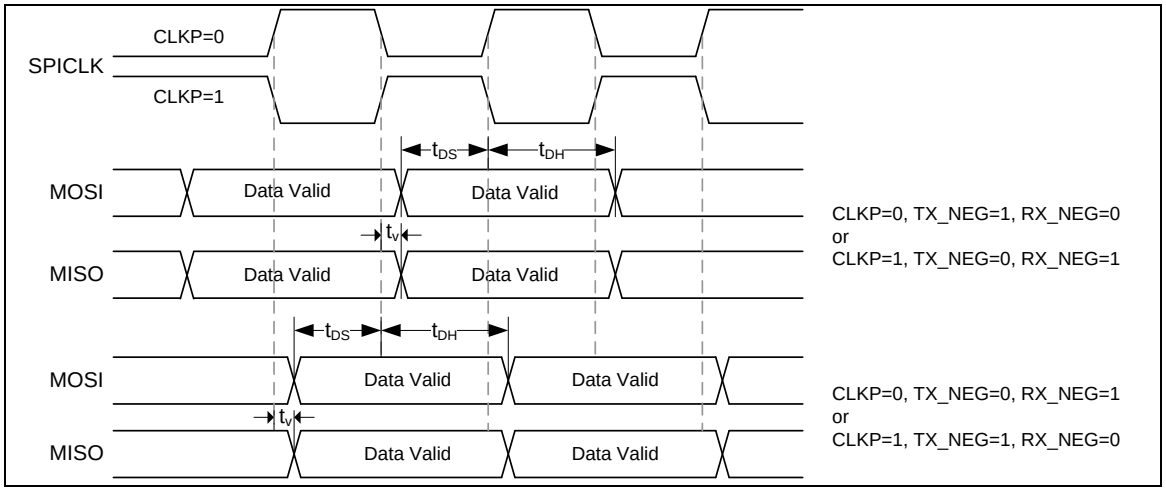


Figure 7.7-2 SPI Slave Mode Timing Diagram

7.8 I²S Dynamic Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{w(CKH)}$	I²S clock high time	Master fPCLK = MHz, data: 24 bits, audio frequency = 256 kHz	42	-	ns
$t_{w(CKL)}$	I²S clock low time		37	-	
$t_{v(WS)}$	WS valid time	Master mode	7	-	
$t_{h(WS)}$	WS hold time	Master mode	1	-	
$t_{su(WS)}$	WS setup time	Slave mode	34	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
DuCy(SCK)	I²S slave input clock duty cycle	Slave mode	25	75	%
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	0	-	ns
$t_{su(SD\_SR)}$		Slave receiver	0	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$		Slave receiver	0	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	32	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	16	-	
$t_{v(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	-	5	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	0	-	

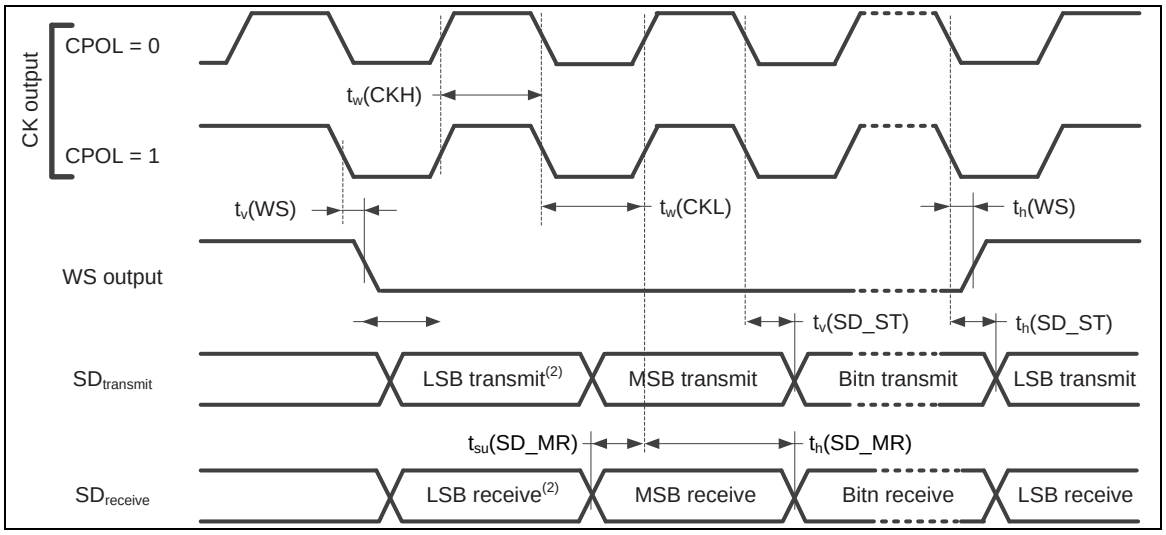


Figure 7.8-1 I^{2}S Master Mode Timing Diagram

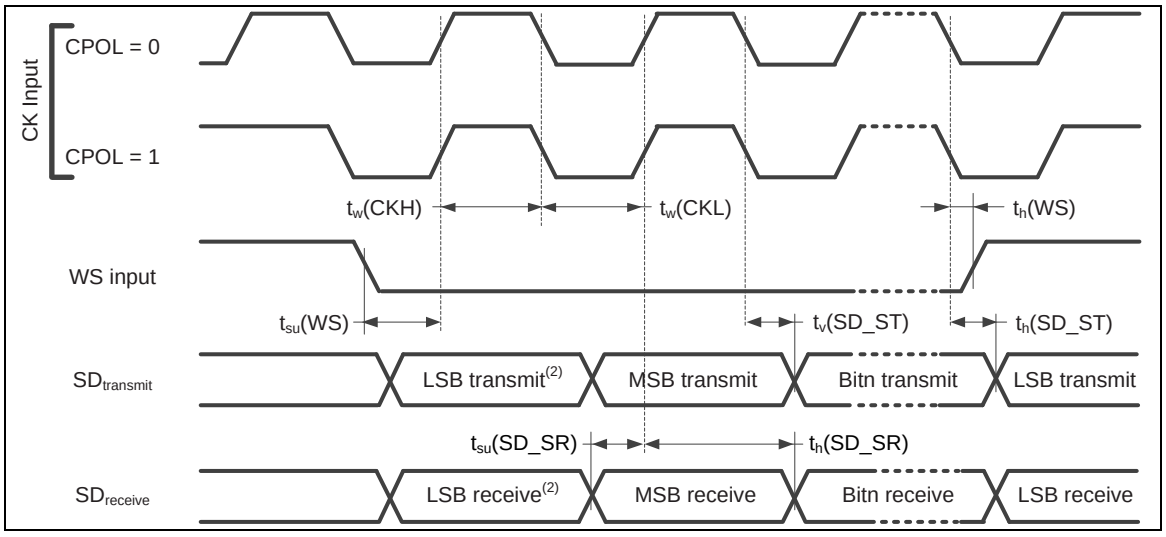
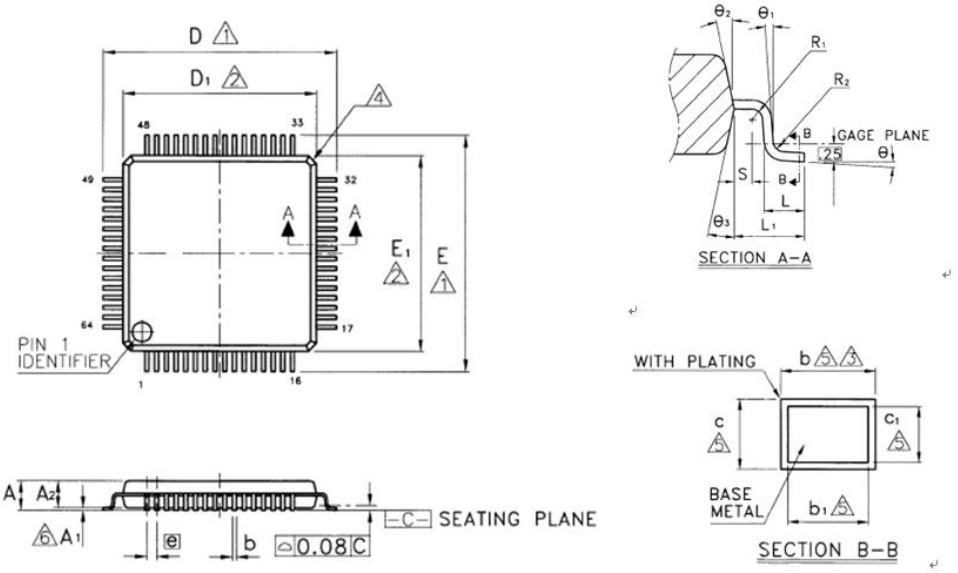


Figure 7.8-2 I^{2}S Slave Mode Timing Diagram

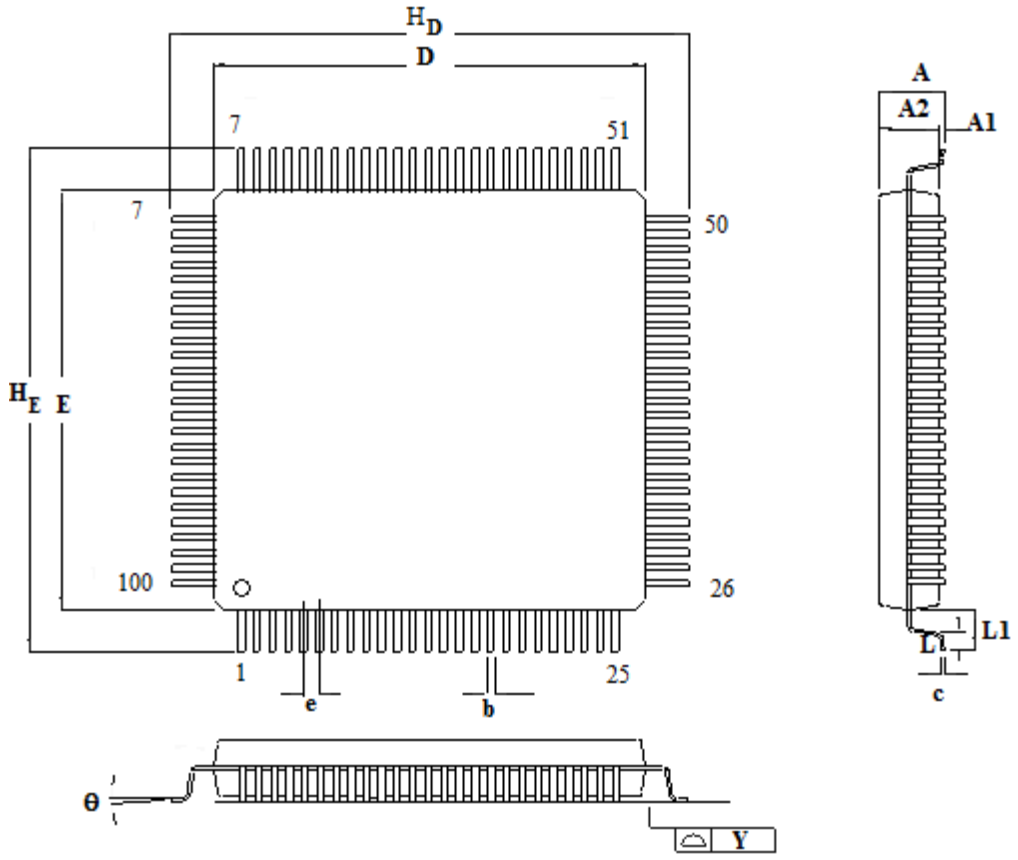
8 PACKAGE DIMENSIONS

8.1 LQFP 64L (10x10x1.4 mm footprint 2.0 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.394 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		

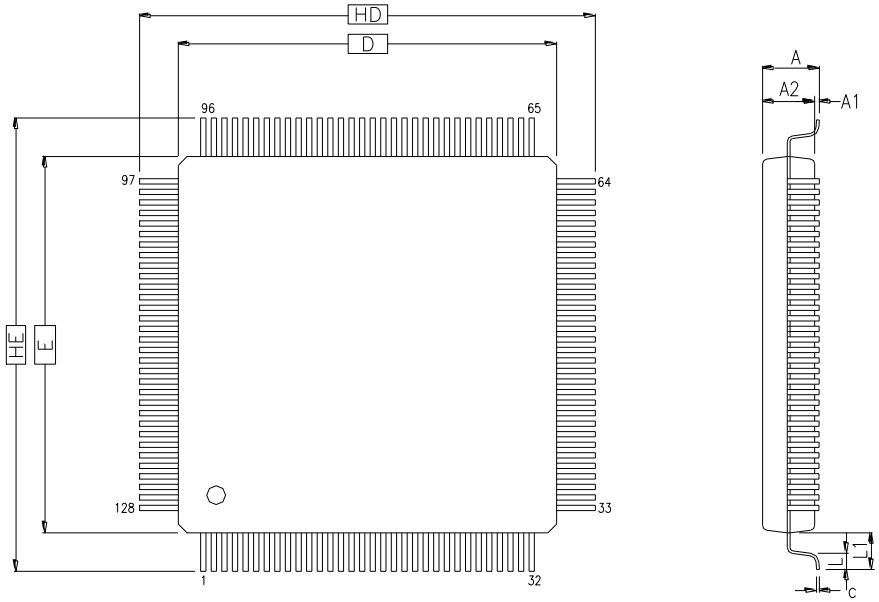
8.2 LQFP 100L (14x14x1.4 mm footprint 2.0 mm)



Controlling Dimension : Millimeters

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	-
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.10	0.15	0.20
D	13.90	14.00	14.10
E	13.90	14.00	14.10
e	-	0.50	-
HD	15.80	16.00	16.20
HE	15.80	16.00	16.20
L	0.45	0.60	0.75
L1	-	1	-
y	-	-	0.10
θ	0°	-	7°

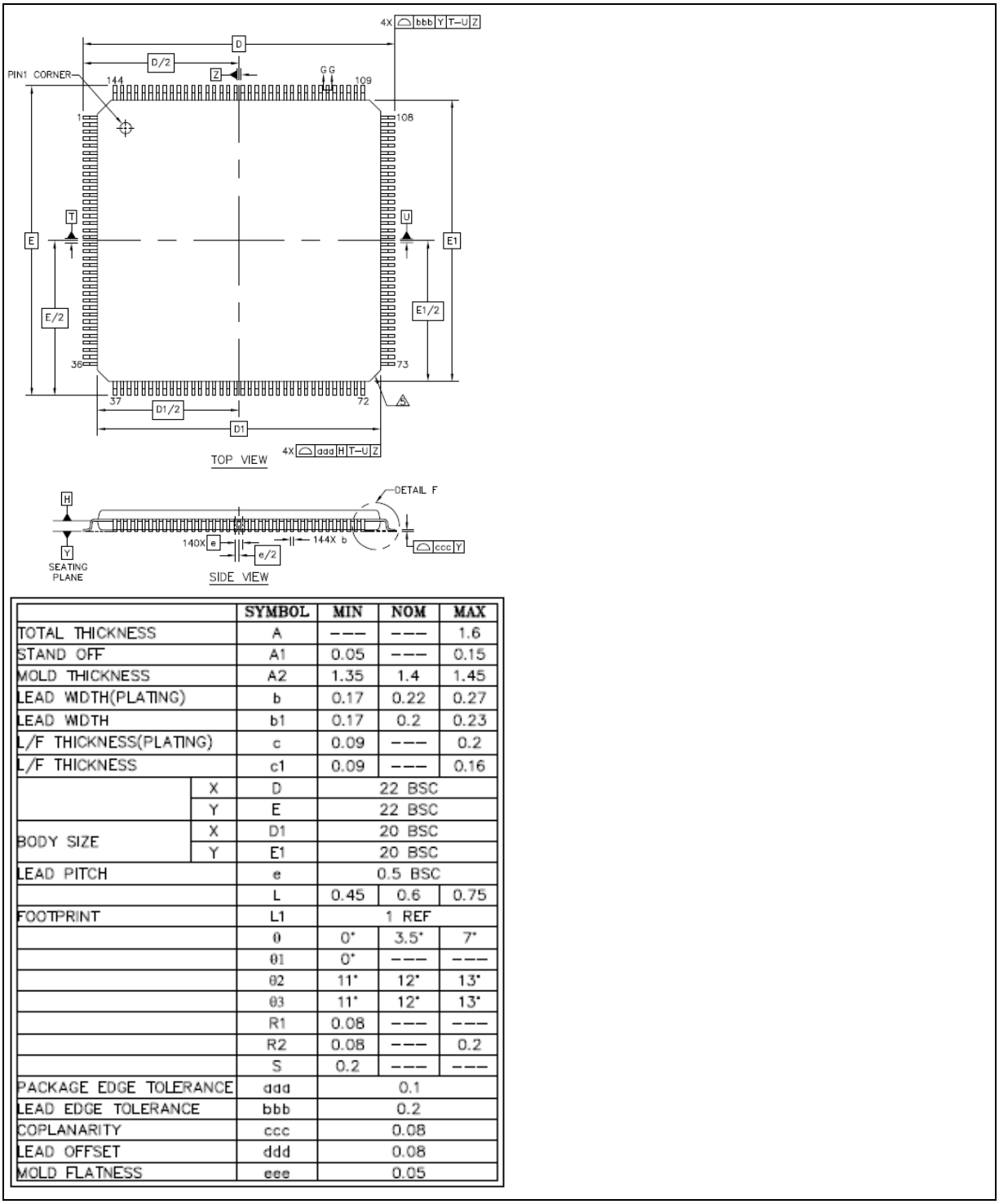
8.3 LQFP 128L (14x14x1.4 mm footprint 2.0 mm)



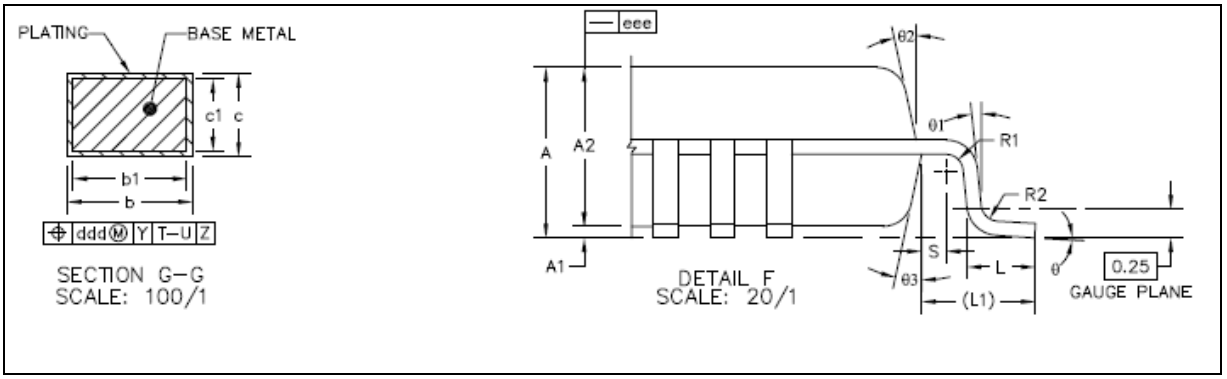
COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

8.4 LQFP 144L (20x20x1.4 mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.17	0.22	0.27
LEAD WIDTH		b1	0.17	0.2	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	22 BSC		
	Y	E	22 BSC		
	X	D1	20 BSC		
	Y	E1	20 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.1		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		


PLATING
BASE METAL
c1
c
b1
b
ddd M Y T–U Z
SECTION G–G
SCALE: 100/1
eee
θ2
θ1
R1
R2
A
A2
A1
S
L
θ
θ3
(L1)
0.25
GAUGE PLANE
DETAIL F
SCALE: 20/1

9 REVISION HISTORY

Date	Revision	Description
2013.11.01	1.01	1. Preliminary version.
2013.11.15	1.02	1. Editorial changes.
2014.01.29	1.03	1. Updated the Clock Generator Global View Diagram. 2. Updated the LQFP 64L package dimension.
2014.04.16	1.04	1. Modified the pin description table.
2014.05.23	1.05	1. Added the I^2C, SPI and I^2S Dynamic Characteristics.
2014.07.21	1.06	1. Modified the Section 4.2 Pin Configuration and Section 4.3 Pin Description. 2. Modified the SPI Features. 3. Added SRAM origination and description.
2015.04.15	1.07	1. Added the clock switch note in all clock source blocks. 2. Updated the Section 4.2 Pin Configuration and Section 4.3 Pin Description for the NUC442-LQFP64. 3. Added the note description for V_{REF} and LDO_CAP pins. 4. Updated the Clock Generator Global View Diagram.
2016.03.10	1.08	1. Removed the Serial Wire Viewer (SWV) in the Section 2.1 Features. 2. Corrected some EBI_ADxx description typo in the Section 4.3 Pin Description. 3. Corrected the Figure 6.3-1 and Figure 6.3-2.
2016.06.16	1.09	1. Removed the PDMA time-out function description in the Section 2.1 and Section 6.7.

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