

**CSMF SERIES: Multi-Frequency Oscillator with Low Jitter Output 10MHz – 1200MHz**

### ■ PRODUCT DESCRIPTION

The CSMF clock series is a cutting edge family of High Frequency, Low Jitter Output, Multi-Frequency Clock Oscillators based on an advanced digital PLL platform. The CSMF clocks are available in a 7x5mm ceramic package with output frequency from 10MHz to 1.2 GHz. The CSMF units are pre-programmed with up to 2 different output frequencies, any of which are user selected. Such flexibility significantly reduces design cycle time and overall cost. The CSMF clock design incorporates a low frequency crystal along with low Jitter frequency synthesizer to provide a wide range of frequencies. The CSMF Clocks are available in LVCMOS, LVPECL and LVDS outputs, making them suitable for a wide range of applications.

### ■ APPLICATION

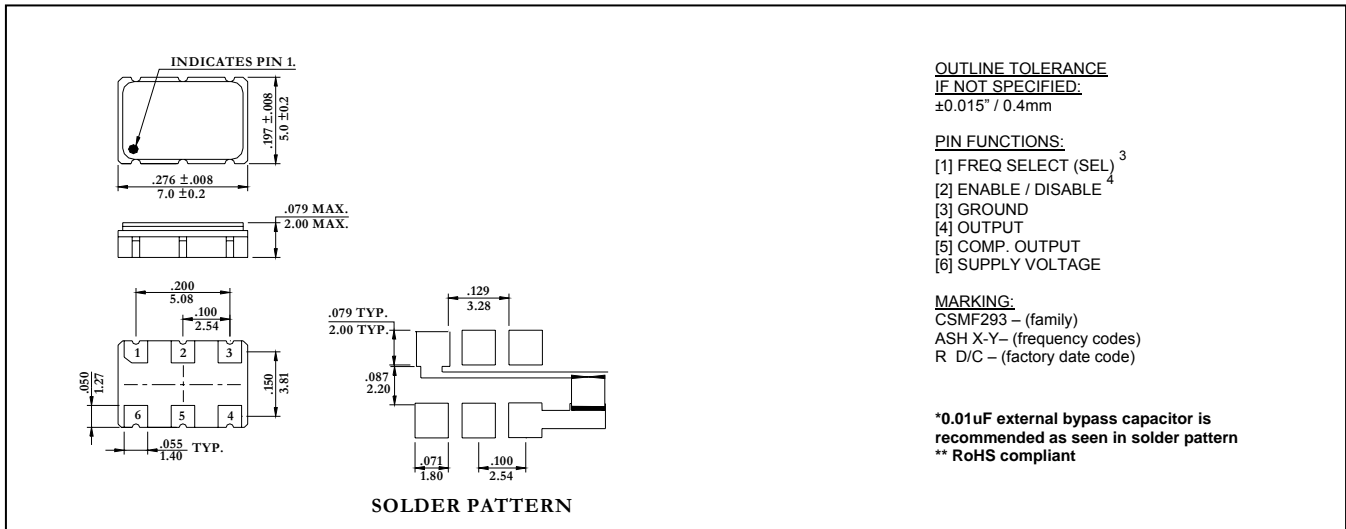
- SONET/SDH
- FIBRE CHANNEL
- 10G,100G, GIGABIT ETHERNET
- CLOCK / DATA RECOVERY
- TEST AND MEASUREMENT

### ■ ELECTRICAL SPECIFICATION

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Frequency, nominal	$f_o$	Up to 2 available output frequencies	10 -1200	MHz
Supply voltage, nom.	$V_{CC}$		2.5 or 3.3	V
Supply current	$I_s$	Typical (depending on output)	35 ~ 45	mA
LVPECL output levels	VOH	Output termination 50Ω ~ Vcc - 2.0V	$V_{CC} - 1.4 \sim V_{CC} - 0.9$	V
	VOL		$V_{CC} - 2.0 \sim V_{CC} - 1.7$	V
LVPECL output voltage swing	$V_{p-p}$	Output termination 50Ω ~ Vcc - 2.0V	0.6 ~ 1.0	V
LVDS differential output voltage	$\Delta V_{OD}$	100Ω termination between outputs	350	mV
LVDS offset voltage, typical	$V_{OS}$		1.25	V
LVCMOS / LVTTTL output levels	VOH / VOL	min/max	$0.7V_{CC} / 0.3V_{CC}$	V
Duty cycle	DC	Load = 10kΩ // 20pF	40/60 or 45/55	%
Rise/ fall time, max.	$t_r / t_f$	20% - 80% (VOL, VOH)	0.6	ns
RMS phase jitter	J	Typical	0.8	ps
Overall freq. stability, max. <sup>1</sup>	$\Delta f/f_c$	Various available, specified when ordered	$\pm 20 \sim \pm 100$ .	ppm
Enable / Disable	En / Dis	Min (logic 1) / Max (logic 0)	$0.7 (V_{CC}) / 0.3 (V_{CC})$	V
Operating temperature	$T_a$		-40 ~ +85	°C
Storage temperature	T(stg)	Absolute max	-45 ~ +100	°C
Absolute voltage range	$V_{CC(ABS)}$		$V_{CC} \pm 0.5$	V

**Notes**<sup>1</sup>See part numbering table<sup>2</sup>Contact factory

### MECHANICAL SPECIFICATION



#### Notes

<sup>3</sup> Frequency Select pin (SEL)

Logic 1 (NC) = Output Frequency 1 (First frequency listed in part # is automatically available. Customer specified at time of order)

Logic 0 = Output Frequency 2 (Second frequency listed in part # is available. Customer sets SEL pin to Low)

<sup>4</sup> Enable / Disable feature is available on either pin 1 or pin 2. See options on part numbering table.

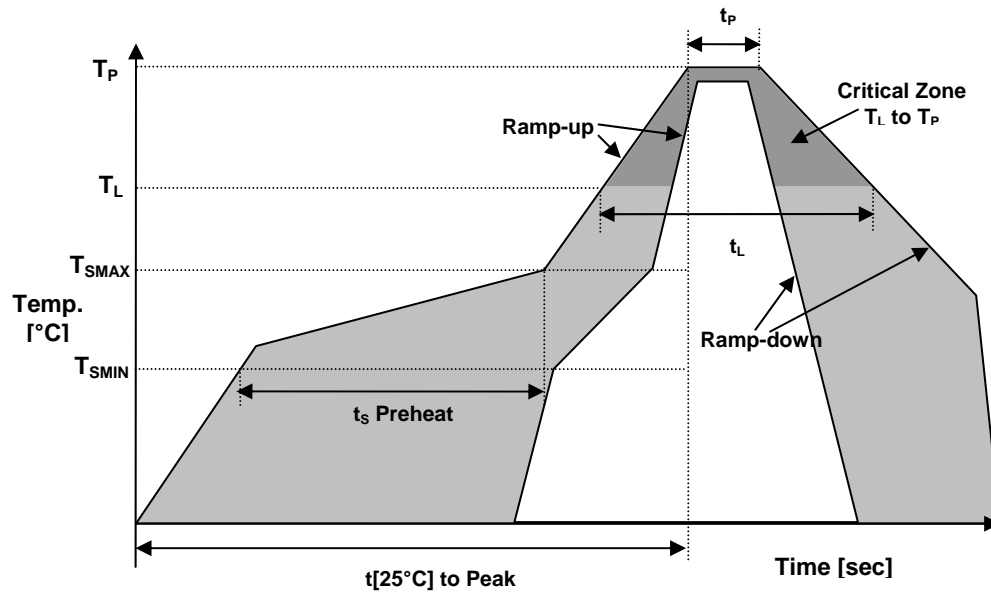
### PART NUMBERING SYSTEM:

SERIES	NUMBER OF OUTPUTS	OUTPUT	SUPPLY VOLTAGE (V)	SYMMETRY (%)	TEMP RANGE (°C)	FREQUENCY STABILITY (ppm)	ENABLE / DISABLE PIN	OUTPUT FREQUENCY (MHz)
Surface mount Multi-frequency Clock Oscillator	1: Single Output 2: Dual Output	9: LVPECL 8: LVDS 4: LVCMOS	1: Vcc =2.5 3: Vcc =3.3	A: 40/60 T: 45/55	R: 0~50 S: 0~70 U: -20~70 V: -40~85	K: ±20 I: ±25 H: ±50 J: ±100	1: Pin 1 2: Pin 2	XXX.XXX-YYY.YYY Freq1- Freq 2
<b>CSMF</b>	<b>2</b>	<b>9</b>	<b>3</b>	<b>A</b>	<b>S</b>	<b>H</b>	<b>2</b>	<b>-</b>
								<b>XXX-YYY</b>

#### EXAMPLE: CSMF293ASH2-622-311

Clock Oscillator, 7x5mm package, Dual output, LVPECL, +3.3V Supply, 40/60 Symmetry, 0~+70°C Operating Temperature Range, ±50ppm overall Frequency Stability, Enable/Disable on pin 2, 622.080 MHz and 311.040MHz output frequency.

■ REFLOW PROFILE:



Reflow profile IPC/JEDEC J-STD-020 REV. C			
Temperature Min Preheat	$T_{SMIN}$		150°C
Temperature Max Preheat	$T_{SMAX}$		200°C
Time ( $T_{SMIN}$ to $T_{SMAX}$ )	$t_s$		60-180 sec.
Temperature	$T_L$		217°C
Peak Temperature	$T_P$		260°C
Ramp-up rate	$R_{UP}$		3°C/sec max.
Ramp-down rate	$R_{DOWN}$		6°C/sec max.
Time within 5°C of Peak Temperature	$t_p$		20-40 sec.
Time $t[25^\circ\text{C}]$ to Peak Temperature	$t[25^\circ\text{C}] \text{ to Peak}$		480 sec.
Time	$t_L$		60-150 sec.